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Implementing STDP

on SpiNNaker

Xin Jin, Alexander Rast, Francesco Galluppi,
Sergio Davies, Steve Furber

APT group
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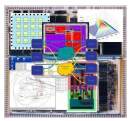

EPSRC

ARM

Silistix

SpiNNaker
a universal
Spiking Neural Network
architecture

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Overview of the topics

- Neural network chip architectures
- Features of the SpiNNaker chip
- Neural simulation
- Spike Timing Dependent Plasticity
- Implementation in SpiNNaker
- Future learning algorithm

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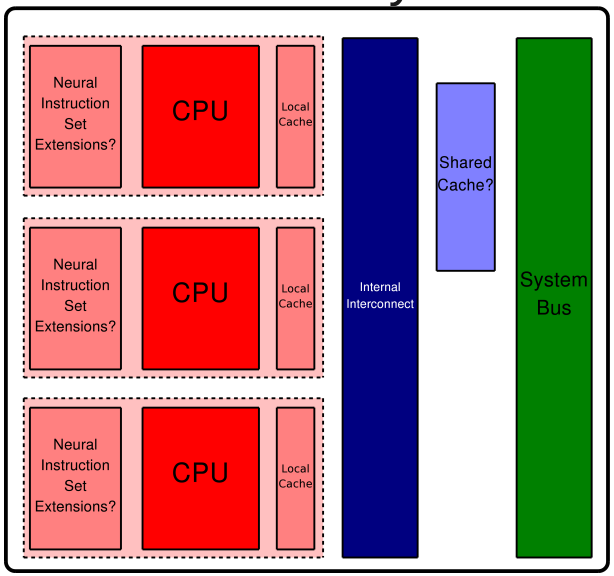
Neural network chip architectures

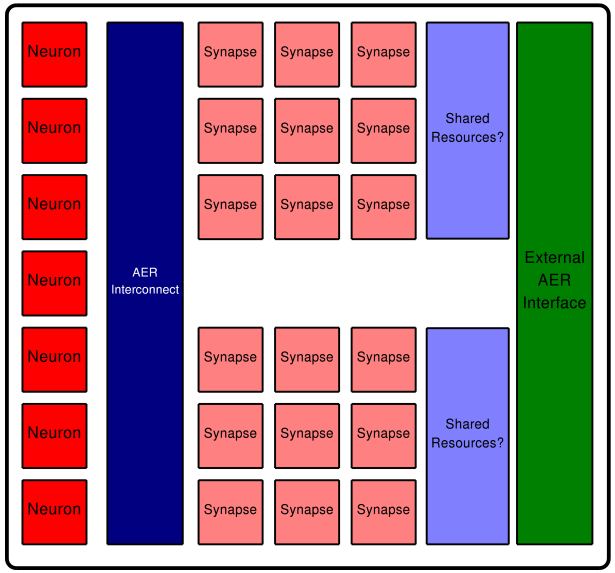
NEUROPROCESSOR

- Domain-specific multiprocessors
- High programmability
- Limited biological fidelity
- Minimal exploitation of intrinsic neurodynamics



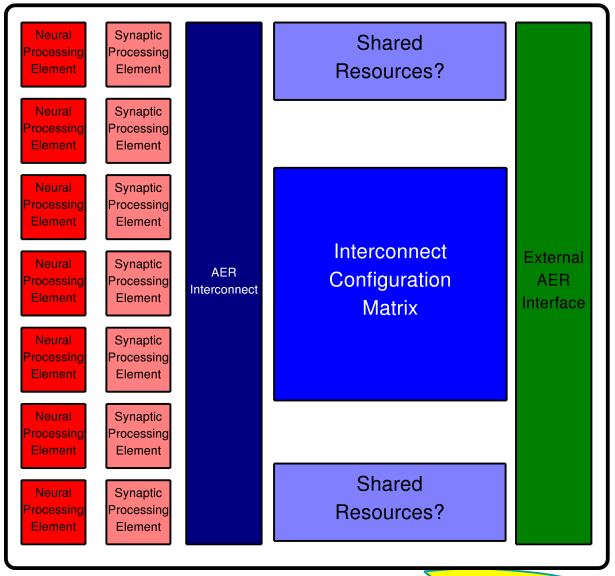
NEUROMORPHIC

- Application-specific neuroprocessors
- Limited model support
- High biological fidelity
- Minimum exploitation of configuration



NEUROMIMETIC

- Universal neuromorphic chip
- Dynamic configurability
- Tunable biological fidelity
- Balance neurocomputing and programmability



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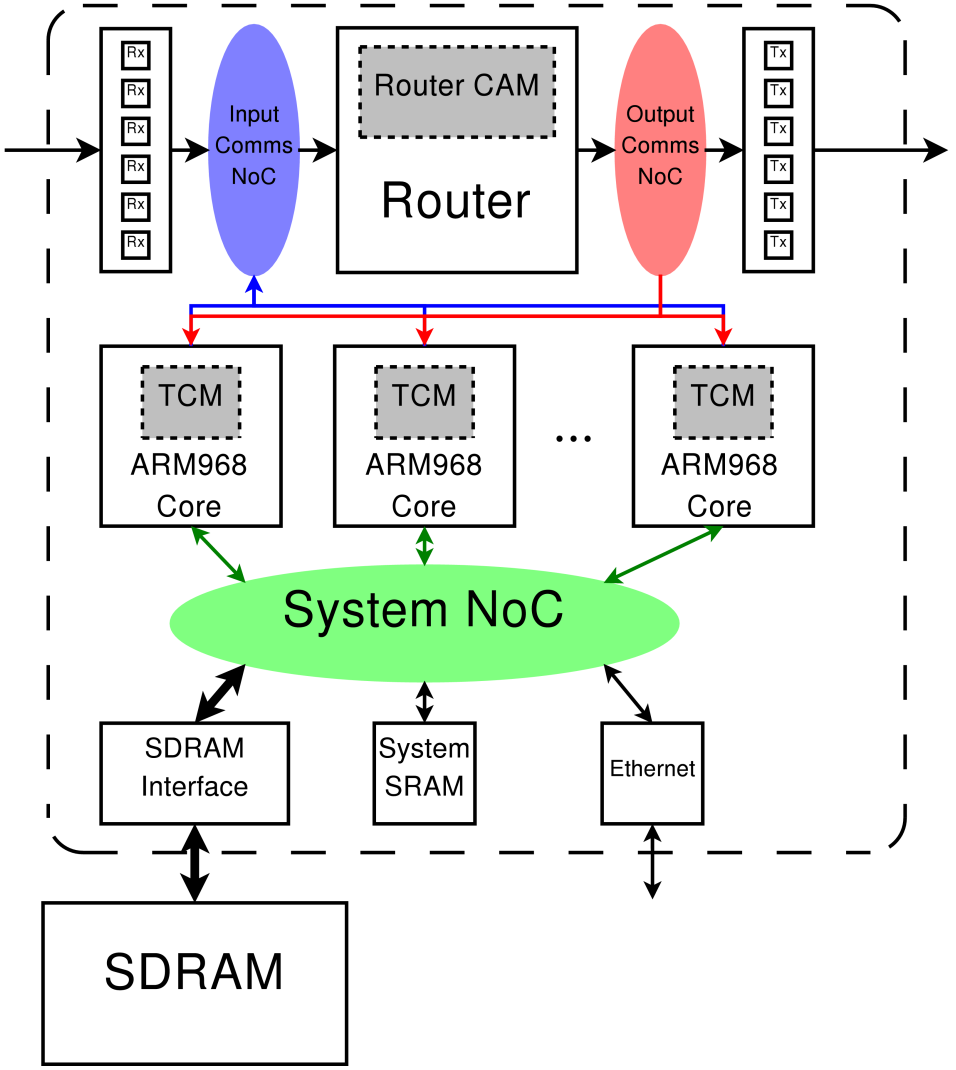
Features of the SpiNNaker chip

- Native parallelism
- Event-driven processing
- Incoherent memory
- Incremental reconfiguration



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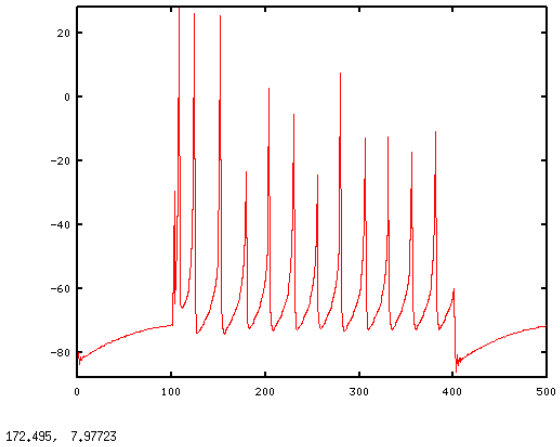
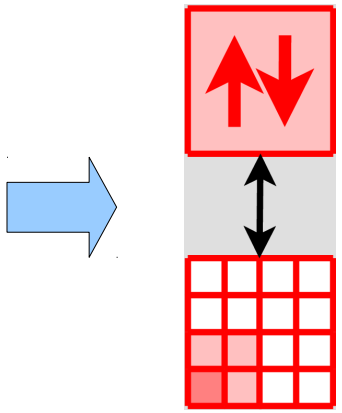
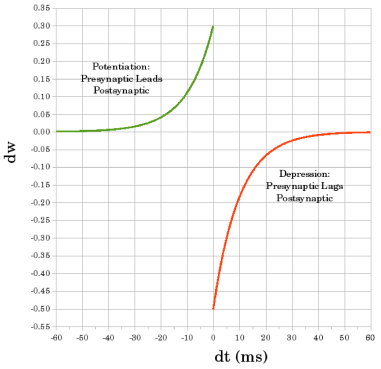
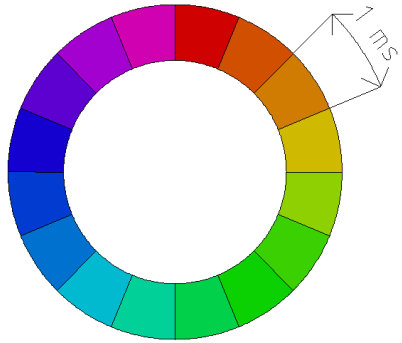
Incoming spikes









Spike incoming (interrupt received)

Retrieving synaptic weights

Synaptic plasticity (STDP)

Adding the new input in the delay buffer

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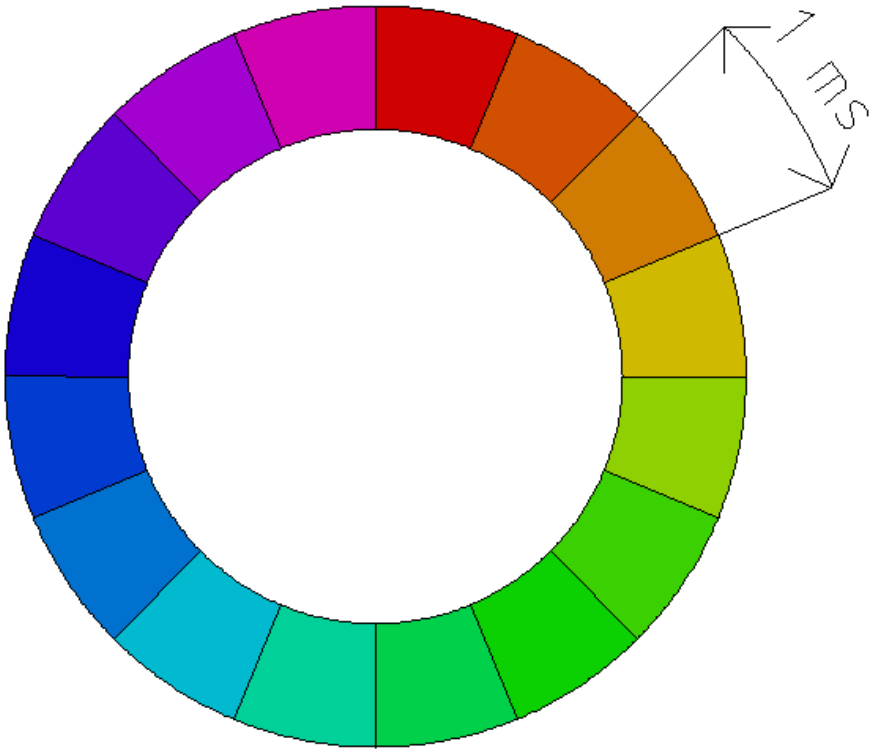
The delay buffer



- 1 millisecond each slot (a.k.a. bin);
- 16 slots for a maximum delay of 16 millisecond;
- Incoming spikes adds synaptic weights in the correspondent slot;

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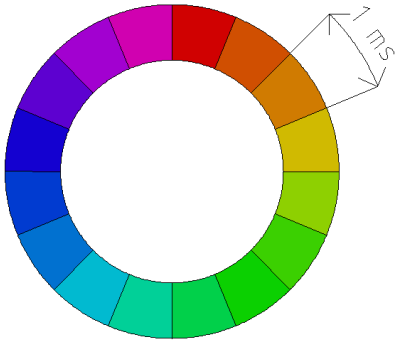
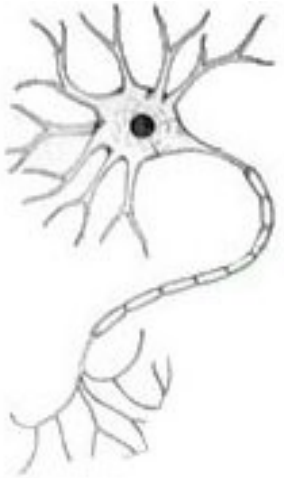
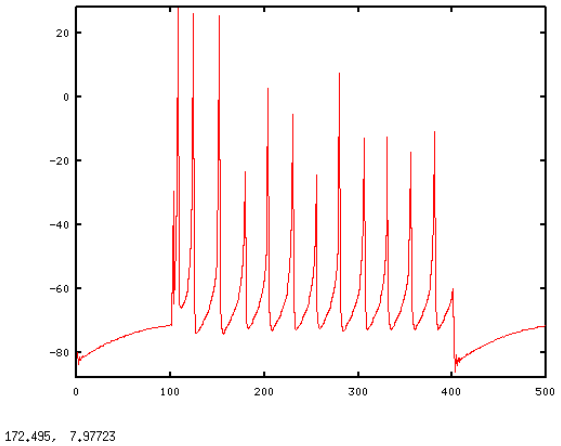
Neural simulation







Timer interrupt

Neuron input

Differential equation computation

Spike emission

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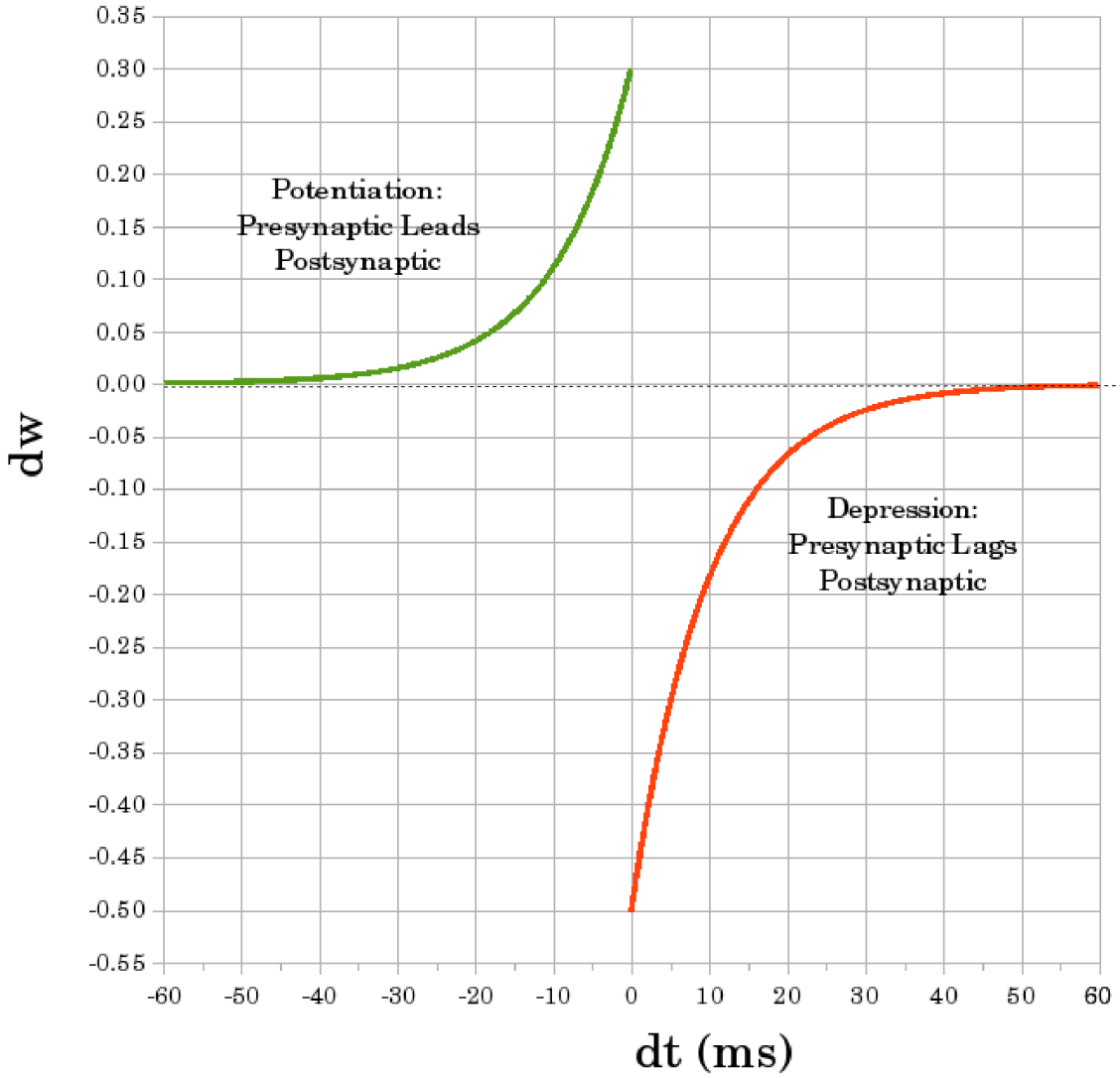
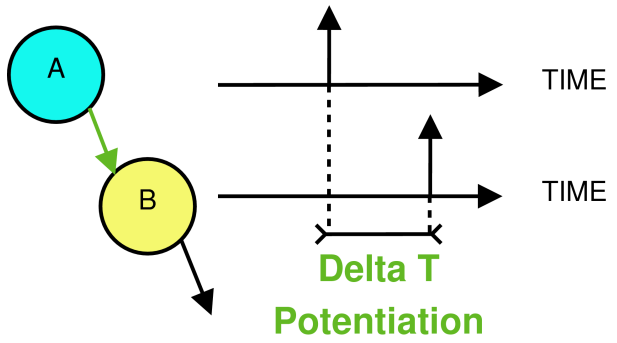
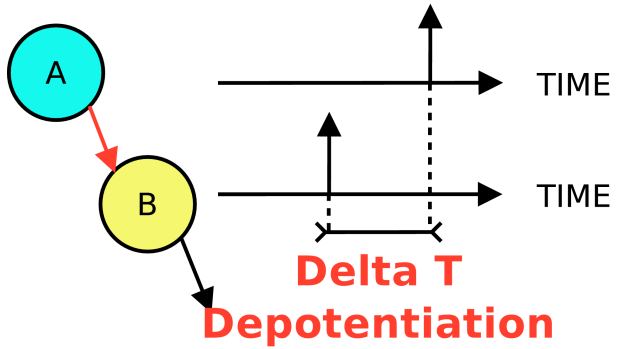
Spike Timing Dependent Plasticity







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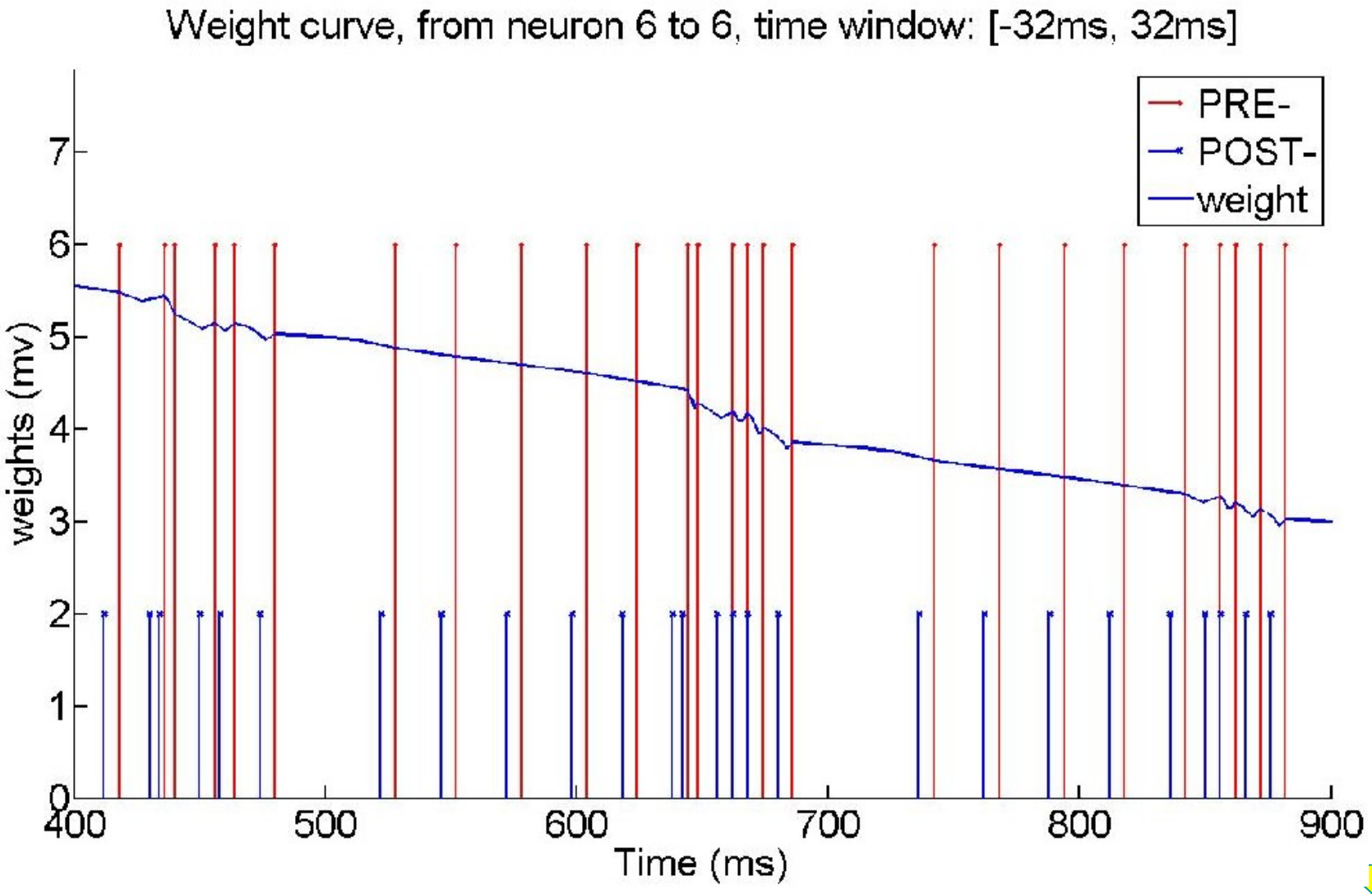
LTD - example



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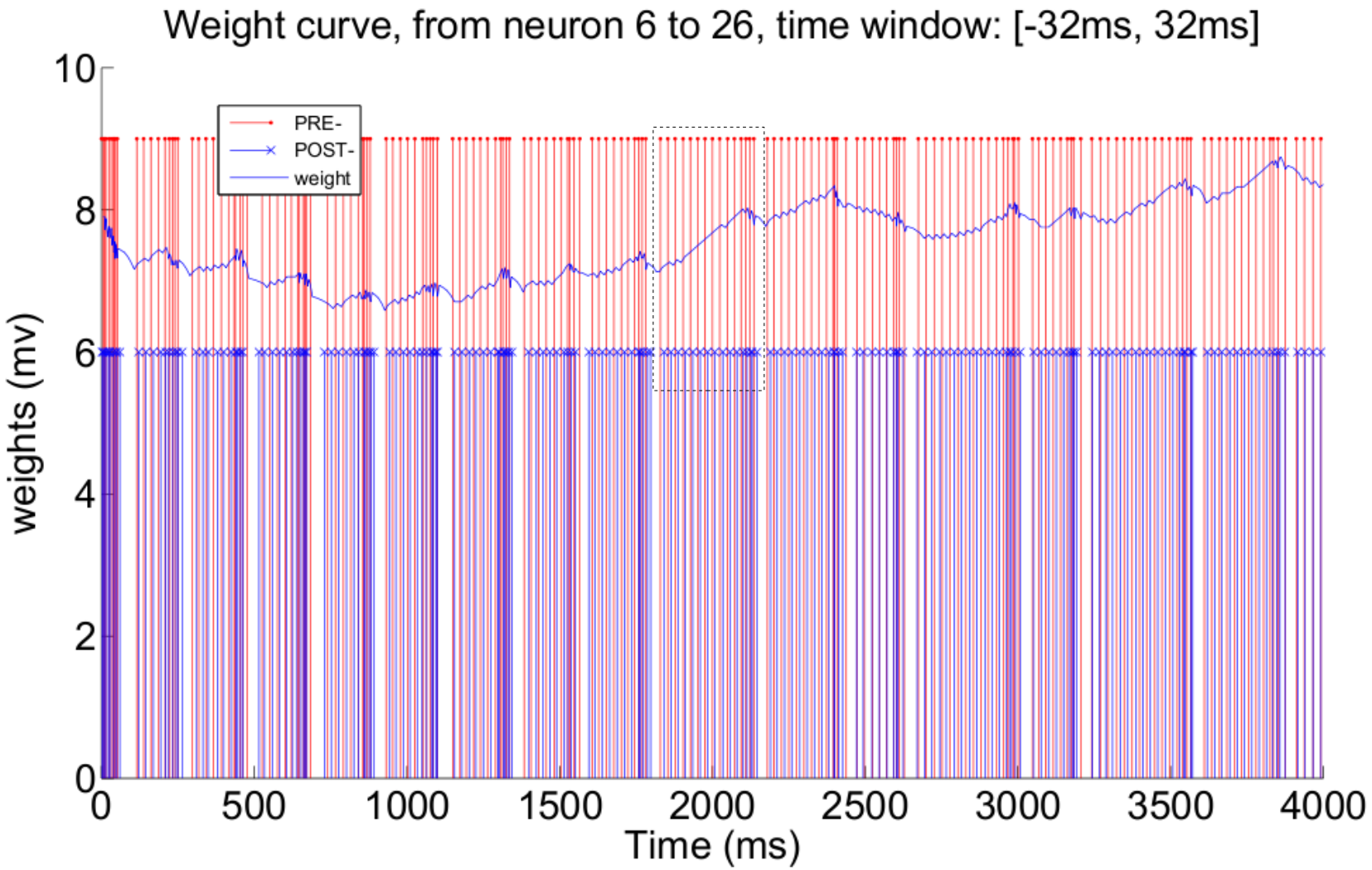
LTP - example



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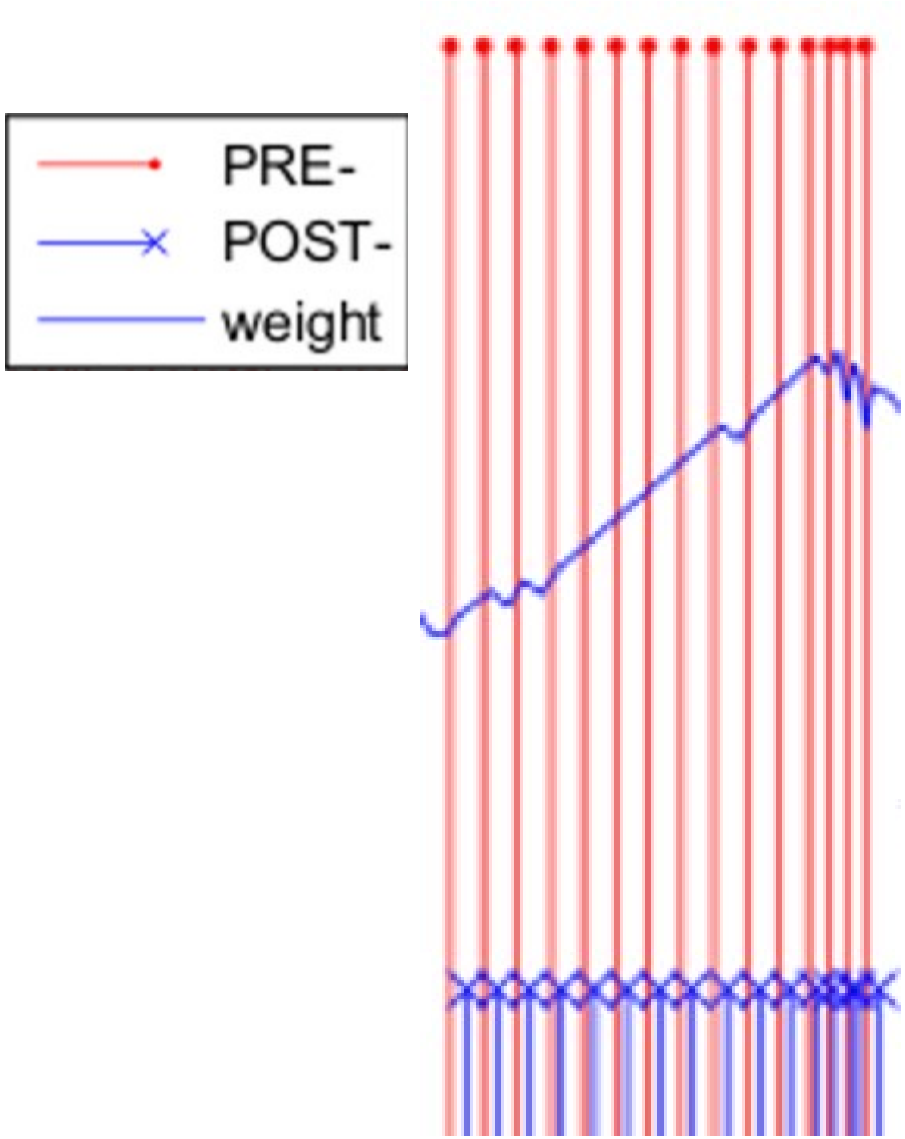
LTP – example – details

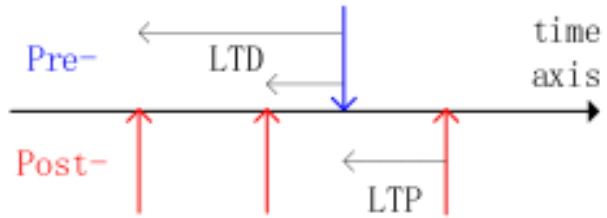


- Each sequence of pre-post synaptic spike generates an increase in the synaptic weight.
- When the pre-synaptic and the post-synaptic spikes are too close, the weight starts to oscillate rapidly

Implementation

Triggering the STDP algorithm

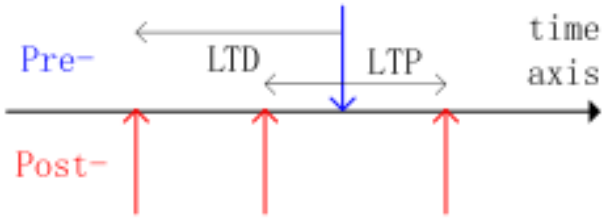
The usual way:



STDP is triggered on:

- Pre-synaptic spike arrival (LTD)
- Post-synaptic spike emission (LTP)

The SpiNNaker way:



- STDP is triggered only on pre-synaptic spike arrival (LTD and LTP)
- Weights are available only at pre-synaptic spike arrival.
- Since LTP needs future information, the algorithm needs to be deferred until the time window is filled

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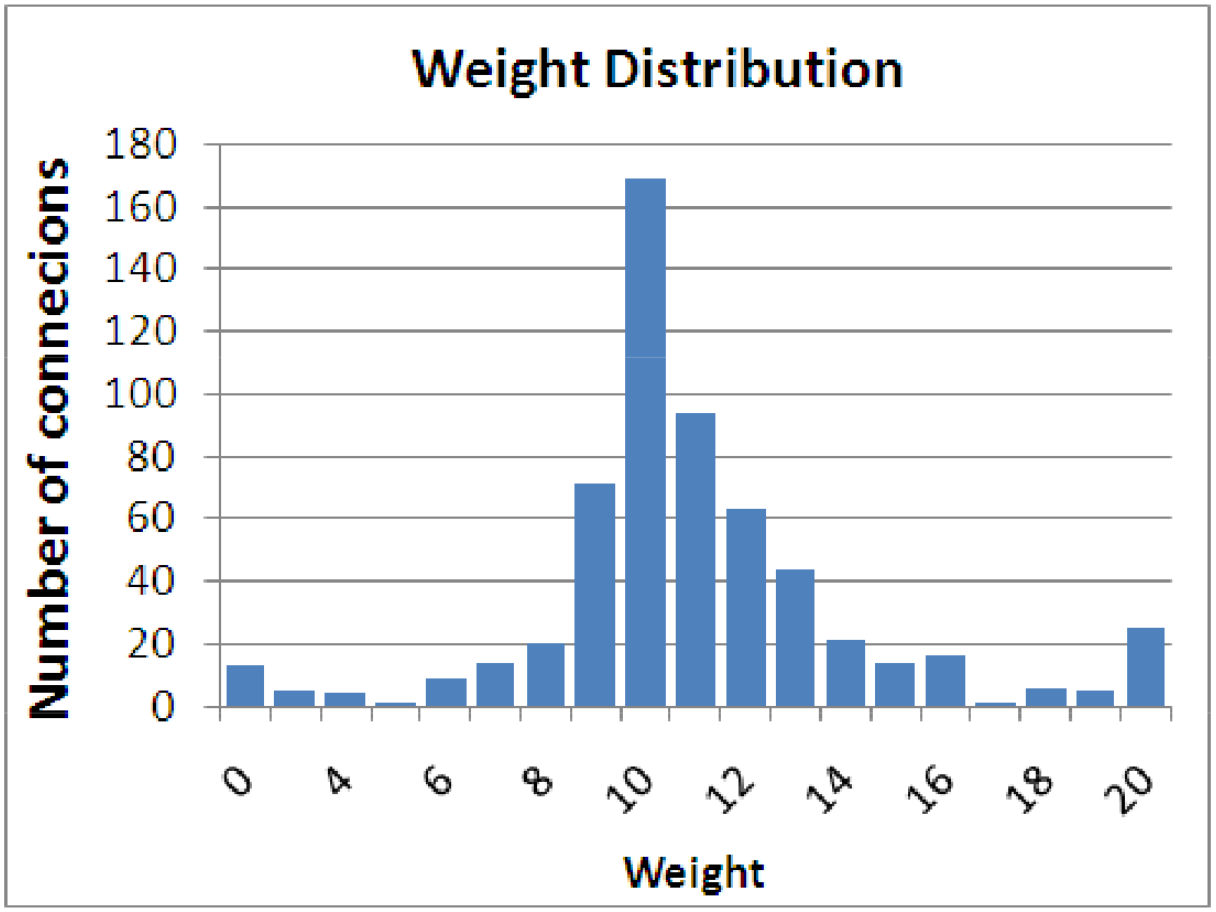
Network parameters

- Number of neurons: 76 – 60 excitatory, 16 inhibitory
- Type of neuron: Izhikevich model – exc: TS, inh: FS
- Simulation time: 30 seconds
- Starting weights: exc weights set at 10, inh set at -8;

(inspired by Izhikevich, “Polichronization”)



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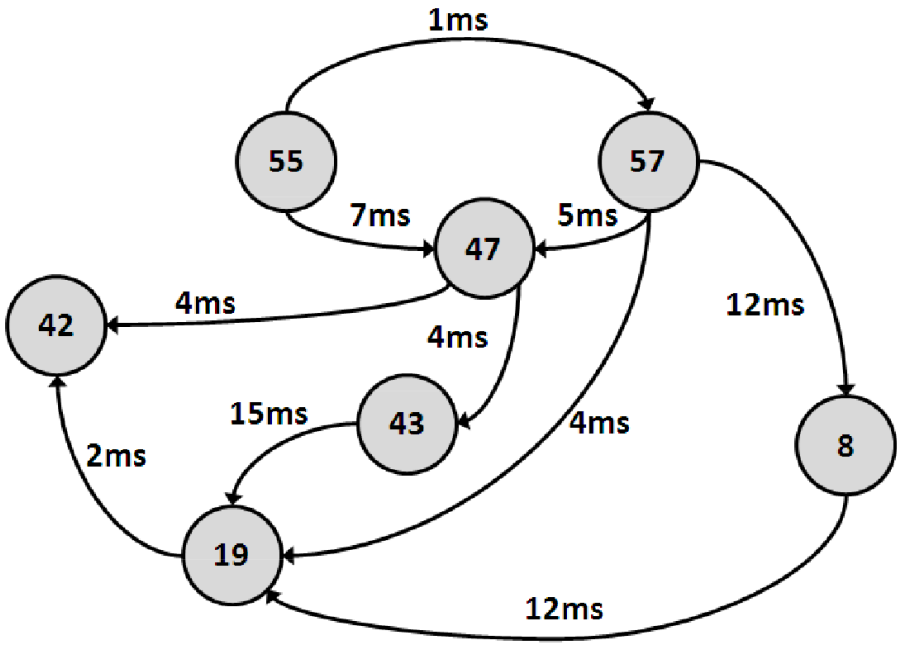
Results

In a simulation we run there were a group of 7 neurons which were strongly interconnected at the end of the simulation



Three circuits with converging delays:

- 57 → 8 → 19 and
  57 → 47 → 43 → 19
- 55 → 57 → 47 and
  55 → 47
- 55 → 57 → 19 → 42 and
  55 → 47 → 42

These connections are systematically reinforced due to the converging delays which makes the neurons fire in a pattern.

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Future work

- Rate – based plasticity
- Propagation delay plasticity
- Homoeostasis
- Rewiring

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Thank you!!!

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Back-up slides

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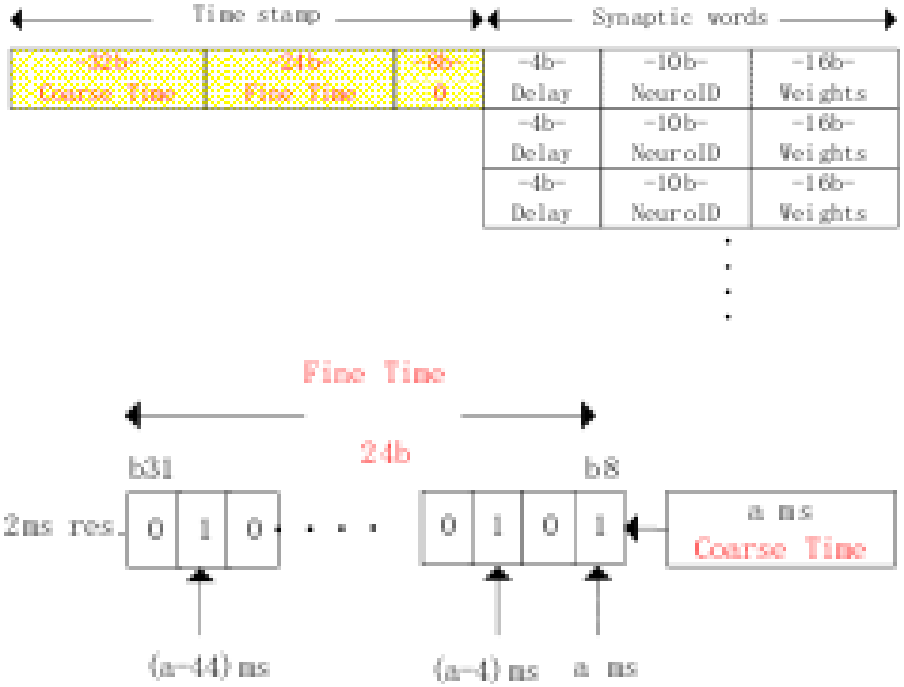
Implementation

Representation of spike timestamp

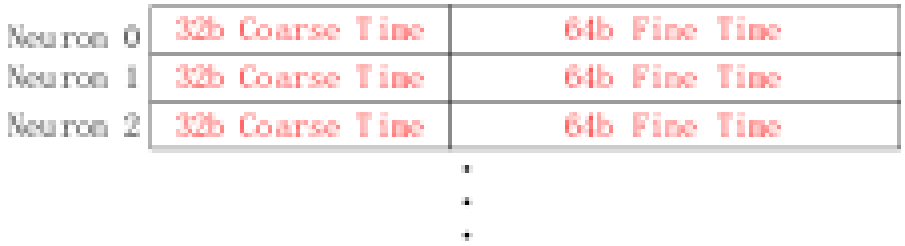
Pre-synaptic timestamp

Needed only when a pre-synaptic spike arrives. Stored as header of the synaptic weight block



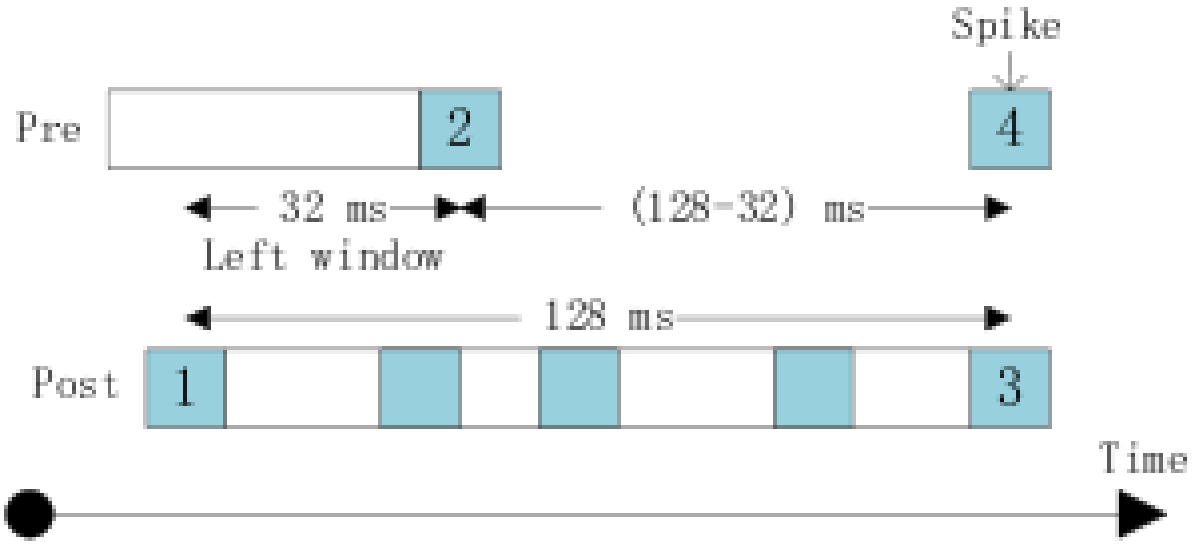
Post-synaptic timestamp

Needed at all time. Stored in processor's local memory



Implementation

Length of timing records



The STDP is triggered when an incoming spike pushes an old input record into the carry bit
However, if the input arrives at very low rate the output generated pushes forward the previous records and the history will be lost.