

Maintaining Real-Time on SpiNNaker

Sergio Davies, Alexander Rast, Francesco Galluppi
and Steve Furber

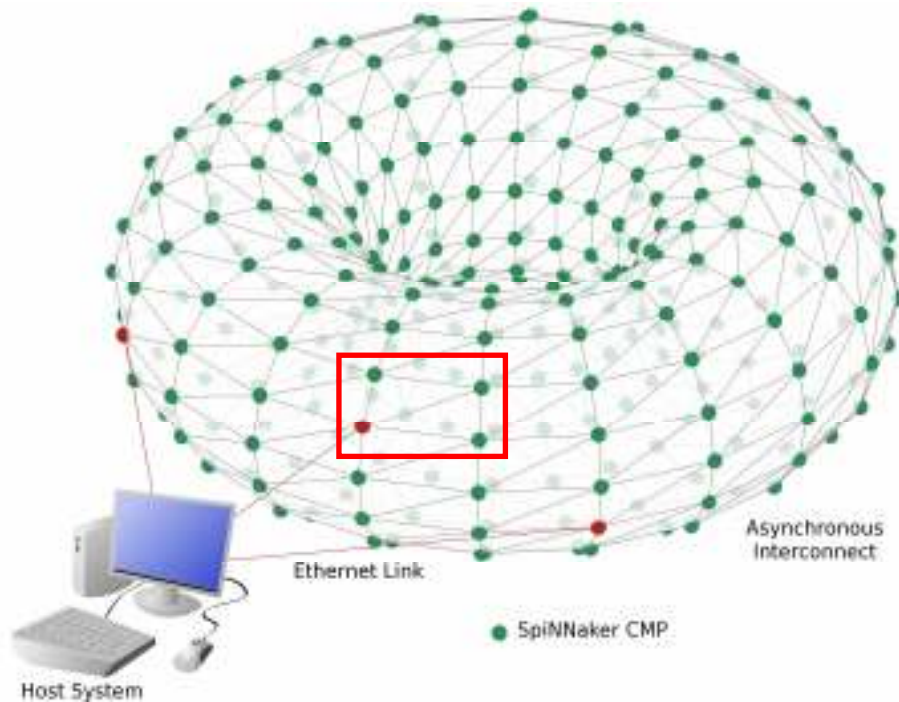
APT group
The University of Manchester



Overview of the topics

- The SpiNNaker system
- Neural network simulations
- Simulation timing

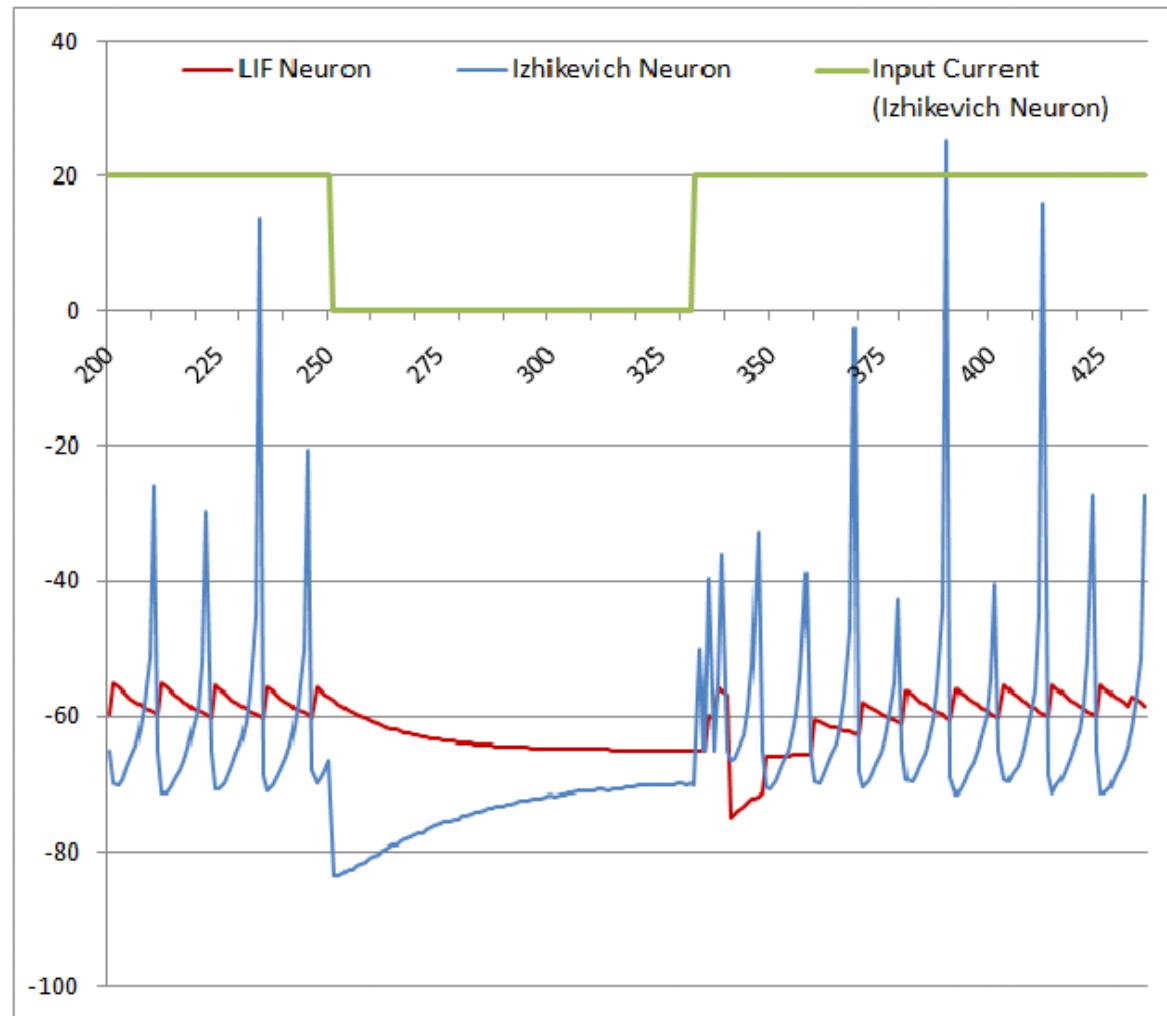
The SpiNNaker system



Biologically-inspired spiking neural network simulator:

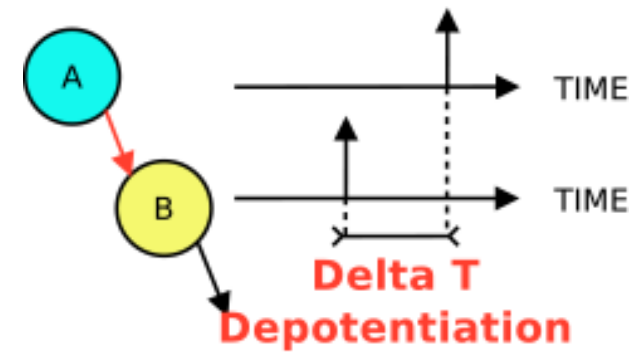
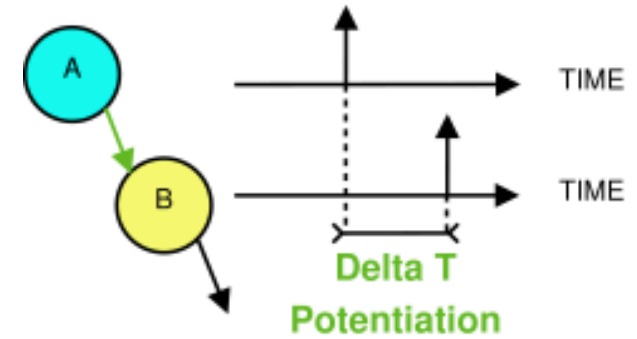
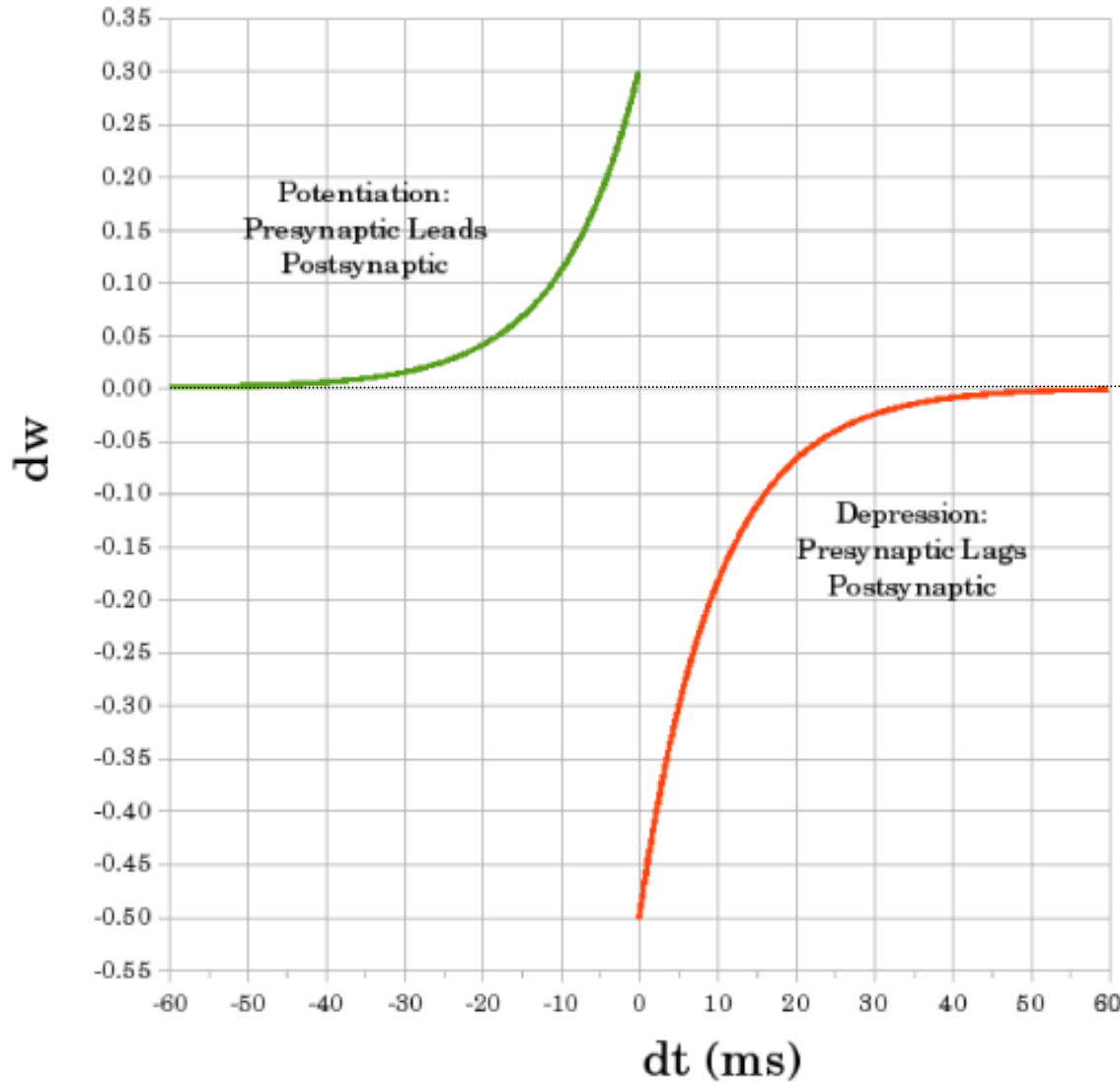
- Off-the-shelf cores (multiple ARM9 per chip) with custom interconnect devices (asynchronous);
- Aims to simulate 1 billion+ neurons in real-time (~1% brain's neuron count).

Neural network simulation

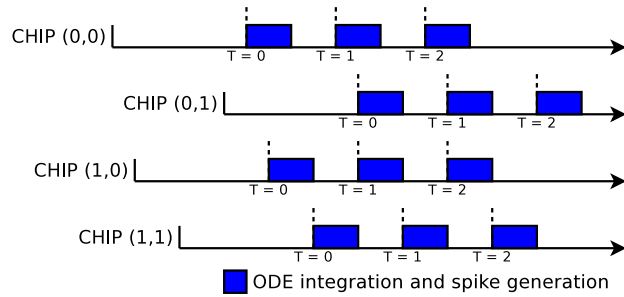


- Multiple neuron types during one simulation;
- Multiple synapse types during one simulation;

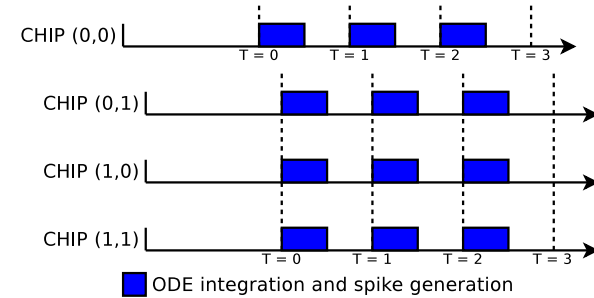
Learning (STDP)



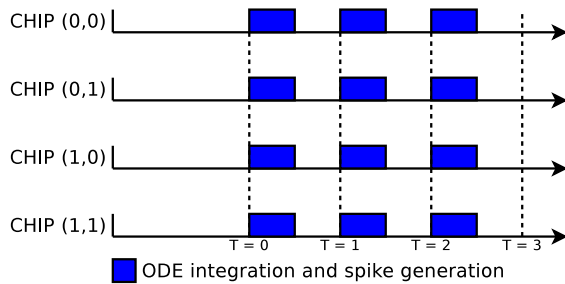
Simulation timing



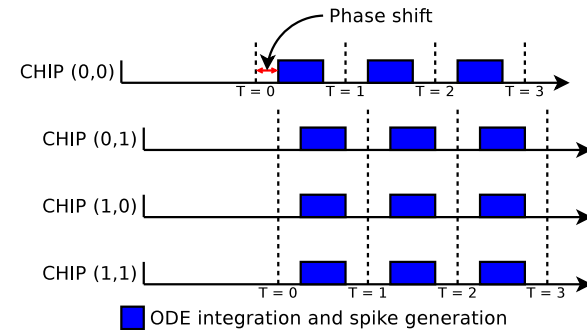
Simulation without synchronization across chips



Real simulation timing (with a barrier synchronization)



Simulation perfectly synchronized across multiple chips



Phase shifting

Conclusions

Features of SpiNNaker:

- Simulates very large networks
- Real-time
- Multiple neuron types
- Multiple synapse types
- Learning



Thank you!!!

Questions???

Maintaining Real-Time Synchrony on SpiNNaker
Sergio Davies, Alexander Rast, Francesco Galluppi, and Steve Furber

SpiNNaker system details

SpiNNaker

(Analog) neuromorphic integrated circuit (based on the industrial factories of the latest tools)

- 48,000 SpiNNaker chips
- Each chip contains 38 ARM cores each simulating ~1,000 neurons (8 ARM cores in the core chip)
- Total: 1 billion+ neurons
- SpiNNaker system is able to simulate ~1% of the brain.

Synchronization details

Barrier synchronization

• A theoretical synchronization procedure (for multi-processor simulation)

Simulation timing

• Evolution of the simulation on multiple chips

- Examples of simulation running on the SpiNNaker system with the slight de-synchronization.

Features of SpiNNaker chip

SpiNNaker mimics the brain in numerous ways:

- Resilient to individual component failure;
- Modular processing elements;
- Asynchronous event based communication;
- Multiple functional blocks with small elements.

Neural simulation

- Ability to simulate one neuron trace per core
- Neuron traces can be different across multiple cores in the system during the same simulation.

Test board schematic

- Each green dot represents an external connection

Phase shifting

- Phase shifting technique to solve the de-synchronization problem;
- Available computation time reduced by this technique;
- The neural simulation is memory bounded but CPU bounded, so this does not influence the amount of neurons that each core can simulate.

Further Information

Get more info at: <http://www.spiNNaker.org> or sergio.davies@man.ac.uk

Sergio Davies' website: <http://www.spiNNaker.org> or sergio.davies@man.ac.uk

Sergio is supported by a PhD scholarship funded by EPS Research Council

Developed by:
APT Group,
The University of Manchester

SpiNNaker sponsors and collaborators:
EPSRC, ARM, MANCHESTER

The SpiNNaker project is supported by EPSRC through the grant EP/H05746/1

Sergio is supported by a PhD scholarship funded by EPS Research Council

Please, come near the poster!!!

