tors whose input sources are the gate voltages of M5 and M6, V_A and V_B, respectively. Therefore, in steady-state conditions the voltages across capacitors C_3 and C_4 are equal to V_A and V_B, respectively, and the input voltage is forced to ground (which is set to half the supply voltage to achieve a symmetric biasing). Current I_Q is hence set by currents I_{B1} and I_{B2} and the aspect ratios of M1-M2 and M5-M6. To reduce charge injection errors, capacitors $C_{3,4}$ are set larger than $C_{1,2}$.

The circuit can be operated with any supply voltage higher than the minimum requirement, but for low-power supplies a clock booster must be used to properly drive the switches [5].

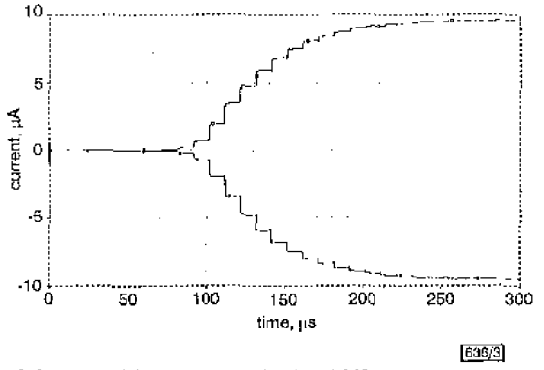

Fig. 3 *Start-up of drain currents of M1 and M2*

◇ i_{d1} (M1)
□ i_{d1} (M2)

Table 1: Main design parameters

Component	Value
M1 M3 M5	50/2μm/μm
M2 M4 M6	20/2μm/μm
I_{B1} I_{B2}	10μA
C_1 C_2	0.5pF
C_3 C_4	1pF
V_{DD}-V_{SS}	1.2V

Simulations: The circuit in Fig. 2 was simulated using SPICE and the process parameters of a standard 0.8μm CMOS technology. Since the transistor threshold voltages are ~0.8V, a 1.2V power supply was chosen. Transistor dimensions and other electrical parameters are given in Table 1. Minimum dimensions were adopted for the transistors implementing the switches. Moreover, *n*-channel transistors were used for S1-S4 and *p*-channel transistors for S5-S6. The clock period was set to 10μs. Since switches S3-S4 both need a clock booster, a 2.4V clock (i.e. twice the power supply) was adopted to drive these two switches. Finally, parasitic capacitances associated with the top and bottom plate of capacitors C_1–C_4 were taken into account and set to 1 and 10% of their respective capacitor values.

Fig. 3 shows the start-up time interval needed by the quiescent currents of input transistors M1-M2 to reach a steady-state condition. Both currents are nearly zero until around 80μs since transistors M1-M2 are working in the subthreshold region. Once the threshold voltage is reached, the module of currents increases until the desired bias current (10μA) is attained. The simulated quiescent current is 9.56μA, which is reached in ~250μs. Of course, this start-up time can be reduced by reducing the time constant of the damped integrators.

With the chosen supply voltage, the analogue ground is equal to 0.6V. This value is accurately transferred to the input terminal with an error lower than 0.1mV.

8 December 1999
Electronics Letters Online No: 20000120
DOI: 10.1049/el:20000120

G. Palmisano and S. Pennisi (*Dipartimento Elettrico Elettronico e Sistemistico, Università di Catania, Viale Andrea Doria 6, I-95125 Catania, Italy*)

E-mail: gpalmisano@dees.unict.it

References

1 TOUMAZOU, C., LIDGEY, F., and HAIGH, D. (Eds.): 'Analogue IC design: the current-mode approach' (Peter Peregrinus, 1990)
2 TOUMAZOU, C., HUGHES, J.B., and BATTERSBY, N.C. (Eds.): 'Switched-currents: an analogue technique for digital technology' (Peter Peregrinus, 1993)
3 PALUMBO, G., and PENNISI, S.: 'Low voltage class AB CMOS current output stage', *Electron. Lett.*, 1999, **35**, (16), pp. 1329–1330
4 PALMISANO, G., PALUMBO, G., and PENNISI, S.: 'CMOS current amplifiers' (Kluwer Academic Publishers, 1999)
5 PALMISANO, G., and PALUMBO, G.: 'Clock boosters for 1.2-V SC circuits'. IEEE ISCAS'97, Hong Kong, June 1997, pp. 2012–2015

Power reduction in self-timed circuits using early-open latch controllers

P.A. Riocreux, M.J.G. Lewis and L.E.M. Brackenbury

An early-open latch controller for use in self-timed micropipeline circuits is described. It switches into normally-open mode shortly before the arrival of the data, preventing energy dissipation due to data propagation down the pipe, but preserves the speed advantage of a normally-open latch controller. This is confirmed by comparing the throughput and power for a large circuit with those obtained using other latch controllers.

Latch controller styles: Micropipelines [1] represent a practical engineering approach to implementing pipelined asynchronous systems. Fig. 1 shows a typical micropipeline arrangement with the transfer of data between adjacent stages controlled by local request and acknowledge handshake signals.

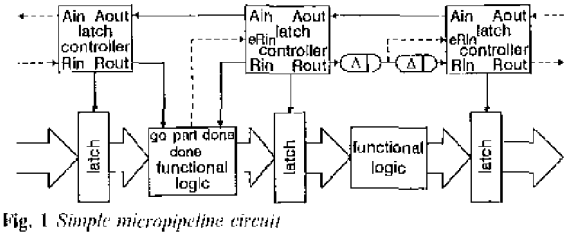

Fig. 1 *Simple micropipeline circuit*

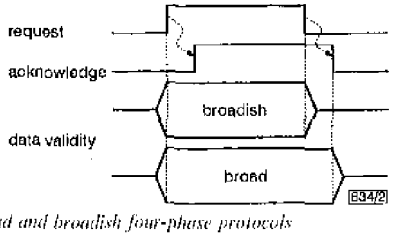

Fig. 2 *Broad and broadish four-phase protocols*

Four-phase control signals with a broad or broadish protocol (Fig. 2) are usually adopted because this facilitates the enabling of processing logic by *Rin* [2]. In the broad protocol, data must remain valid until the back edge of the *Acknowledge* signal whereas it is only to the back edge of the *Request* signal in the broadish protocol.

Latches operate in either normally-open (NO) or normally-closed (NC) mode. An NO latch is normally transparent with the latch closing to capture new data when it arrives. An NC latch is normally closed and briefly opens when new data arrive to pass these data to its output.

When pipeline occupancy is high, it is desirable to operate the latches in NO mode so that data propagate down the pipe at the maximum rate. However, during lower occupancy, high throughput is not necessary and the NC mode is desirable to reduce unnecessary power dissipation from data propagating through unoccupied stages.

Controlling latch operating mode: For these reasons, latch controllers capable of reconfiguring the latch mode were developed [3]. These used an additional signal to switch the latches between the NO and NC mode depending on the pipeline load. To detect when the operating mode should change required a significant software or hardware overhead; the early-open latch controller described here overcomes this.

A schematic diagram for the early-open latch using the broad protocol is shown in Fig. 3. The logic for the broadish protocol is similar except that the latch enable, *En*, is only held low (closed) by the output stage while *Request Out* is high.

The latch operates in NC mode and uses an additional signal, '*earlyRin*' which gives advanced notice of an impending input request; it can be derived from the *Request Out* signal of the preceding block as shown by the dashed lines in Fig. 1. The '*earlyRin*' signal is used to switch the data latches into NO mode. This scheme has the virtues of both high performance and low power dissipation. Opening the latches just prior to the arrival of the *Request In* signal allows the input to propagate to the latch output as fast as possible while normally operating in NC mode prevents unwanted data propagating beyond the input to the first pipeline stage.

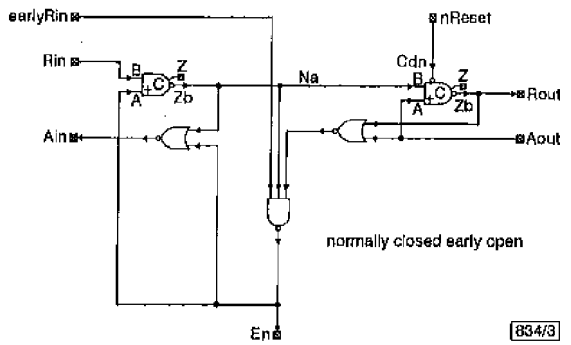

Fig. 3 *Broad protocol early-open latch controller*

Results: The early-open latch controller circuit was tested against the existing reconfigurable normally-open (RNO), reconfigurable normally-closed (RNC) and conventional NO latch controllers in a 31k-transistor design consisting of a 32 × 32 bit five-stage pipelined multiplier [4]. Simulations were performed on the full extracted layout, with TimeMill and PowerMill used to measure throughput and power.

(i) *Throughput*: Random data were used for the throughput tests, as the performance is not data-dependent. Table 1 shows the results of these tests.

Table 1: Throughput performance (in MOPS)

	NO	RNO	RNC	Early-open
Broad	101	97	90	95
Broadish	106	106	98	106

For the broadish protocol, the early-open latch has a performance comparable to that of any other latch style while for the broad protocol, it has a slightly inferior performance. This is due to the slightly increased complexity of the critical path in the latch controller circuit. With the broadish protocol, the latches can begin to reset before the output *Acknowledge* has completed, so this penalty disappears.

(ii) *Power consumption*: Here, measurements on different levels of pipeline occupancy and also input skew were performed. The results with the inputs coincident are shown in Fig. 4. As is to be expected, the energy consumption per operation for high occupancy levels is similar for all controller styles, since the propagation of spurious transitions is restricted. At low occupancy, the early-open design exhibits near minimum energy per operation for both protocols; at an occupancy of one, its power is comparable to that of an RNC controller and is 22–25% better than that of the other NO controller types demonstrating the advantage of only opening the latches just prior to the arrival of data.

Tests with the inputs skewed show that the power per operation rises slightly for the early-open and both NO designs while remaining approximately constant for the NC latch design. This increase in the early-open implementation can be attributed to not being able to use early-open latches in the first stage; NO latches had to be used here so transitions can propagate to the second latch before being stopped.

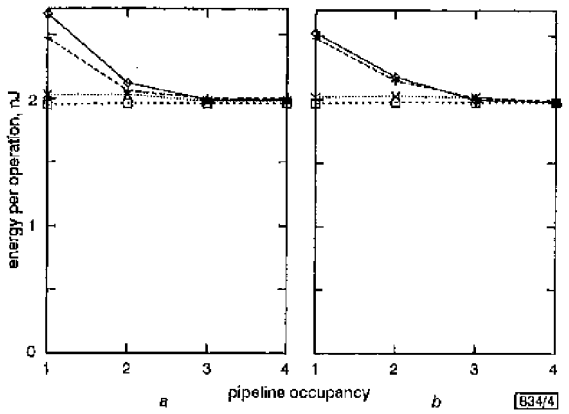

Fig. 4 *Power for different latch controllers*

a Broad protocol
b Broadish protocol
—◇— normally open
– – □ – – reconfigurable (N-C)
– · + · – reconfigurable (N-O)
····×···· early-open

Conclusions: A high performance, low power early-open latch controller for use in asynchronous pipeline systems has been described and compared with other controller types. Its maximum throughput is comparable to that of the fastest control style. At high pipeline occupancies, the power per operation of all controller styles is comparable. However, at the lowest occupancy it exhibits ~25% less power per operation than that of the other high performance latch controllers. The latch therefore can be used to best advantage when the pipeline load is variable.

Acknowledgment: The authors express their thanks for support from the EPSRC/MoD Powerpack project GR/L27930.

13 October 1999
Electronics Letters Online No: 20000178
DOI: 10.1049/el:20000178

P.A. Riocreux, M.J.G. Lewis and L.E.M. Brackenbury (*Amulet Group, Computer Science Department, University of Manchester, Oxford Road, Manchester, M13 9PL, United Kingdom*)

References

1 SUTHERLAND, I.E.: 'Micropipelines', *Commun. ACM*, 1989, **32**, (6), pp. 720–738
2 FURBER, S.B., and DAY, P.: 'Four-phase micropipeline latch control circuits', *IEEE Trans. VLSI Syst.*, 1996, **4**, (2), pp. 247–253
3 LEWIS, M., GARSIDE, J.D., and BRACKENBURY, L.: 'Reconfigurable latch controllers for low power asynchronous circuits', Proc. Async'99, April 1999, (IEEE Computer Society Press), pp. 27–35
4 LIU, J.: 'Arithmetic and control components for an asynchronous microprocessor'. PhD thesis, University of Manchester, 1997

Simple model for positive-feedback adiabatic logic power consumption estimation

A. Blotti, S. Di Pascoli and R. Saletti

A model based on constant R-C elements for the calculation of the energy dissipated in adiabatic circuits with positive feedback is presented. The model can be used to estimate the energy dissipated as a function of both the load capacitance and operating frequency with an error of < 8 and 18%, respectively.