# Learning in a Biologically Inspired Massively Parallel Architecture

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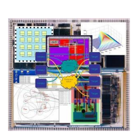
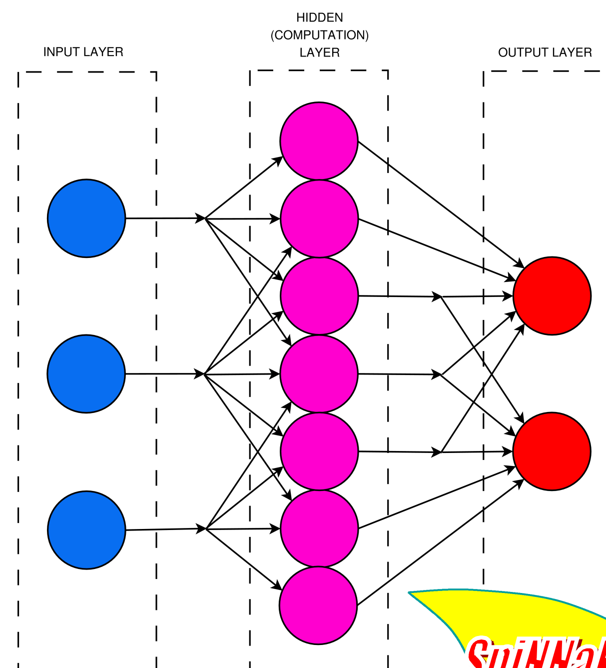


# Neural networks

- **Neural networks** are circuits of biological (or biologically-inspired) neurons;

- **Biological neural networks** are circuits formed by biological neurons connected to carry out functionalities typical of the nervous system;

- **Artificial neural networks** are circuits formed by artificial neurons which mimic the behaviour of biological neurons.



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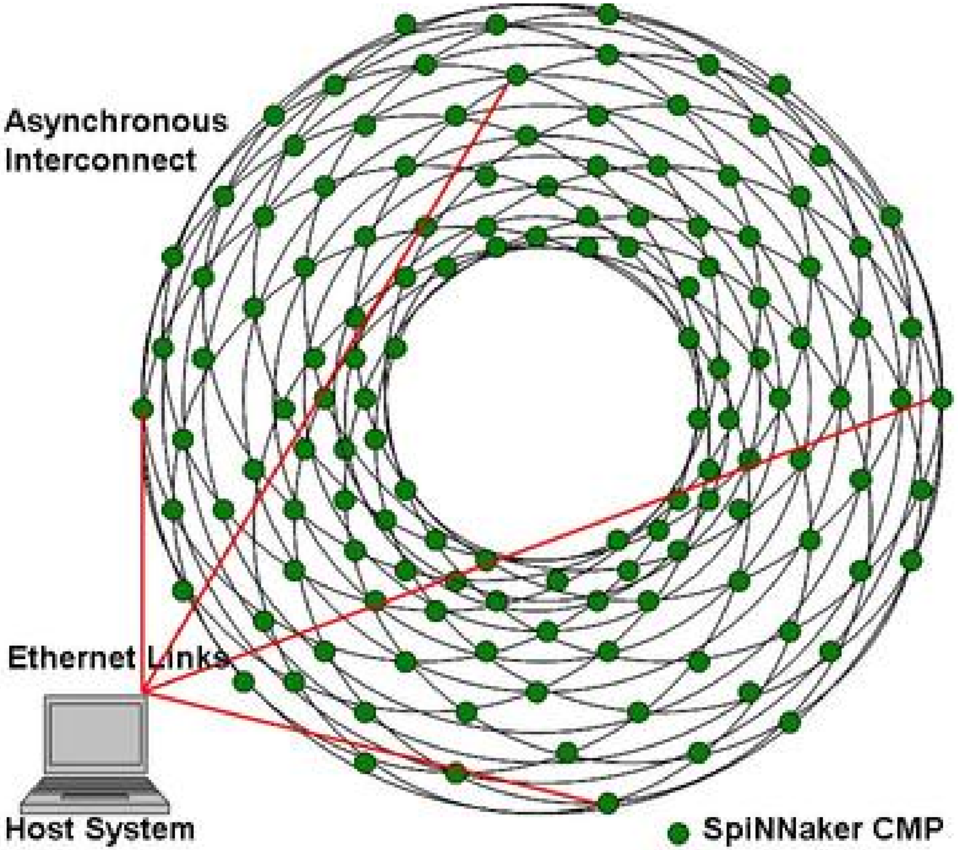
# The SpiNNaker simulator

- SpiNNaker is a platform for modelling and simulate artificial spiking neural networks in real-time.

- Each node of the system is an ASIC chip with multiple ARM cores




SpiNNaker a universal Spiking Neural Network architecture

# Learning in biological neural networks

The basis of learning in biological neural networks resides in Hebb's postulate:

- "*The general idea is an old one, that any two cells or systems of cells that are repeatedly active at the same time will tend to become 'associated', so that activity in one facilitates activity in the other*"

Hebb, D.o. (1949), "The organization of behaviour", New York: Wiley, p.70.

# Learning in artificial neural networks

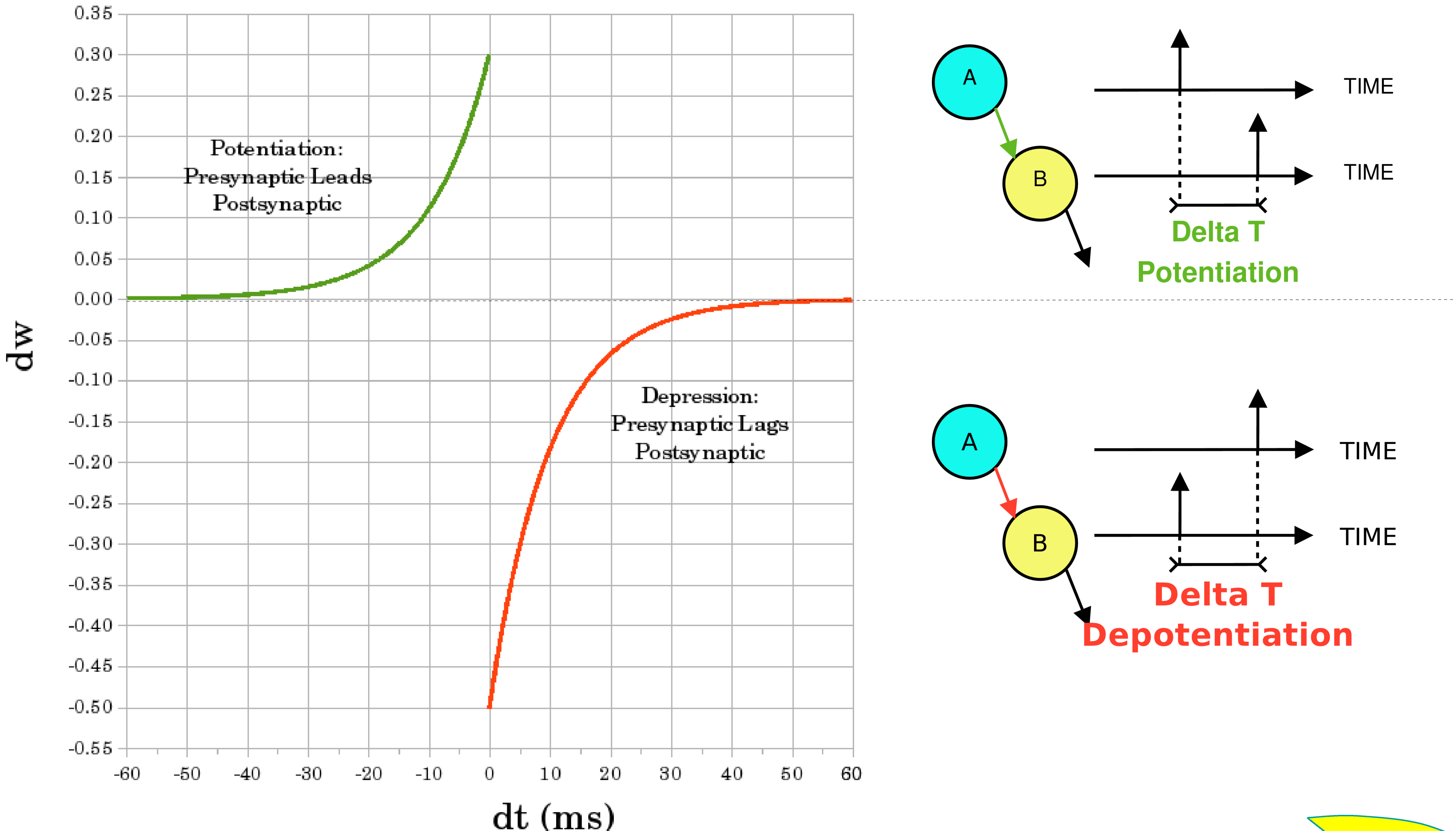
Three major learning paradigms:

- Supervised learning;
  *(known input – known output)*

- Unsupervised learning;
  *(known input – unknown output)*

- Reinforcement learning;
  *(unknown input – unknown output)*

# Spike Timing Dependent Plasticity



# Statement of the problem

From biology we learn that neural cells start to form connections between each other shaping the nervous system since the beginning of a new life.

During the development, some of the connections get weak and disappear, while new connections develop and evolve.

The purpose of this research is to develop these functionalities (a.k.a. synaptic rewiring) in the SpiNNaker simulator.

# Research objectives

To develop a software simulator which includes features of synaptic plasticity:

- Synaptic weight modification;
- Creation of new interconnections between neurons;
- Deletion of interconnections with very weak synaptic weights.

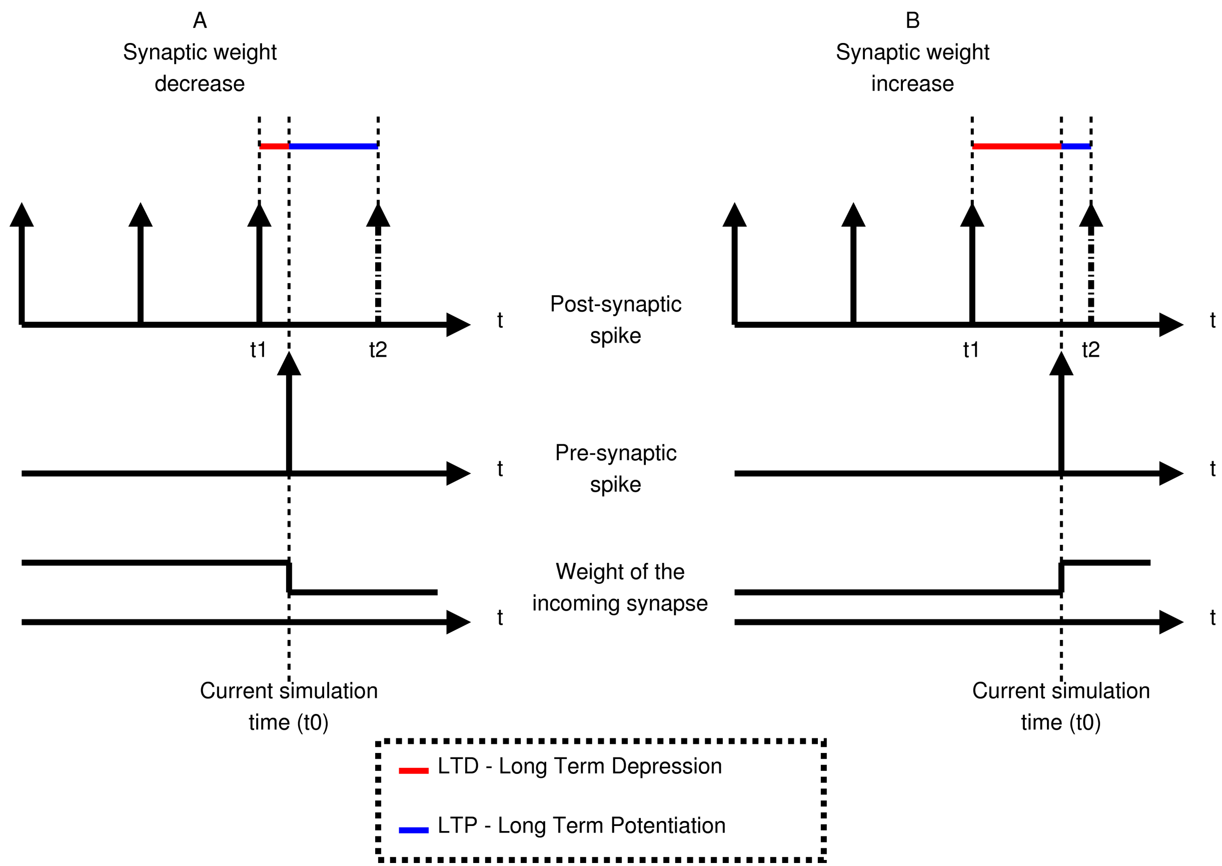
# Methodology

Research project divided in three steps:

- Definition and implementation of a synaptic weight modification algorithm;
- Definition and implementation of a dynamic routing algorithm;
- Definition and implementation of a synaptic rewiring algorithm (based on the previous two steps).

# Synaptic weight modification algorithm

## “Rolling average” STDP algorithm

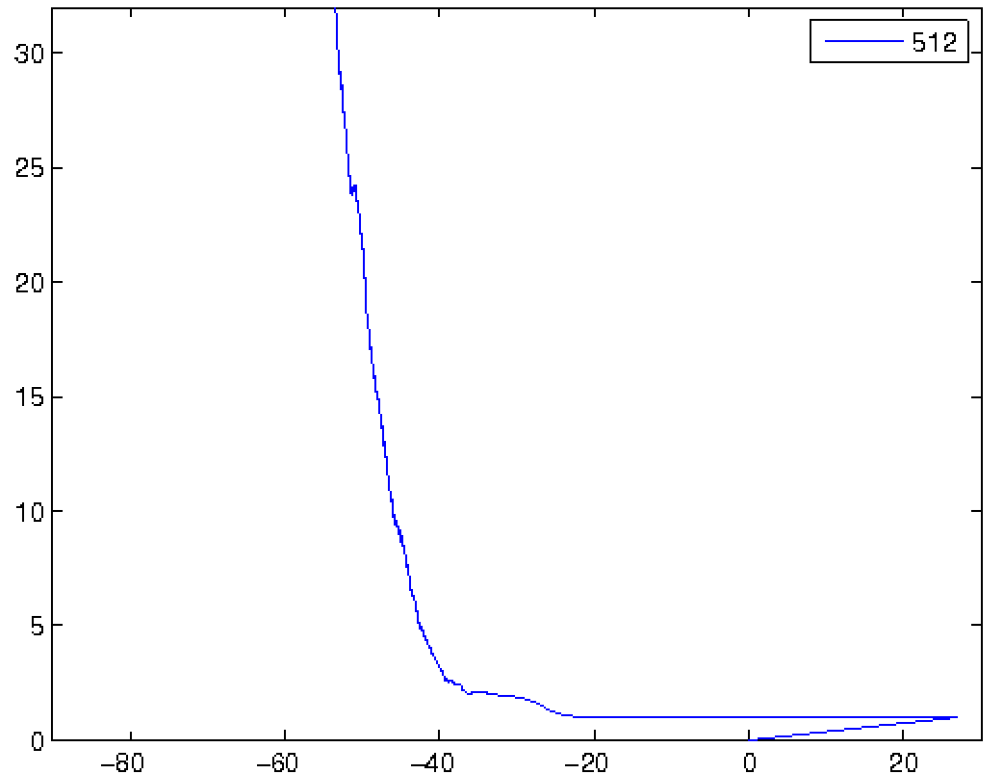


# Synaptic weight modification algorithm

Using the membrane potential as proxy for the spike emission

X axis:
Membrane potential (mV)

Y axis:
Time-to-spike (ms)



# Publications

[1]X. Jin, A. Rast, F. Galluppi, S. Davies, and S. Furber, ``Implementing Spike-Timing-Dependent Plasticity on SpiNNaker neuromorphic hardware''. Neural Networks, 2010. IJCNN 2010. I presented this paper at IJCNN 2010 in Barcelona from July 18th to 23rd.

[2]X. Jin, F. Galluppi, C. Patterson, A. Rast, S. Davies, S. Temple, and S. Furber, ``Algorithm and software for simulation of spiking neural networks on the multi-chip SpiNNaker system''. Neural Networks, 2010. IJCNN 2010.

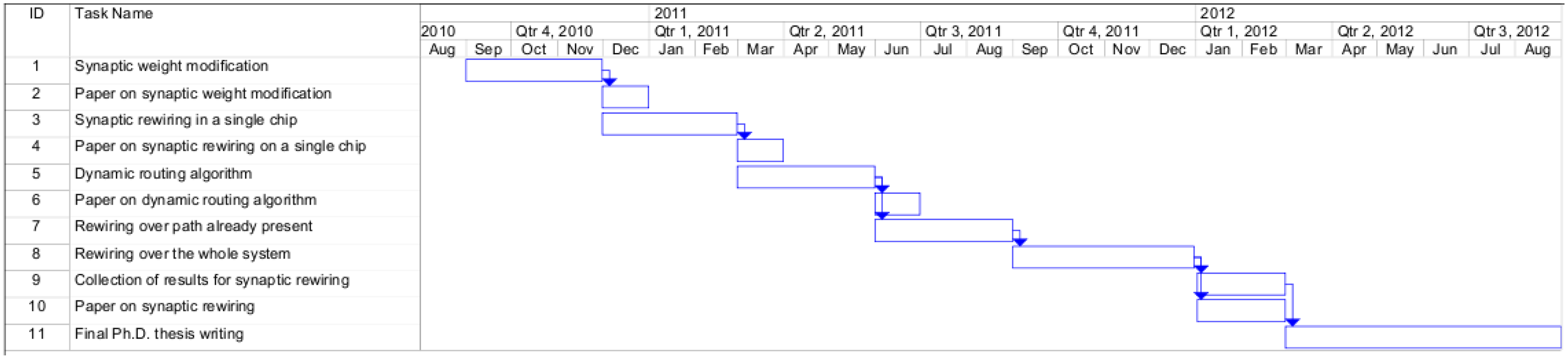
[3]X. Jin, M. Lujan, L. A. Plana, S. Davies, S. Temple, and S. Furber, ``Modelling of spiking neural networks on SpiNNaker''. Computing in Science and Engineering, September/October 2010.

[4]F. Galluppi, A. Rast, S. Davies, and S. Furber, ``A general-purpose model translation system for a universal neural chip''. ICONIP 2010 (Accepted – September 2010).

[5]S. Davies, C. Patterson, F. Galluppi, A. D. Rast, D. Lester and S. B. Furber, ``Interfacing Real-Time Spiking I/O with the SpiNNaker neuromimetic architecture''. ICONIP 2010 (Accepted – September 2010).

[6]A. Rast, F. Galluppi, S. Davies, L. Plana, C. Patterson, T. Sharp, S. Furber, "Concurrent Heterogeneous Neural Model Simulation on a Neuromimetic System", SUBMISSION PENDING - ICONIP, August 2010

# Time plan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Qtr 2, 2012
Qtr 3, 2012
Aug Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug Sep Oct Nov Dec Jan Feb Mar Apr May Jun Jul Aug
1 Synaptic weight modification
2 Paper on synaptic weight modification
3 Synaptic rewiring in a single chip
4 Paper on synaptic rewiring on a single chip
5 Dynamic routing algorithm
6 Paper on dynamic routing algorithm
7 Rewiring over path already present
8 Rewiring over the whole system
9 Collection of results for synaptic rewiring
10 Paper on synaptic rewiring
11 Final Ph.D. thesis writing

# Thank you!!!

# Synaptic weight modification algorithm

## "Rolling average" STDP algorithm

Estimated firing rate computed as:

$$FR(n) = \frac{1}{2} FR(n-1) + \frac{1}{2} IST(n)$$

Where:

FR(n): firing rate estimated after n outgoing spikes

IST(n): Inter Spike Time between spike n-1 and spike n