Learning in a Biologically Inspired Massively Parallel Architecture

Sergio Davies
Supervisor: Prof. Stephen B. Furber, Advisor: Dr. Toby Howard

***Abstract*— SpiNNaker is a massively parallel biologically inspired computing platform for modelling artificial neural networks in real-time. Neuron and synaptic models can be modified arbitrarily and standard STDP is one of the models that has been developed in the past years. This article presents a research proposal about implementing synaptic plasticity (synaptic weight modification and synaptic rewiring) in the SpiNNaker system. New models of synaptic weight modification have been tested during this year giving the basis for a new STDP algorithm. An approach to synaptic rewiring is then proposed. This report concludes with a work plan for the remaining two years of the Ph.D. programme and the structure of the final thesis.**

I. Introduction

SpiNNaker is a massively parallel biologically inspired computing platform for modelling artificial neural networks in real-time [10]. The core of this simulator is the SpiNNaker chip [4]: a full-custom ASIC chip with 18 ARM cores (see fig.1), running at 200 MHz. The core is an ARM 968 with low power consumption specifications and extended instruction set for digital signal processing.

In December 2009 a first test chip has been produced as proof-of-concept. The technical specifications of this test chip are lower than the complete chip (e.g.: 2 cores in the test chip vs. 18 cores in the final chip).

The neuron models used in this simulator can be modified arbitrarily. The basic STDP algorithm has been implemented in SpiNNaker with the use of the Deferred Event-Driven (DED) model [9], but the complexity of this algorithm reduces significantly the number of neurons that each chip can simulate in real time.

Publications: during this first year, together with colleagues of my group I contributed in writing several papers:

1) X. Jin, A. Rast, F. Galluppi, S. Davies, and S. Furber, "Implementing Spike-Timing-Dependent Plasticity on SpiNNaker neuromorphic hardware". Neural Networks, 2010. IJCNN 2010. (IEEE World Congress on Computational Intelligence). IEEE International Joint Conference on, 2010 [9]. I presented this paper at IJCNN 2010 in Barcelona from July 18th to 23rd.
2) X. Jin, F. Galluppi, C. Patterson, A. Rast, S. Davies, S. Temple, and S. Furber, "Algorithm and software for simulation of spiking neural networks on the multi-chip SpiNNaker system". Neural Networks, 2010. IJCNN 2010. (IEEE World Congress on Computational Intelligence). IEEE International Joint Conference on, 2010 [7].
3) X. Jin, M. Lujan, L. A. Plana, S. Davies, S. Temple, and S. Furber, "Modelling of spiking neural networks on SpiNNaker". Computing in Science and Engineering, September/October 2010 [8].
4) F. Galluppi, A. Rast, S. Davies, and S. Furber, "A general-purpose model translation system for a universal neural chip". SUBMISSION PENDING - ICONIP, July 2010 [3] [5].
5) S. Davies, C. Patterson, F. Galluppi, A. D. Rast, D. Lester and S. B. Furber, "Interfacing Real-Time Spiking I/O with the SpiNNaker neuromimetic architecture". SUBMISSION PENDING - ICONIP, July 2010 [2].

II. Aims of the research

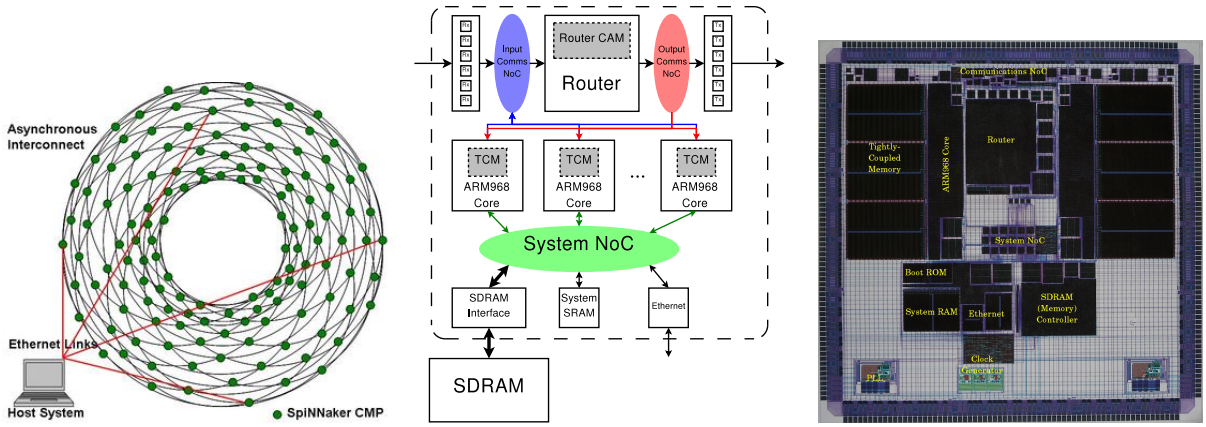
The topic of synaptic plasticity is very common in biological research as the complete mechanism of this process is not yet completely understood. So various hypothesis on this process are being developed by biologists. On the SpiNNaker neuromimetic hardware some of these processes can be implemented to verify the consequences of the hypothesis described by the biologists.

My area of interest is to develop new forms of synaptic plasticity, and in particular the synaptic rewiring. This is the ability of neural network to form new connections between neurons and delete connections which are very weak. This process is believed to be the basis of memory and learning from experience in biological neural networks.

III. Methodology

The steps proposed to carry out the research on the synaptic plasticity are the development of:

1) Synaptic weight modification algorithm. Results in this area are presented later in this report as outcome of the studies done in this first year.
2) Dynamic routing algorithm. To allow the process of synaptic rewiring, the SpiNNaker system must be able to reconfigure the routing tables for multicast packets, so to allow the possibility of connecting a neuron in a new chip or deleting an existent connection. Multicast packets are used to send neural spikes across the whole system.
3) Synaptic rewiring. This task can be divided in three subtasks:
   - Rewiring of new neurons within a chip where a connection is already present (see fig.2a);
   - Rewiring of new neurons within a chip not already reached by the needed connection but within the path followed by relevant multicast packets (see fig.2b);



(a) Structure of the SpiNNaker system

(b) Block diagram of the full SpiNNaker chip

(c) Layout of the SpiNNaker chip

Fig. 1. Diagram of the SpiNNaker chip

- Rewiring of new neurons within a chip not already reached by the needed connection and away from the path followed by relevant multicast packets (see fig.2c);

IV. Results

Two algorithms for synaptic weight modification [11] [6] have been tested during this year: the "rolling average" STDP algorithm and the "voltage based" STDP algorithm [1]. In particular this last one gave interesting results when compared with biological experiments.

The "rolling average" STDP algorithm did not give results close to the standard STDP (used as reference), but it gave the basis for the new algorithm which is currently under development. The idea of this new algorithm is to forecast the spike emission on the basis of the membrane potential (see Fig.3a). This forecast help the computation by replacing the DED model with the statistic forecast of the "time to spike" of a neuron.

This relation is extracted from a neural network simulation (see fig.3a) and then filtered with a sliding window which computes the mean value over the selected interval (see fig.3b).

This allows the simplification of the STDP algorithm implemented [9], leaving some computational power for the synaptic rewiring process.

V. Work plan

The work plan is described by the Gantt Chart in Fig.4, where the tasks described before are detailed with the relevant dates. Additionally, every achievement supported by results is planned to be submitted to relevant conferences and/or journals, so that these will form part of the final Ph.D. thesis.

VI. Thesis structure

A. Chapter 1 – Introduction

Identification of the problem, motivations for approaching it and a relevant literature review about the topic.

B. Chapter 2 – Background of the research

Major knowledge about the environment of the research, with references to the SpiNNaker project.

C. Chapter 3 – Tools developed for the research

Description of the approach to the synaptic rewiring and of the tools developed for this research.

D. Chapter 4 – Results of the tests

Description of the results achieved, with the details about learning in neural networks.

E. Chapter 5 – Discussion

Discussion on the results and why these are relevant for the neural network community (in general) and for the SpiNNaker project (in particular).

F. Chapter 6 – Conclusions and future work

Description of possible future use of the tools developed: application of synaptic plasticity processes described in biology (e.g.: Nerve Growth Factor).

References

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[2] S. Davies, C. Patterson, F. Galluppi, A. D. Rast, D. Lester, and S. B. Furber. Interfacing real-time spiking I/O with the SpiNNaker neuromimetic architecture. SUBMISSION PENDING - ICONIP, August 2010.

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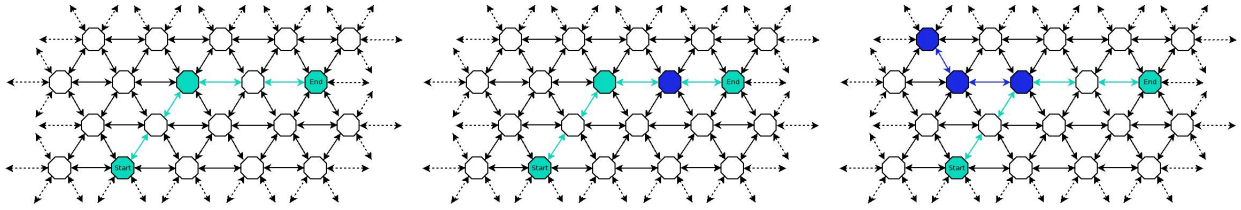
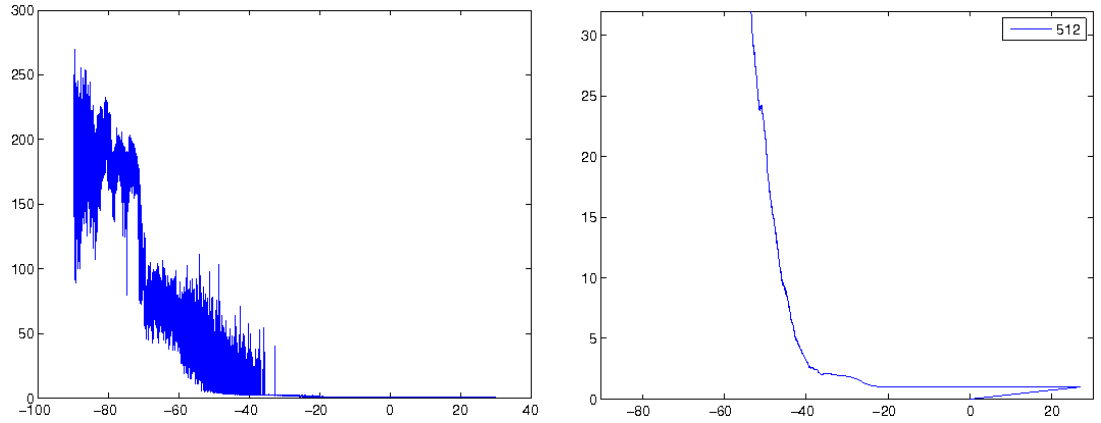


(a) Connection of a new neuron - Case 1 (b) Connection of a new neuron - Case 2 (c) Connection of a new neuron - Case 3

Fig. 2. Three different conditions for the synaptic rewiring. The cyan chips and connections are the existing ones, while the blue chips and connections are the one to be created or modified to connect the neuron as required



(a) Function that relates the membrane potential (X axis) with the time to spike (Y axis)

(b) Filtering with a 512 values window

Fig. 3. Membrane potential and time-to-spike relation function

[7] X. Jin, F. Galluppi, C. Patterson, A. Rast, S. Davies, S. Temple, and S. Furber. Algorithm and software for simulation of spiking neural networks on the multi-chip SpiNNaker system. *Neural Networks, 2010. IJCNN 2010. (IEEE World Congress on Computational Intelligence). IEEE International Joint Conference on*, 2010.

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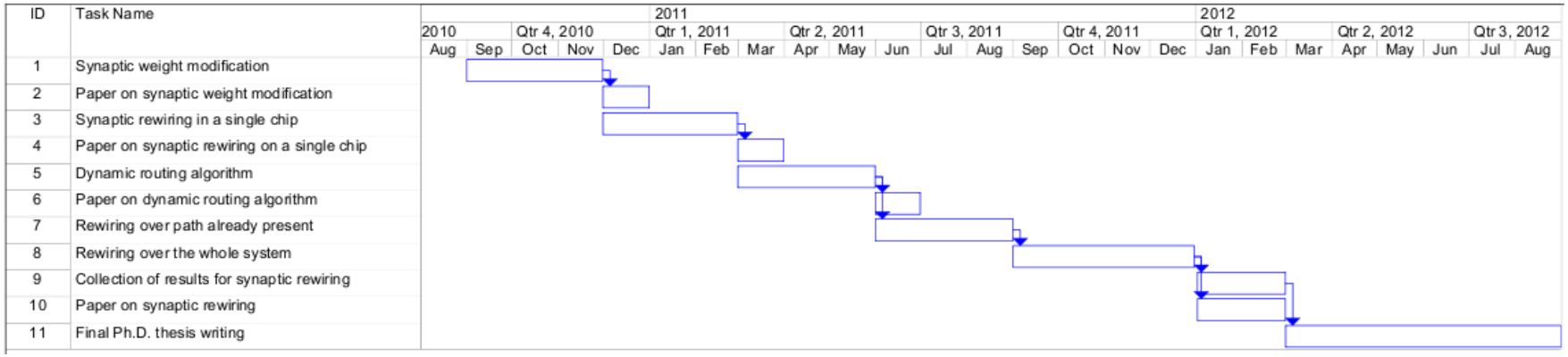

Fig. 4. Gantt Chart of the plan for the Ph.D. course.