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SpiNNaker: A Large-Scale Universal Spiking Neural Network Architecture

Sergio Davies & Francesco Galluppi

APT group
The University of Manchester

EPSRC ARM Silistix SpiNNaker

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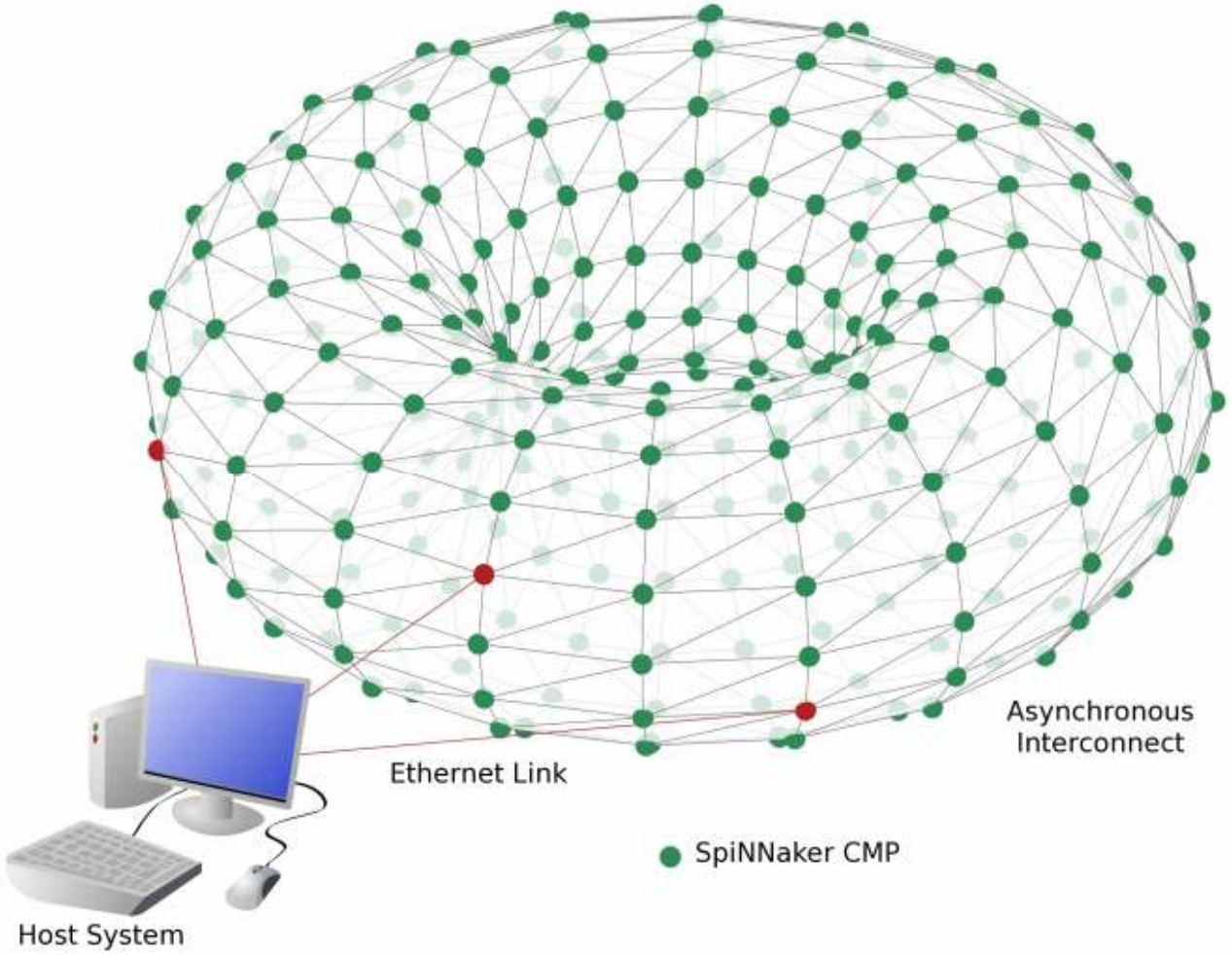
SpiNNaker project

- Multi-core CPU node
  - 18 ARM968 processors
  - to model large-scale systems of spiking neurons
- Scalable up to systems with 10,000s of nodes
  - over a million processors
  - >10^8 MIPS total



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Map Neural Networks to SpiNNaker

A Universal Spiking Neural Network Architecture

Application dynamics:
Neuron/Synapse/Plasticity

ITCM

Neuron data
parameters, state variables

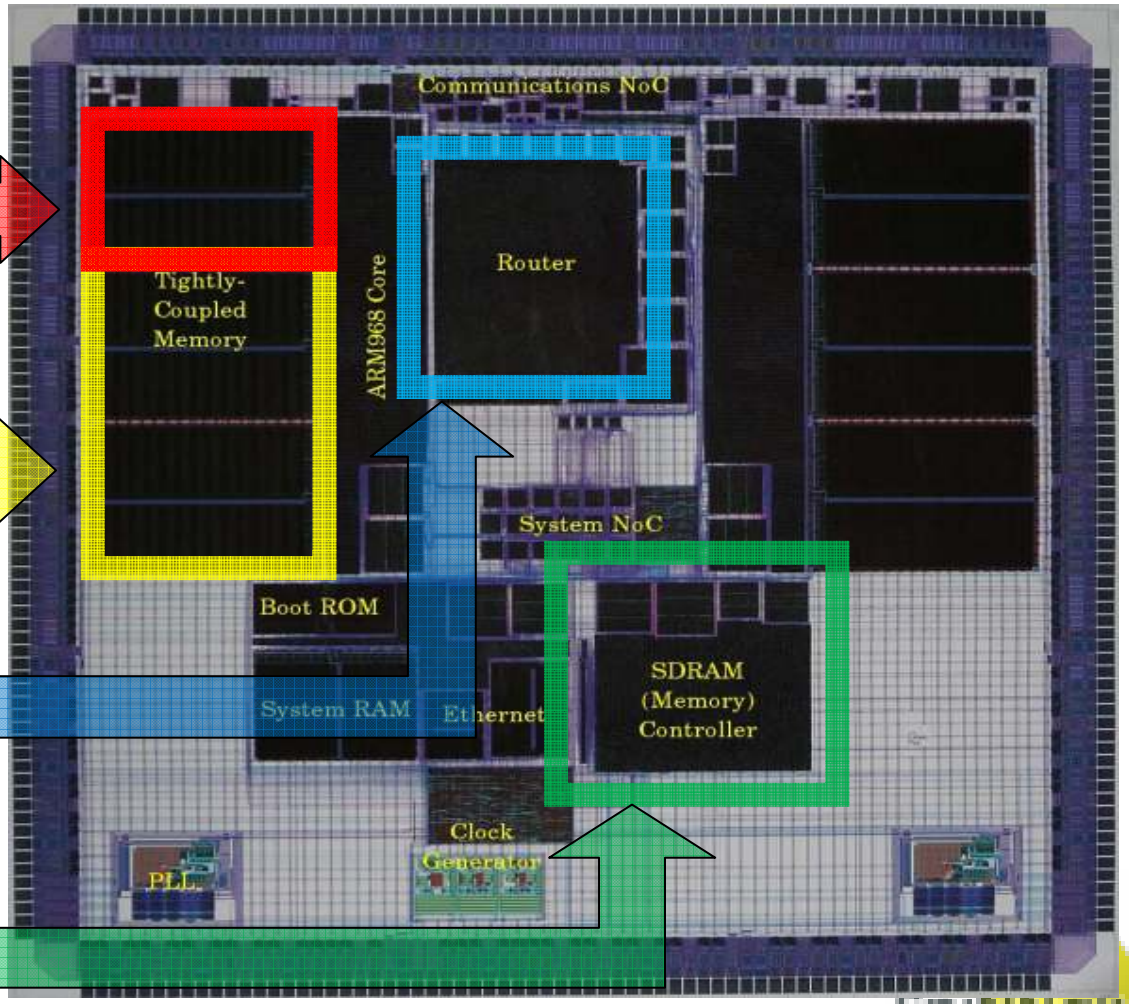
DTCM

Connectivity Information

ROUTER

Synaptic Data:
weight, delay, type of synapse

SDRAM



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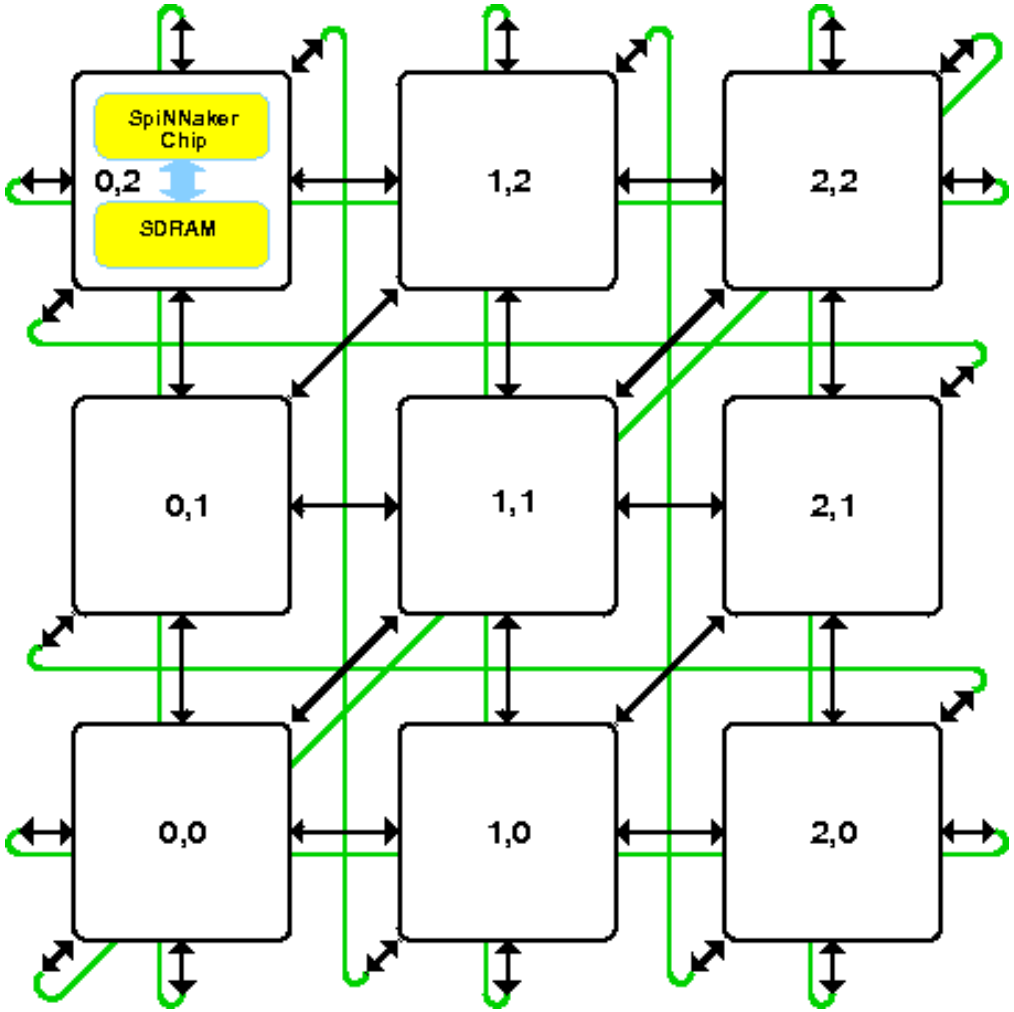
SpiNNaker system



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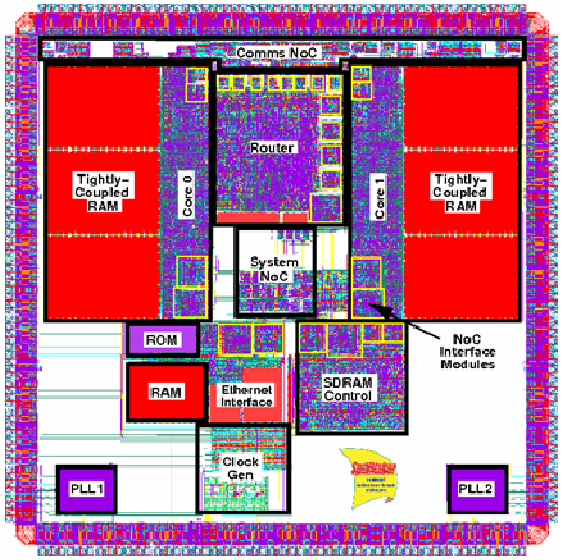
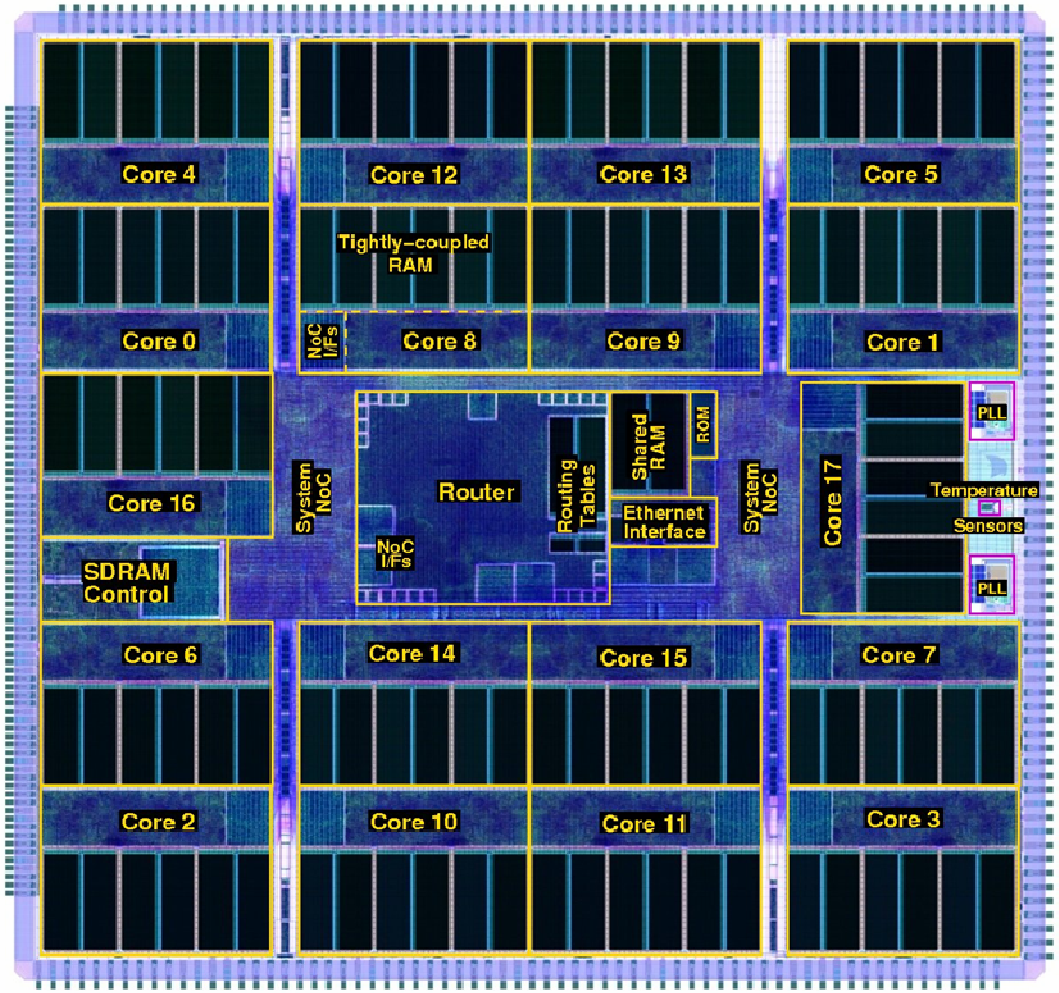
SpiNNaker chips





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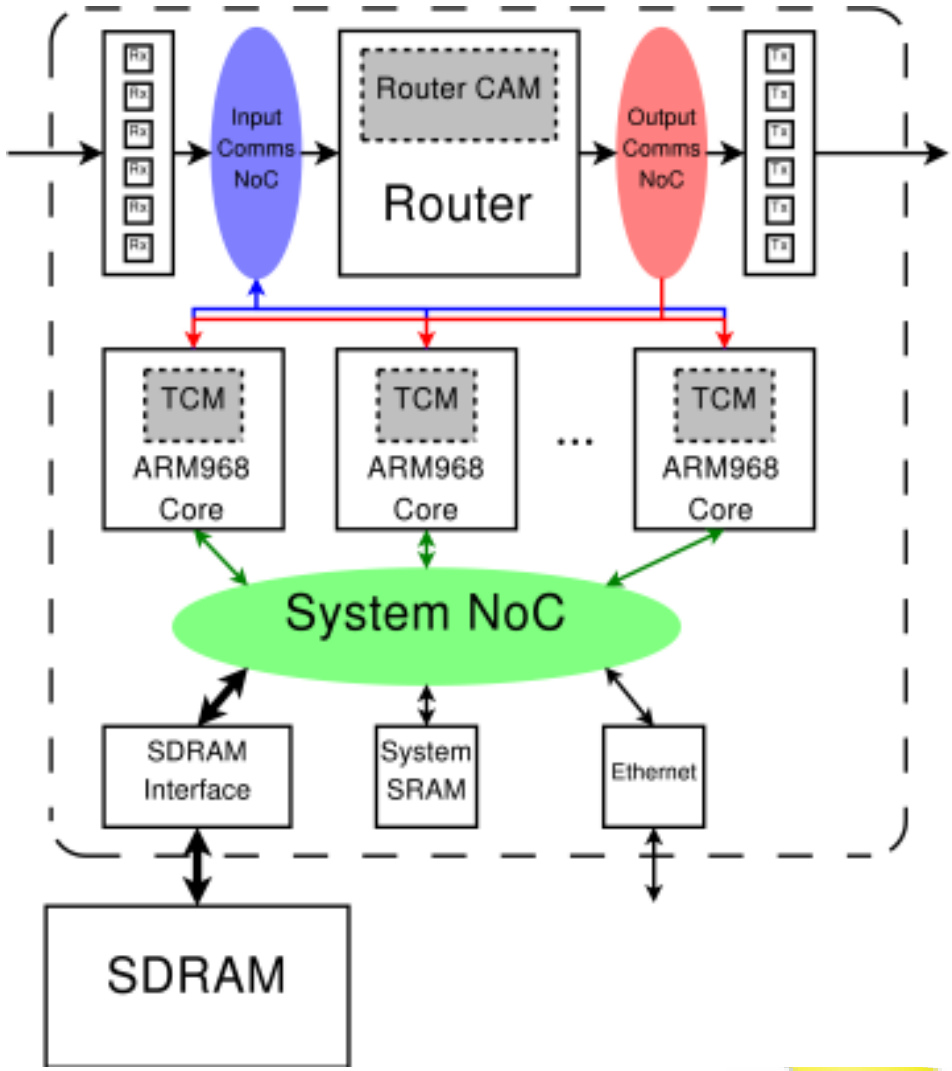
Features of the SpiNNaker chip

- Native parallelism
- Event-driven processing
- Incoherent memory
- Incremental reconfiguration



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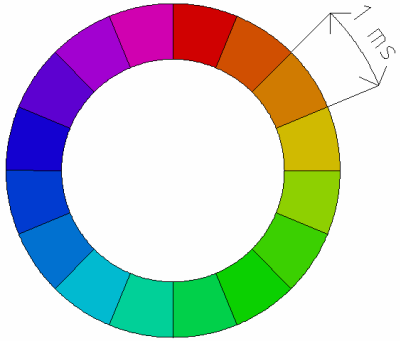
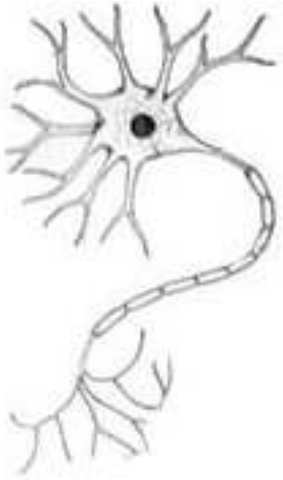
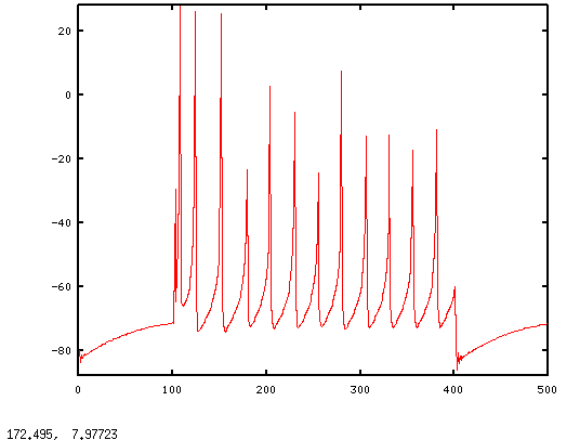
Neural simulation







Timer interrupt

Neuron input

Differential equation computation

Spike emission

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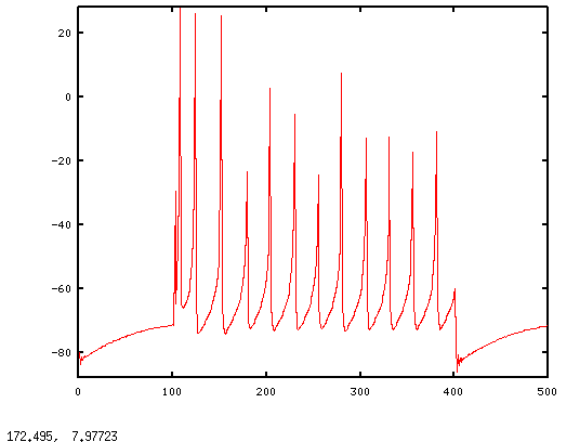
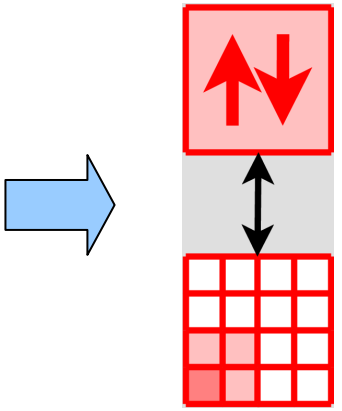
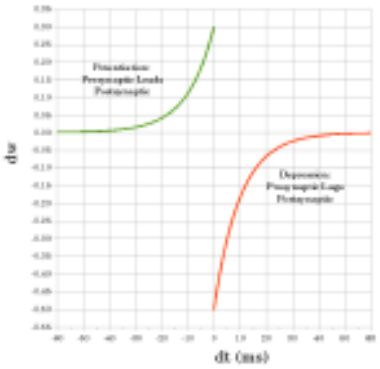
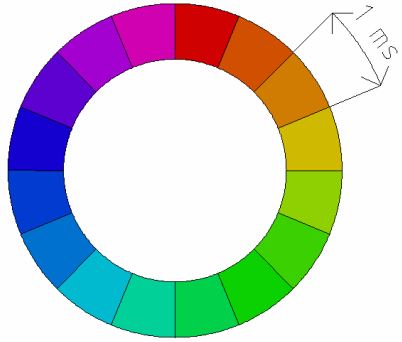
Incoming spikes









Spike incoming (interrupt received)

Retrieving synaptic weights

Synaptic plasticity (STDP)

Adding the new input in the delay buffer

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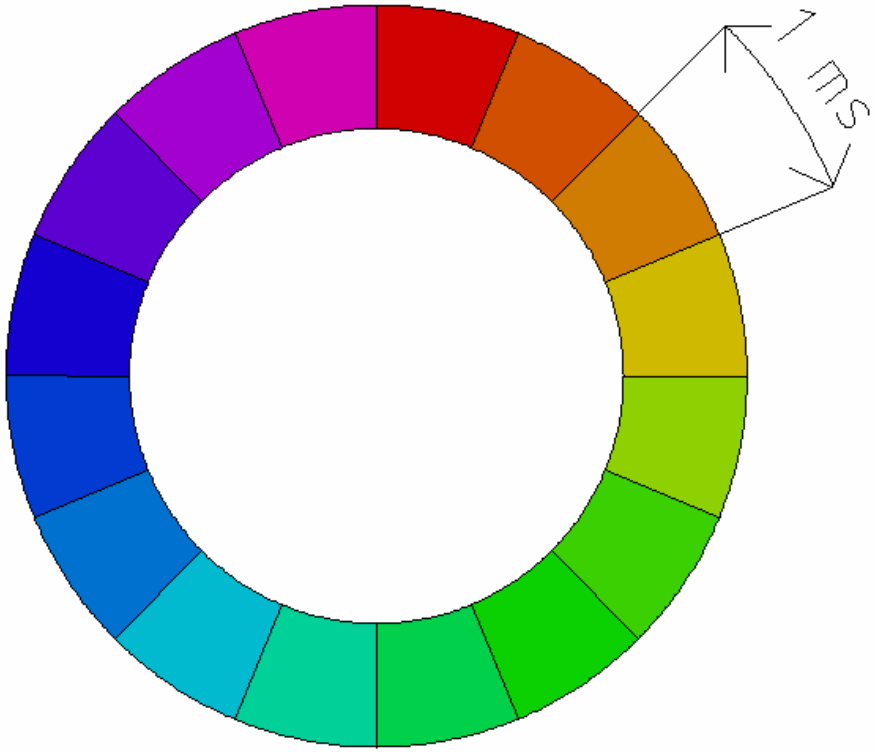
The delay buffer



- 1 millisecond each slot (a.k.a. bin);
- 16 slots for a maximum delay of 16 millisecond;
- Incoming spikes adds synaptic weights in the correspondent slot;

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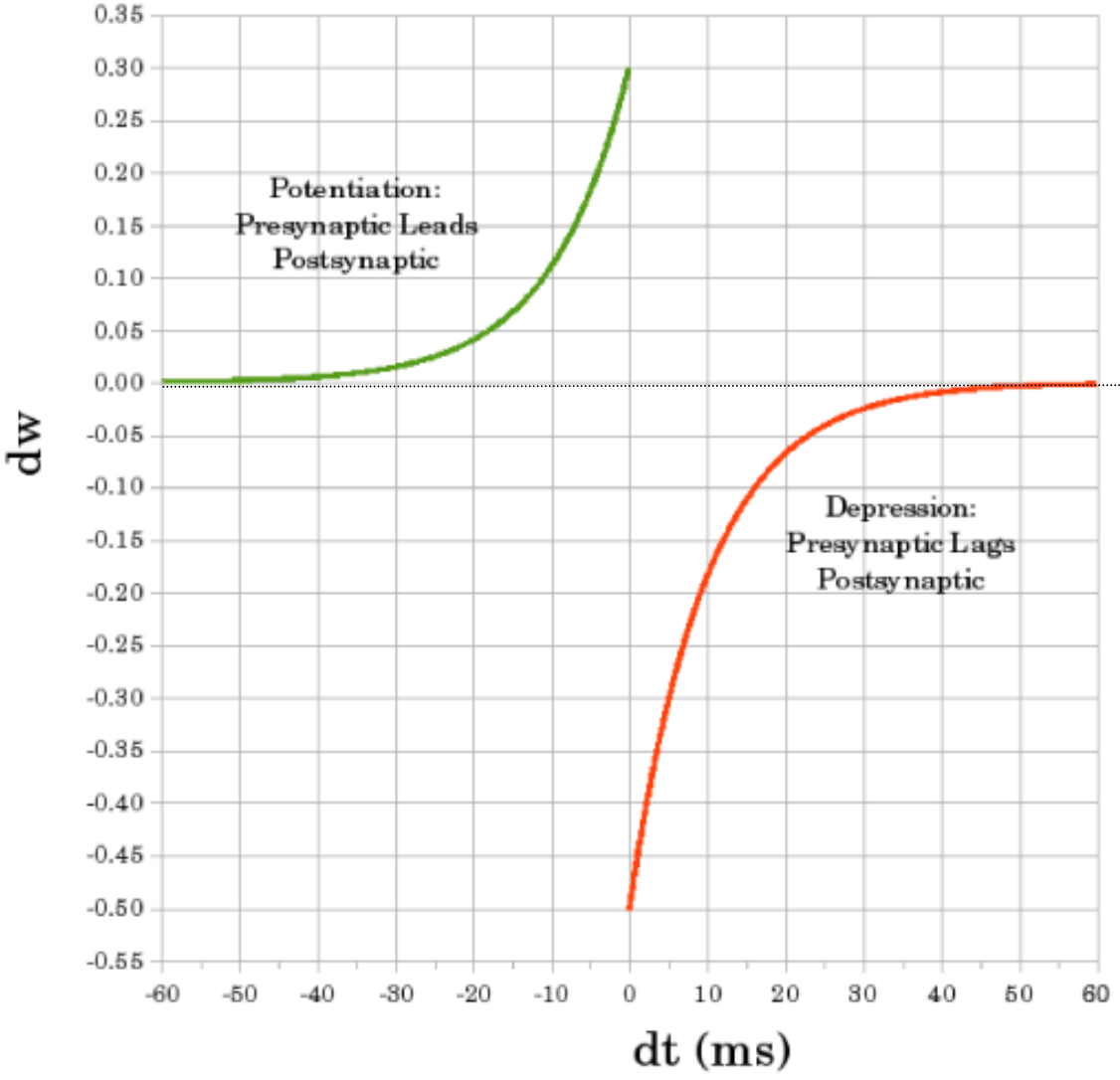
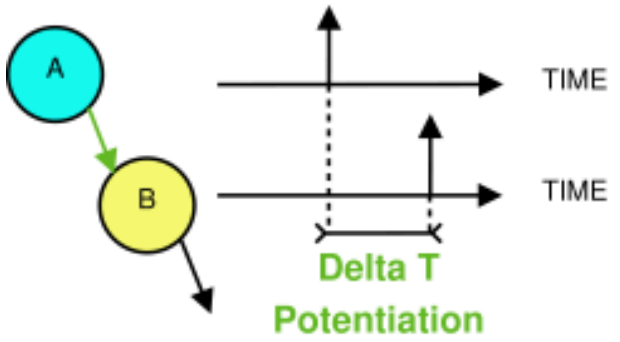
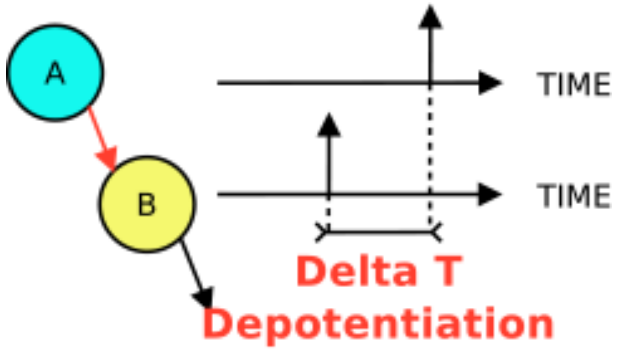
Spike Timing Dependent Plasticity







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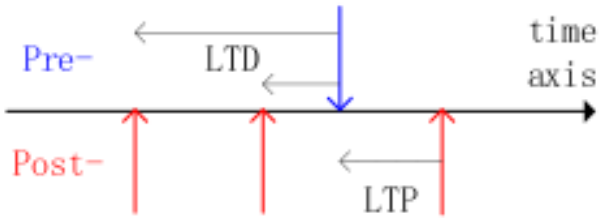
Implementation

Triggering the STDP algorithm

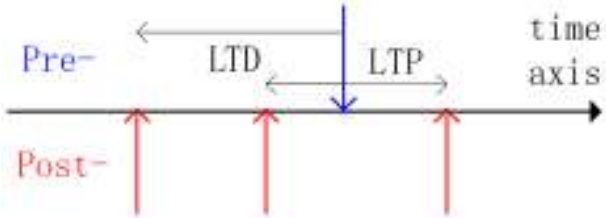
The usual way:



STDP is triggered on:

- Pre-synaptic spike arrival (LTD)
- Post-synaptic spike emission (LTP)

The SpiNNaker way:



- STDP is triggered only on pre-synaptic spike arrival (LTD and LTP)
- Weights are available only at pre-synaptic spike arrival.
- Since LTP needs future information, the algorithm needs to be deferred until the time window is filled

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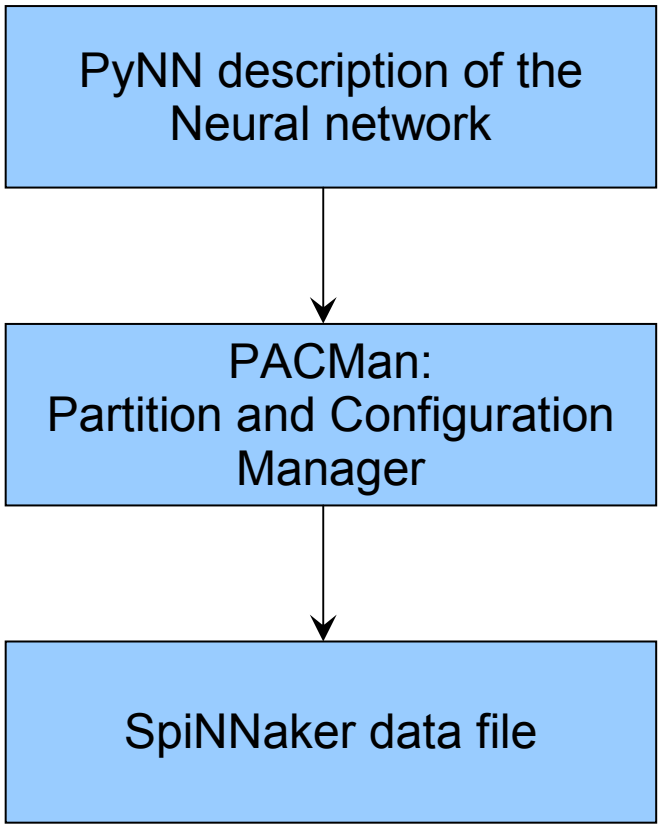
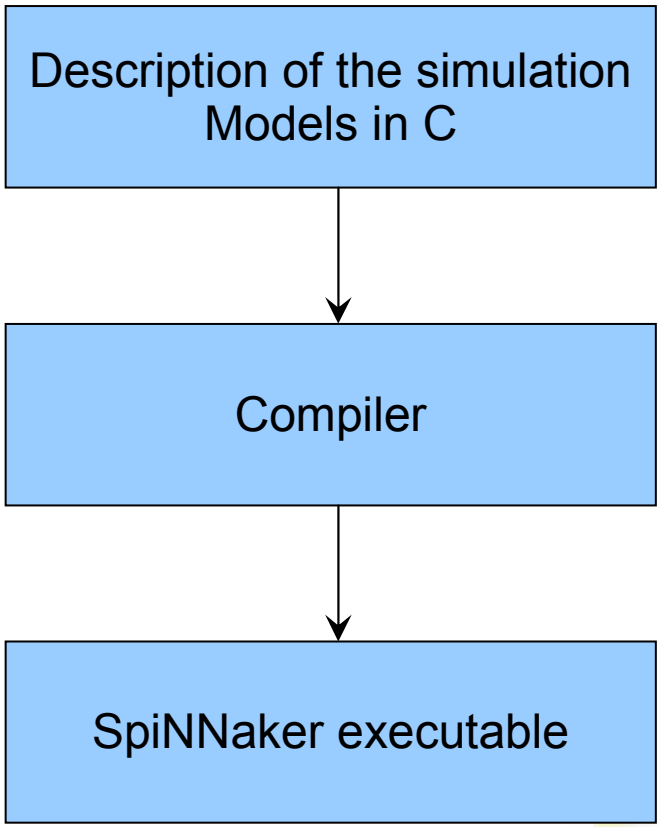
Data generation

Neural network structure



Simulator model



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Thank you!!!

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Back-up slides

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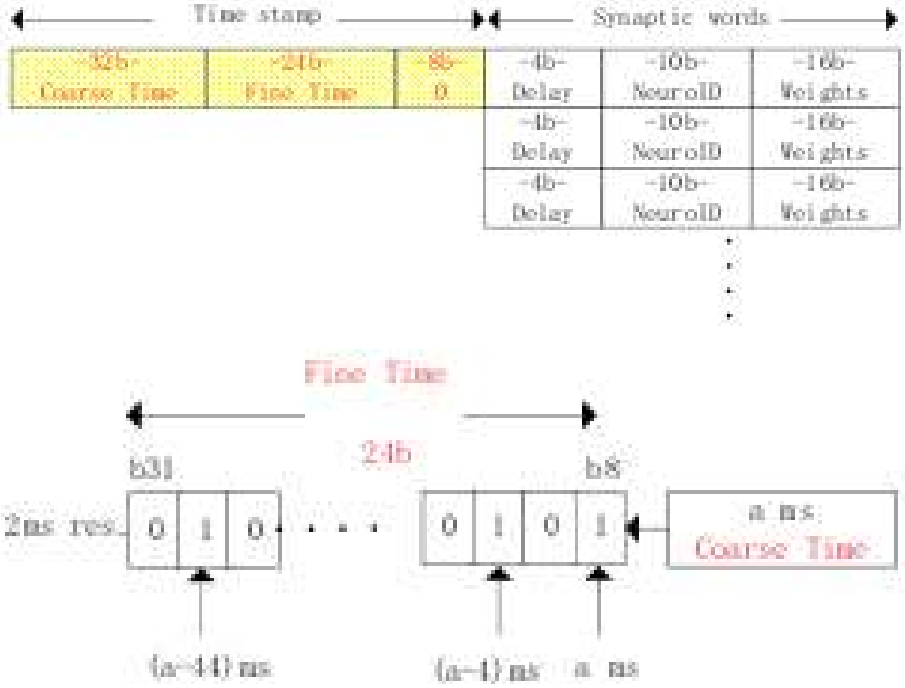
Implementation

Representation of spike timestamp

Pre-synaptic timestamp

Needed only when a pre-synaptic spike arrives. Stored as header of the synaptic weight block



Post-synaptic timestamp

Needed at all time. Stored in processor's local memory

Neuron 0	32b Coarse Time	64b Fine Time
Neuron 1	32b Coarse Time	64b Fine Time
Neuron 2	32b Coarse Time	64b Fine Time

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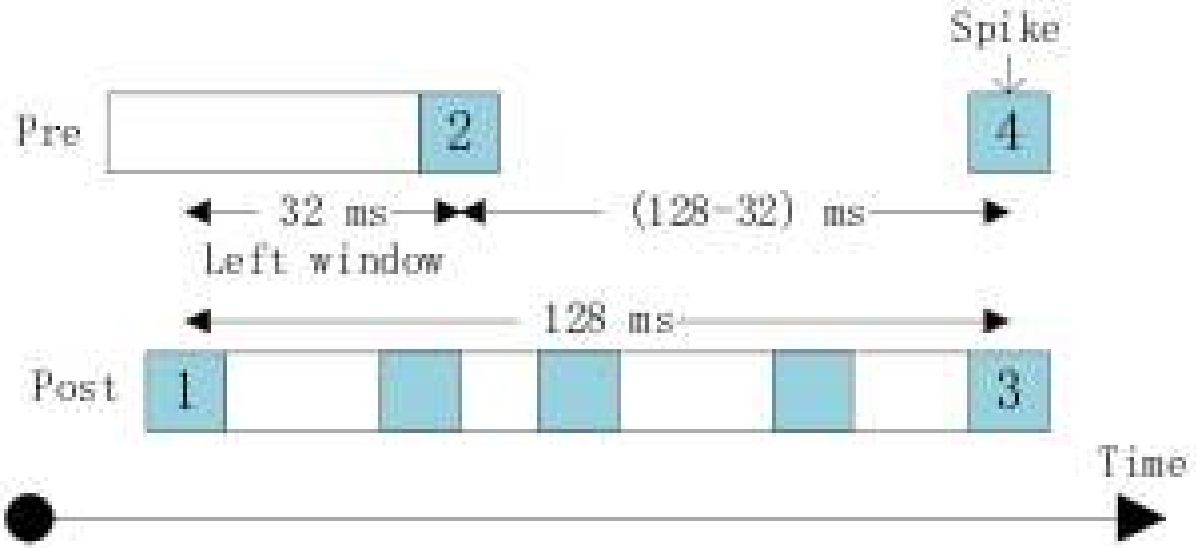
Implementation

Length of timing records



The STDP is triggered when an incoming spike pushes an old input record into the carry bit
However, if the input arrives at very low rate the output generated pushes forward the previous records and the history will be lost.

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