Power Efficiency and Reconfigurability

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1. The Vision

Recent years have seen a move towards reconfigurable hardware platforms for end-product development, as a result of spiralling costs of ASIC design. However, there is a conflicting requirement of low power consumption in many applications; the more programmable an architecture, the less power efficient it tends to be.

These two developments suggest that rather than "one size fits all" reconfigurable devices, the future will consist of domain-specific architectures.

Meanwhile, there is a range of domain-specific, *e.g.* Simulink/System Generator, and domain-general, *e.g.* C-based, approaches to the problem of behavioural specification languages. Some features of the High-Level Synthesis problem will be common amongst the spectrum of specification language(s) and domain-specific architectures, such as resource allocation issues, whereas some will be specific to certain specifications, such as transfer-function manipulation, and some will be specific to certain architectures, such as hardware/software partitioning for bus-based architectures.

We would like form a system that can take a variety of input language specifications, and produce designs optimized for a variety of different domain-specific architectures, based around a common infrastructure.

If the variety of architectures could be expressed in a common "architectural description language", then the synthesis system would be able to act accordingly.

The CAD tools and the architecture would be developed concurrently, and the re-targetable synthesis system would form a platform for exploring the design space of the next generation of reconfigurable architectures.

2. The Impact

This vision, if realised, will have a major impact on both the high-level design industry, *i.e.* companies like Celoxica, but also on the reconfigurable device manufacturing industry. Power-efficient reconfigurability will, in the short term, result in a much faster time-to-market for mobile devices. In the long term it will be a necessity even for non-mobile devices, without which thermal technology will not be able to keep pace with Moore's law.

3. Scope for Collaboration

The establishment of a common architectural description format, and a framework to define the required features of input description formats and resulting architectural features, will enable the division of this task by problem domain. For example, one group could work on the DSP domain, one group on the Networks domain, while sharing a common supporting infrastructure.
There is strong multi-disciplinarity across the subjects of Electrical and Electronic Engineering and Computing. Demonstrator projects could result in further multi-disciplinary collaborative possibilities.