

Impact of nano-CMOS devices on future microelectronic design

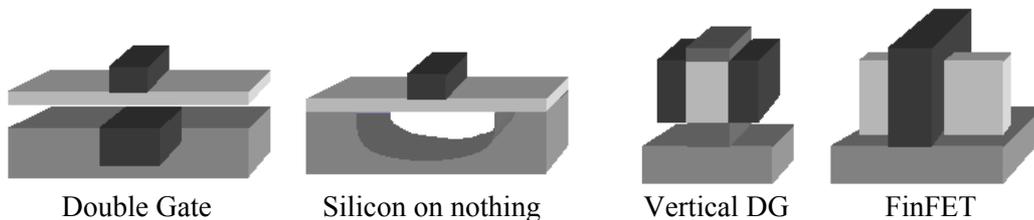
Vision Statement

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For more than three decades a significant fraction of analogue, mixed signal and all digital designs have been based on conventional MOSFETs. Despite aggressive scaling of these devices their basic structure, operation, materials and electrical characteristics have remained broadly similar. As a result, circuit and system design has evolved conservatively, allowing significant reuse of design techniques across device generations.

Currently, 90 nm technology node high performance MOSFETs with 35 nm physical gate lengths are in mass production. However, there are clear indications that it will be impossible to effectively scale conventional MOSFETs beyond the 45 nm node, which is expected to be in mass production in 2010. Gate oxides are thinning past the point of acceptable gate leakage. Doping concentrations, needed to ensure device electrostatic integrity, are high enough to unacceptably degrade charge transport and device performance. According to the International Roadmap for Semiconductors (ITRS) at least one major material or architecture innovation will be needed for every new device generation until the end of the roadmap in 2018. These include architectures such as; fully depleted Ultrathin Body (UTB) SOI, FinFET, trigate or Ω gate FETs and planar self-aligned double gate transistors. New materials are also required; high- κ gate dielectrics, strained silicon, germanium and III-V channels. It is expected that there will be not a single winner to supersede conventional MOSFETs and so various device architectures will coexist and compete, often on a project-by-project basis depending on the market goals of each IC manufacturer. New and the conventional transistors will co-exist on-chip in future System on a Chip (SoC) technology platforms.



Examples of device architectures expected to be introduced in future technology nodes.

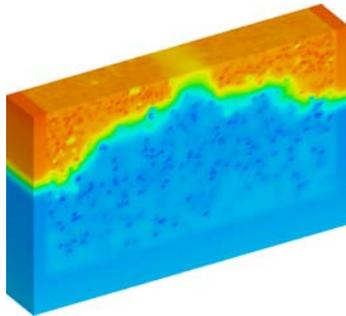
The new device architectures will have a profound effect on design, with more radical changes in device layout and electrical behaviour, and a greater mix of devices in the same system. The pace of change will also be faster than anything seen in the past. Competition will favour designers who take best advantage of the new device architectures in their designs. This may be particularly problematic for UK designers both in academia and industry, who do not have the benefit of close local interactions with the large IC manufacturers who drive these changes. The situation calls for closer interactions and collaboration between the silicon device research and the UK design community.

The following research objectives cross the boundaries between the two communities and will enhance innovation and competitiveness of both UK academic and industrial design.

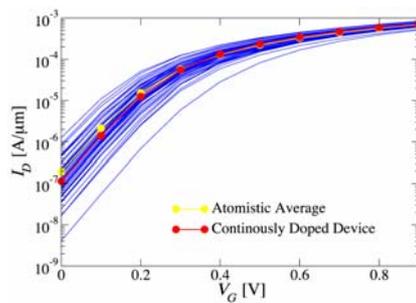
- Early understanding of the operation and characteristics of next generation nano-CMOS devices with new architectures and material structures.
- Development of compact models and parameter extraction strategies for the new devices.

- Early supply of compact model parameters for the new architectures, through physical simulation and research prototypes.
- Detailed investigation of the impact of new device architectures on well established circuit building blocks and systems (which presently use conventional FETs).
- Development of automated design tools to convert designs based on conventional FETs to designs utilising new device architectures.
- Development of new circuit and system design concepts utilising specific properties of the new device architectures.
- Development of design methodologies which allow the mixing of different device architectures in single circuit or SoC design.

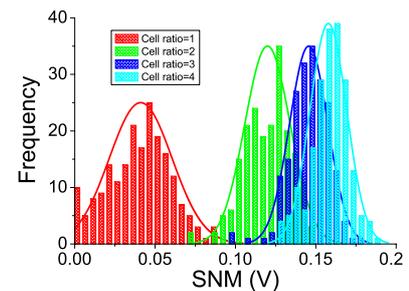
An important problem which is predicted to adversely affect the design of next generation analogue, digital and mixed signal circuits (and which acts as a specific example of the interesting research areas at the interface of device and circuit design noted above) is the ever increasing magnitude of intrinsic parameter fluctuations introduced by the discreteness of charge and matter in the next generation nano-CMOS devices independent of architecture.



3D simulation of a 35×35 nm FET featuring random discrete dopants. The potential distribution is colour mapped. Potential fluctuations in the channel associated with the dopant distribution result in different characteristics for each device.



Set of I_D - V_G characteristics for an ensemble of 200 macroscopically identical but microscopically distinct 30×30 nm MOSFETs. Differences result from varying numbers and positions of dopants within the active region of each transistor.



Distribution of static noise margins in SRAM cells assembled using an ensemble of 200 distinct 30×30 nm FETs. Only cells with a cell ratio larger than 3 achieve 90% yield in 1Mbit systems.

As illustrated above, variations in the number and position of dopants, make even contemporary MOSFETs microscopically different, introducing significant parameter variations from device to device. In addition, the trapping of a single electron in the channel region can change device I_D by over 100%. Interface roughness on the order of 1-2 atomic layers and related local variations in the oxide/body thickness introduce variations in gate tunnelling, quantum confinement and mobility between devices. The granularity of gate materials and the photo-resist introduce unavoidable line edge roughness (LER) in the gate pattern definition and variations in device geometry. New materials such as high- κ dielectrics and SiGe are predicted to exacerbate these variations. All these effects introduce intrinsic parameter fluctuations whose magnitude increases as devices shrink, and will increase dramatically as CMOS scales to nanometer dimensions. Contrary to the device parameter variations introduced by well understood processing deviations, these intrinsic parameter variations cannot be controlled by improving the fabrication technology.

Intrinsic parameter fluctuations will have a crucial impact on the functionality, yield and reliability of both analogue and digital circuits and systems. They already affect the scaling of SRAM cells, at a time when absolute noise margins are shrinking due to continued

supply voltage reduction. Pictured above are random dopant induced distributions of static noise margin (SNM) in an ensemble of SRAM cells of various cell ratios, for devices in the advanced stages of the 90 nm technology node. To obtain acceptable yield in the presence of such fluctuations, the cell ratio of the circuit must be increased from $W/L=1$ to $W/L=3$.

The problems introduced by intrinsic parameter fluctuations are well understood and under active research by large semiconductor players like Intel, Motorola/Freescale and IBM, but not widely advertised, and not well appreciated by the design community – particularly in the UK. As a leading international player in the simulation and understanding of the various sources of intrinsic parameter fluctuations in nano-CMOS, the Device Modelling group at Glasgow is funded, not only by EPSRC and EC, but also by IBM, Freescale, Toshiba and Fujitsu – all in this specific area. This creates an opportunity for the UK design community to obtain an early quantitative and qualitative appreciation of the implications of intrinsic parameter fluctuations on the next generation circuits and systems. The research activities at the interface between the device and the circuit community might include.

- Comprehensive physical simulations in order to understand the source and the magnitude of intrinsic parameter fluctuations in transistors with conventional and novel device architectures to the end of the roadmap, and beyond.
- Development of compact model and parameter extraction strategies which capture intrinsic parameter fluctuation effects and can be used in circuit and system simulations.
- Studying the impact of the intrinsic parameter fluctuations on circuit building-blocks and systems and understanding at which technology node they will be prohibitive for particular components design.
- Development of intrinsic parameter fluctuations resistant architectures including concepts like, redundancy, self-organisation, self-healing and random logic.
- Developing circuit concepts and architectures that could benefit from the presence of intrinsic parameter fluctuations (for example neural network based computing, pattern recognition and control).