Design methodologies for complex SoC

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The following document outlines a number of grand challenges which have been developed to some extent, with a "design" philosophy in mind.

(1) Intelligent" design flow. This would allow a system realisation to be achieved against the following metrics: speed, energy, area, level of programmability, reconfigurability, speed of design, memory requirements. The concept would to be develop a suitable mathematical system description e.g. using dataflow for DSP systems, and then allow automatic translation against a list of the goals highlighted above that are ranked in terms of importance/relevance. It would be envisaged that this design flow would accurately be able to rank possible hardware solutions in terms of metrics used and would therefore, need to consider in a hierarchical manner, detailed implementations. Ideally, this design flow would realise efficient system design allowing trade-offs between RF circuit complexity and DSP system realisation. For example, there is a considerable effort in simplifying RF receiver front ends (as they do not scale with technology) and introducing more complex DSP circuitry to realise system implementation.

(2) Portable speech recognizer. This would allow real-time efficient speech recognition with a very high capacity recognition for a range of different languages. This would revolutionalise human-machine interaction allowing various forms including real-time dictation, efficient interaction for a number of applications including banking, airport check-in, novel locking systems. This presents enormous memory storage issues and novel solutions are required to allow the operation to be performed in real-time.

(3) Wireless sensors. The target here would be to develop a low-power wireless sensor. I'm not exactly sure of system target performance requirements here but it could be a sensor that could last up until a month, transmitting over a 10 metre range and allowing various forms of processing such as movement, sound, image to be performed. From a design point of view, this requires considerable interaction with the design of the wireless receiver, low energy operation (in terms of both wireless system design and mode of operation), new technology. A considerable amount of activity exists in this area by a number of research institutes including the Wireless Research Centre at Berkeley and Stanford University.

(4) Optimised processor platform. The target here will be to develop an "on-the-fly" processor architecture that best matches the computational requirements. Obviously the high costs of developing masks for new SoC designs will negate development on an application-by-application basis, but considerable scope exists for investigating processor architecture for a range of applications and will cover memory organisation and hierarchy, high speed interconnection (probably asynchronous), architecture development based on low power applications, etc…This would also consider close integration of analog circuitry. This would probably be linked to the thoughts in (1) as the tool flow and system architecture are closely linked.

The purpose of this document is to provide initial thoughts on possible "grand challenges" for microelectronics design and does not represent a definite list or comprehensive description of the possible challenges.