Bio-Inspired Hardware: vision statement

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Areas of research in the domain of hardware realization include pulsed neural networks, which is motivated by the nature of the communication medium used in real neural, reconfigurable digital platforms, dedicated analogue topologies and mixed mode techniques. However, there are many challenges, common to all of these approaches, which must be overcome if neural networks realized in hardware are to succeed as a viable general-purpose intelligent computational machine. A major challenge is the development of efficient hardware implementation techniques that can be scaled to very large density with acceptable power requirements. Neurons receive thousands of inputs simultaneously via their synapses and hence from a hardware viewpoint, it is clear that the dominant building block within a neural system is the synapse, which can either be implemented in analogue, digital or a hybrid of the two. From the point of view of precision and noise immunity, the digital option is the preferred one. However, if neural networks, comparable in terms of scale to their biological counterparts, are to be implemented, then the core neuronal functions such as synaptic plasticity must be achieved with minimal power requirements, consume minimal area and exhibit a biologically plausible transfer function. These constraints alone suggests an analogue approach. Therefore, the preferred option is probably to realize low level neuronal functionality, such as spike generation and membrane time dependence, using analogue components and higher level network functionality, such as inter-neuron communications, weight storage, etc, using digital components: a mixed-mode approach. Paramount to the success of this approach is the availability of device level components with characteristics that are explicitly compatible with low level functions within the neural systems. To this end we propose the following.

Our work is currently exploring the potential of a two capacitor Charge Coupled Device (CCD) structure as a synaptic node and a multi-gate neuMOS transistor as the integrating/thresholding point neuron. Modulation of the inputs via synapses will be achieved using a packet of charge in the inversion layer of one of the MOS capacitors where the associated gate voltage controls the magnitude of the charge packet. The CCD structure uses two conventional MOS capacitors side by side, where the first capacitor will have a “permanent inversion layer” induced in the substrate of magnitude that reflects the “weight” voltage stored on the gate. The second capacitor will be used to “clock” the charge packet onto the gate of a multi-gate ‘neuMOS’ transistor whose threshold voltage will determine the firing level of the neuron. In this arrangement the clock for the second capacitor is the pre-synaptic neuron output, which serves to release the “weighted” charge packet. Hence, the magnitude of the postsynaptic spike is proportional to the density of charge in the charge packet and therefore is modulated by the voltage stored on the gate of the first capacitor.

The novelty of the CCD synapse is evident if the limitations of current state-of-the-art VLSI architectures are considered. These architectures fail to match the scale of biological networks because the fundamental building blocks (transistors) do not possess the correct physical attributes to emulate a synapse. The problem of a modifiable connection, i.e. synaptic plasticity, lies at the core of our current inability to build biological-scale networks. Although single-transistor based synapses exist, their solid-state characteristics are simply too restrictive in the way they attempt to mimic synaptic plasticity. If a small geometry low power semiconductor device could be engineered to provide the same attributes as a biological synapse, then larger and more powerful networks become realisable. The authors feel that proposed CCD structure could provide a single device solution that combines the ability to generate a spike characteristic, and therefore serves as the output of the pre-synaptic neuron, with the ability to emulate plasticity behaviour, as the spike amplitude can be either attenuated or amplified. In addition, the synapse proposed in this work, is based on a well proven and robust CCD technology, is clearly a very simple but effective method of implementing a synapse in hardware and facilitates an ultra low power small geometry implementation.