SEVENTH FRAMEWORK PROGRAMME
THEME ICT-2007-1-3.3
Embedded systems

Grant agreement for: **Collaborative Project**
Small of medium-scale focused research project

Annex I - "Description of Work"

Project acronym: GALAXY

Project full title: GALS InterfAce for CompleX Digital SYstem Integration

Grant agreement no.: 214364

Date of preparation of Annex I: 23/10/2007

Date of approval of Annex I by Commission: 26/10/2007

List of Beneficiaries

Beneficiary Number	Beneficiary name	Beneficiary short name	Country	Date enter project	Date exit project
1 (coordinator)	IHP GmbH - Innovations for High Performance Microelectronics/ Institut fuer Innovative Mikroelektronik	IHP	Germany	1	36
2	The University of Manchester	UNIMAN	UK	1	36
3	Ecole Polytechnique Fédérale de Lausanne	EPFL	Switzerland	1	36
4	Alma Mater Studiorum - Università di Bologna	UNIBO	Italy	1	36
5	Silistix UK Limited	STX	UK	1	36
6	Infineon Technologies AG	INFINEON	Germany	1	36

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A.1.1 OVERALL BUDGET BREAKDOWN OF THE PROJECT

Grant agreement Preparation Forms

EUROPEAN COMMISSION

7th Framework Programme on Research, Technological Development and Demonstration

Collaborative Project

A3.2: What it costs

Proposal number (1) 214364 *Proposal acronym (2)* GALAXY

ONE FORM PER PROJECT

Participant number in this project	Organisation short name	Estimated eligible costs (whole duration of the project)				TOTAL A+B+C+D	Total receipts	Requested EC contribution
		RTD / Innovation (A)	Demonstration (B)	Management (C)	Other (D)			
1	IHP	712.000,00	0,00	104.073,97	0,00	816.073,97	0,00	638.073,97
2	UNIMAN	735.542,00	0,00	17.846,00	0,00	753.388,00	0,00	569.502,50
3	EPFL	543.040,00	0,00	2.400,00	0,00	545.440,00	0,00	409.680,00
4	UNIBO	490.800,00	0,00	13.000,00	0,00	503.800,00	0,00	381.100,00
5	STX	662.099,50	0,00	11.450,00	0,00	673.549,50	0,00	508.024,63
6	INFINEON	787.237,80	0,00	0,00	0,00	787.237,80	0,00	393.618,90
TOTAL		**3.930.719,30**	**0,00**	**148.769,97**	**0,00**	**4.079.489,27**	**0,00**	**2.900.000,00**

A.1.2 PROJECT SUMMARY

Grant agreement Preparation Forms

EUROPEAN COMMISSION

7th Framework Programme on Research, Technological Development and Demonstration

Collaborative Project

A.1: Our Project

Project number (1)	214364	*Project acronym (2)*	GALAXY

ONE FORM PER PROJECT

GENERAL INFORMATION

Project Title (3)	GALS InterfAce for CompleX Digital SYstem Integration		
Starting Date (4)	01/01/1900		
Duration in months (5)	36	*Call (part) identifier (6)*	FP7-ICT-2007-1
Activity code(s) most relevant to your topic (7)	ICT-1-3.3	-	-
Free keywords (8)	GALS, asynchronous design, system integration, NoC, EMI reduction, deep-nanometer technologies		

Abstract(9) (max. 2000 char.)

This project builds on a technology approach in which the EU currently has world leadership, thanks to previous pan-European funding, and in which the participants are recognised centres of excellence. We propose to provide an integrated GALS (Globally Asynchronous, Locally Synchronous) design flow, together with novel Network-on-Chip capabilities, that will materially aid embedded system design for a significant class of problems. We aim to remove existing barriers to the adoption of the technology by providing an interoperability framework between the existing open and commercial CAD tools that will support development of heterogeneous systems at the different levels of abstraction. The project will evaluate the ability of the GALS approach to solve system integration issues and, by implementing a complex wireless communication system on an advanced 45nm CMOS process, explore the low EMI properties, inherent low-power features and robustness to process variability problems in nanoscale geometries.

A.1.3 LIST OF BENEFICIARIES

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PART B

B1. Concept and objectives, progress beyond state-of-the-art, S/T methodology and work plan

B.1.1 CONCEPT AND PROJECT OBJECTIVES

B.1.1.1 Objectives of GALS architecture for target applications

It is envisioned by the European Nanoelectronics Initiative Advisory Council (ENIAC) that during the course of the FP7 the CMOS technology miniaturisation will continue, even if increasing difficulties may slow down the pure technological progress. And in fact, the increased complexity, performance requirements, and the need for power and EMI reduction present almost unsolvable challenges to designers of complex embedded systems. The continued technology improvement towards nanoscale dimensions generates additional problems for embedded system design. The combination of complex application requirements and technology imperfections (e.g. process variability and reliability) exacerbate the problems of timing closure and clock tree generation requiring additional design iterations and extended design-to-market time. It is imperative to deal with these issues; one very promising option is the use of a Globally Asynchronous Locally Synchronous (GALS) design methodology.

The idea of GALS system design is not entirely novel. However, despite significant research effort, the number of industrial GALS applications is currently relatively low.

When analyzing why a GALS approach has not been adopted by industry we observe that several issues have not been fully addressed until now. Firstly, the design-flow for GALS chip interconnect is not mature enough to guarantee reliable and comfortable chip design. Secondly, the main strengths of GALS design, such as improvement of system integration, better EMI characteristics and power reduction, were never completely exploited and proven in practice. Lastly, the targeted GALS applications were sometimes not a perfect match with the GALS techniques.

From our perspective, a GALS solution needs to have the following properties in order to be widely used: standard interfaces should be defined that will be widely adopted (rather than the existing situation in which numerous GALS proposals have each suggested their own interfaces to the synchronous world); the GALS design flow should be based on standard EDA tools extended with an additional reliable and user-friendly asynchronous tool-set; the GALS interface architecture should be based on high-throughput, low complexity solutions; the GALS interface proposal and source code should be offered free-of-charge within an open core framework to gain popularity and to break the prejudices that exist to mixed asynchronous/synchronous approaches.

An important aspect of GALS success or failure is the target application. It is expected that a GALS based chip interconnect will be a good choice for applications in certain fields while in others it will be used very rarely. We think that GALS can show the best results for designs with moderate performance and very complex structure. Another aspect is the design cost. GALS design methodology offers advantages in system integration and consequently GALS can be an extremely useful approach for submicron systems with a short time to market as long as it is supported by an automated design flow based on commercial CAD tools.

In this project, we address these problems and intend to prove that the GALS methodology offers powerful solutions for modern embedded system design integration. We aim at promoting the development of GALS system design by providing an interoperability framework between the existing open or commercial CAD tools for rapid design and prototyping. This framework will support development of heterogeneous systems at the different levels of abstraction. We will explore and evaluate the ability of GALS to solve system integration issues as well as building on its reduced EMI and low-power properties. A promising target platform can be seen in the area of Networks on Chip (NoC) [DEM06]. The NoC paradigm seems to be very attractive solution for the future chip interconnect. There are already a few NoC platforms based on the GALS architecture [DOB05, BEI05,

BJE05]. In this project we intend to investigate different approaches of implementing GALS-enabled NoC platforms, comparing them with fully synchronous implementations, and of integrating the NoC design flow into the GALS design flow.

Finally, with further process miniaturization and increases in system complexity, we see the emerging need for a powerful system integration technique. Furthermore, nanoscale technologies have their own issues such as process variability and reliability. The ENIAC strategic research agenda indicates system integration and parametric variation concerns as two causes that are pushing us closer to the limits of CMOS scaling. In the framework of this project we will explore these critical issues in the context of GALS. Additionally we intend to evaluate the effectiveness of a GALS system design for a highly complex wireless communication application in a very advanced 45 nm CMOS process. We intend a true evaluation of the improvements offered by GALS methods by implementing in parallel a GALS and a pure synchronous version of the example design. With this approach we should be able to present a fair comparison of the effort needed for system integration and for finishing the design process for both cases. We plan to fabricate a separate second chjp in order to compare the effectiveness of the GALS technique of dealing with EMI and of reducing the power without harming performance.

B.1.1.2 Scientific and Technical Project Objectives

On the basis of the previous discussion, we are planning to analyse existing GALS solutions with stretchable or data-driven clocking, and GALS solutions with an asynchronous FIFO interconnect and independent local clocking. During the project we will select optimal GALS architectures for the target applications and define the communication interfaces (8th month of the project). The suggested "optimal" solutions should be based on the existing GALS architectures. However, it is expected that selected the GALS design could incorporate several optimized features in terms of hardware complexity, performance, power dissipation and EMI. We will consider also integration of the GALS interfaces into the NoC application scenario. The criteria for selecting and generating the optimal GALS architecture are based on conformity to the rules and directions and to the probable target application named in Section B1. The proposed solution should have scalable interfaces and, where possible, its source code will be offered as an open core.

In this project, a GALS framework providing interoperability between design tools for rapid design and prototyping will be proposed. This design flow will be based on commercial CAD tools and on the existing Balsa framework [BAR00] with extensions to mixed synchronous-asynchronous systems. Balsa has until now been used for designing pure asynchronous circuits. The main idea is to integrate the Balsa language and tools in a system level design environment, where Balsa will be seen just as any other language, in order to allow mixed descriptions of synchronous and asynchronous circuits. Consequently, we will generate a system level design tool that is able to handle IP blocks referring to Balsa, Verilog, VHDL and SystemC specifications with an open plug-in interface to easily accept new languages and tool flows. The emphasis will be on a graphical system-level design environment acting as a controller and interoperability layer between conventional CAD tools. Firstly, a tool flow will handle the dependencies, file format requirements and incompatibilities between tools, and will control the sequential execution of format conversion, compilation, synthesis and simulation tools. A co-simulation back-plane will provide interoperability between the simulators and emulators from different vendors, enabling the co-simulation and co-debugging of unrelated languages and hardware targets (internal version 19th month of the project, final version 36th month of the project). Finally, a co-visualization back-plane will provide the ability to control and visualise in real-time the activity of external simulators, emulators and software tasks and the simulated circuit's properties (such as its EMI), thereby providing a framework for distributed simulation/emulation of hardware-software electronic systems together with a multi-target debugging environment (internal version 22nd month of the project, final version 37th month of the project). We will completely automate the simulation and synthesis flows for heterogeneous applications. Preliminary, unpublished, work at UNIMAN has produced a co-simulation prototype. A GALS hardware-software prototyping flow will also be provided that will target FPGA devices. This proposed GALS framework will be user-friendly for designers without experience in asynchronous design in order to ease adoption of the GALS methodology. The target is a cheap and simple design flow. Although we could have just integrated Balsa support into existing commercial frameworks, this kind of integration is unsatisfactory: proper interoperability of multiple SME and open-source tools is extremely difficult to achieve, and the subtleties of asynchronous and GALS design (such as meta-stability and pausible clocking) are complex to deal with.

Our GALS design flow will be based on an open format for mixed synchronous-asynchronous IPs

in order to consolidate asynchronous IPs dissemination and re-use (5th month of the project). The IP format will be able to describe hardware/software entities at multiple levels of abstraction in multiple languages (SystemC, C, Verilog, VHDL, Balsa, gate-level netlist etc.), with both synchronous and asynchronous interfaces. The IP format will contain enough information to transparently convert signals between varying levels of abstraction enabling: a transparent co-simulation of IPs at different levels of abstraction, the visualisation of signals at levels of abstraction independently of the simulated level of abstraction, and exploitation of transaction level structures during hardware-software co-design and visualisation. The IP-XACT IP packaging format proposed by the SPIRIT consortium satisfies most of these specifications, but does not include any support for asynchronous-specific structures. Rather than creating a new packaging format altogether, we will work towards extending the IP-XACT format, hopefully integrating these ideas in a future version of their work.

Based on this open IP packaging format, we will establish a library of the important GALS components scalable to different applications (24th month of the project). This library of GALS interface IPs should enable a plug-and-play type of approach when designing a system with a heterogeneous mixture of synchronous and asynchronous IPs. Additionally, we plan to generate a library of asynchronous IPs allowing new users to easily build a functional asynchronous or GALS system. This will be, at least in the beginning, a relatively simple library limited to basic components. However, we expect that this library will be further extended by encouraging community sharing of IPs via a website (similarly to, or in collaboration, with opencores.org). The library will include a full design support including necessary additional cells such as Mutex and Muller-C elements for the IHP CMOS process (14th month of the project). IHP design kits and fab services are already available for academic and research institutions over Europractice program. We plan to extend this support to the GALS design flow and an extended set of standard cells. During the project we will also promote the GALS methodology by organizing training events, summer schools and preparing tutorials and documentation for the tools and libraries.

We will consider challenges for establishing an effective test flow for the GALS systems. In our opinion, since the GALS design is dominated by local synchronous blocks, the test flow will be based on existing synchronous test methodology (a scan approach). For the asynchronous components, implemented we propose a limited implementation of functional tests to give sufficient test coverage (23rd month of the project).

It is planned to investigate the possibilities for lowering EMI and power with a GALS methodology. We plan to build an abstract model of the GALS circuit and generate the optimal algorithms for reducing the EMI. Additionally, the developed EMI reduction algorithms will be evaluated theoretically and in practice (20th month of the project). We will investigate application of dynamic voltage and frequency scaling in conjunction with GALS in order to reduce power in comparison with standard synchronous low-power solutions (20th month of the project).

The project also intends to deploy the power-aware nature of GALS technology to bring NoC architectures to maturity. Network-on-chip (NoC) is the candidate technology to provide scalable communication bandwidth through a modular interconnect design. The lesson learned from state-of-the-art NoC prototypes is that almost 50% of total NoC power is drained by the clock tree (clock distribution and flip-flops). Moreover, the problem of distributing the global clock in a chip with minimal clock skew is getting difficult to solve due to increases in clock frequencies, smaller feature sizes and growing design complexities, which indicates that a global timing notion will not be feasible for highly-integrated nanoscale designs. GALS technology is generally viewed to be a breakthrough technology for future system interconnect designs. GALS-based NoCs would allow the synchronous design of network nodes at their optimum clock frequency, while facilitating asynchronous communication between modules. This would reduce the timing convergence constraints during back-end physical design steps, remove the power-hungry global clock tree and pave the way for new variation-tolerant on-chip interconnection schemes. Unfortunately, although these considerations would appear to be common sense, they have not been enough to remove the barriers to the adoption of GALS interconnects due to the lack of convincing analysis and exploration frameworks, crossbenchmarking with synchronous solutions, proven robustness against nanoscale physics effects and tool support. The project intends to bridge this gap, and consolidate GALS-NoCs as the enabling technology for widespread adoption of network-centric architectures for highly integrated MPSoC platforms in the nanometer regime (31st month of the project).

B.1.1.3 ASIC implementations within the GALAXY Project

Practical IC implementations will be the key issue of the GALAXY project, as it will provide the best

way to evaluate the developed GALS solutions and compare them against traditional circuits. We plan to have two separate ASIC implementation runs within the GALAXY project.

The first chip will be specifically designed to be a test chip containing structures to evaluate GALS components(17th month of the project). As part of WP7 we will investigate the advantages of GALS-based design in reducing power consumption, reducing EMI, and improving process variation tolerance. The first chip will contain test structures that will allow us to quantify these advantages by direct measurements. Additional test structures will be included to test new library components developed in WP3. Most importantly, a set of specially designed test circuits will be developed in order to investigate scaling effects. The same test structures will be replicated in the second chip (which will use a much more aggressive technology). Comparative measurements on both chips will provide us with invaluable, and currently non-existent, data on the suitability of GALS for aggressively scaled technologies. We expect to use the IHP 130 nm technology for the first chip, as the advanced 45nm technology we plan to use for the second chip will not be fully available during the first part of the project. Using two different manufacturing technologies will also give us more reliable results for scaling effects. In addition it will allow us to explore application of GALS techniques to low-cost processes

Finally, we plan to build a complex target system using both a standard synchronous CMOS design flow and the GALS design flow developed in this project (WP3, WP4, WP5) in a cutting edge 45 nm CMOS process (32nd month of the project). First product samples in 45 nm process are announced for early 2008, full production in 09/10. For 32 nm we do not expect early samples before 2009/10. Ramp-up and technology access for our projects would not be available before 2011/12. Therefore, the most advanced process to which we can have access and actually produce chips in the time frame of the project is 45 nm. However, during the project span and particularly in the activity 7.3 (Circuit and architecture level techniques) we will investigate how further technology scaling (32 nm and beyond) will affect GALS topic. Implementing the same system using two separate methodologies (GALS and synchronous) is the only “fair” way to evaluate the GALS design flow. As mentioned earlier, this second design will also contain a set of test structures to investigate scaling effects. With this approach we will be able to estimate and show the viability of the concepts, techniques, architectures and tools developed within the project.

Selecting a suitable target platform for the second design is important. Since wireless communication is an application domain which is gaining more and more popularity and which poses significant technical challenges to system designers (performance- and power-wise), and since several group members have prior experience in this field, we will consider target platforms from this field. For example, one candidate will be an accelerator for an OFDM baseband processor with data rates up to 1 Gbps for communication systems in 60 GHz range which is currently under development in IHP [GRA07b]. Currently, the full processor integrates several Viterbi decoders, 256-FFT and IFFT, many complex interleavers/deinterleavers. We will also consider the application of GALS-enabled Network-on-a-Chip architectures (as developed in WP6) in this target system as well.

The designed chips will be the result of close cooperation between all project partners and will rely on results of several WPs. Building chips is recognised as risky, but all partners have experience in successful, right-first-time, chip design. This work will be a real challenge, but the experience of the project team, and the fact we have worked closely together in the past, gives us complete confidence this can be achieved, and that the results will confirm the initial expectations as to the real value and long-term viability of the GALS and NoC techniques.

B.1.1.4 Dissemination and exploitation of results

Our strategy for the dissemination of results is to place as much as is possible in the public domain to encourage the uptake and further development of the methodology by industry. However, necessarily some IP will remain confidential to be exploited by the project partners. The precise status of the deliverables is given in section B.1.3.4, however in general the design framework and interface definitions will be publicly available. An abbreviated guide to the status of results generated in the project is given in section B.3.2.6 Management of intellectual property.

B.1.1.5 Relevance to the Challenge 3 call topics

In this project we are targeting ICT objective 3.3: Embedded systems design. The first target of this call is "Theory and methods for system design: Methods that can increase system development productivity while achieving predictable system properties". It is quite clear that GALS techniques based on asynchronous interfaces can lead to a system design framework that will improve system

development and simplify design process. This target states that “key issues encompass heterogeneity (building embedded systems from components with different characteristics); composability; predictability of extra-functional properties such as performance and robustness (e.g. safety, security, timing and resources); concepts and tools for specifying and evaluating security properties; adaptivity for coping with uncertainty”. It is expected that a GALS methodology will become the basis for the integration of heterogeneous components (synchronous, asynchronous, components supplied from different voltages and running at different frequencies). Also a GALS methodology could be a key driver for the integration of different IP components from different vendors. Additionally, a GALS approach will increase the robustness of the system, reduce the probability metastability problems, and relax the timing of the system. GALS methodology is also quite effective in the area of secure applications since the asynchronous behaviour of GALS components disables to a significant level Differential Power Analysis (DPA) of system behaviour. Finally, in the context of this project we want to target nanoscale issues such as uncertainty and variability. It is expected in this respect that GALS techniques will also show significant improvement in comparison with classical approaches for system integration.

The second target of the call is "Suites of interoperable design tools for rapid design and prototyping". A large part of our project is dedicated to the construction of a framework able to control the interoperability of compilation, simulation and synthesis tools from SME vendors and from the open-source community. Parallel compilation and synthesis will be made possible by a dependency and file format checker, able to start tools and file conversions when appropriate. Parallel simulation will be made possible by a co-simulation backplane interfacing any number of simulators, emulators and software modules together. A co-visualization backplane merges the simulation traces, emulation feedbacks and software execution results together for efficient debugging of components from different origins. The visualization of circuit properties (such as performance, power, EMI) from multiple tools in a common view will ease circuit optimization. This framework and plug-in interfaces will be released as an open tool framework, therefore facilitating new entrants. Our GALS IP format is expected to be proposed as an extension to the standardized (synchronous) IP packaging format from the SPIRIT consortium. It should be noted that the consortium includes partners experienced in previous open-source projects and an SME whose business is dependent on tool interoperability.

B.1.2 PROGRESS BEYOND THE STATE OF THE ART

B.1.2.1 GALS design as a system integration solution

System on Chip (SoC) integration imposes a number of technical challenges on designers and tools. There are further difficulties for a SoC implementation in the area of wireless communication systems. The methods and tools for reducing power consumption and minimizing crosstalk between analog and digital parts of the system are very limited and often inefficient.

Many of the challenges are associated with the design of the clock network in digital systems. Clock skew appears to be a severe bottleneck for complex digital circuits. The synchronous transitions of the clock lines are a strong source of noise and electro-magnetic interference (EMI). Additionally, the power spent just running the clock tree is comparable to the power consumed in the functional blocks of the system. It is conceivable to conclude that splitting a complex digital system into several independent subsystems, will relax problems significantly. Dealing with smaller blocks is much simpler, and power saving techniques could be more successfully applied. Crosstalk and EMI are suppressed due to the uncorrelated operation of the autonomous blocks. However, synchronisation between blocks operating at different speeds could be very complicated.

Several existing approaches address the problem of block partitioning and data synchronisation between independent blocks. Some of them are used to deal with increased power consumption and EMI. Today, these techniques are mainly referred to as Globally Asynchronous Locally Synchronous (GALS) methods. Many of them are not generally applicable. However, some of the techniques are currently used in design practice. Choosing between different proposed strategies depends very much on the particular system architecture.

GALS systems have a unique structure that is similar for all the different proposals. The principle architecture of GALS for point to point dataflow structures is given in Figure 1. The basic GALS paradigm is based on a system composed of number of synchronous blocks designed in a traditional way. However, it is assumed that clocks of such synchronous systems are not necessarily correlated and consequently that those synchronous systems communicate asynchronously using handshake channels. Locally synchronous modules are usually surrounded by asynchronous wrappers providing such inter-block data transfer. The principle architecture of GALS for point to point dataflow structures is given in Figure 1. Practical GALS implementations may form much more complex structures, such as bus or NoC structures for inter-block communications and use different data synchronization mechanisms, but all proposals are based on the simple structure shown in Figure1.

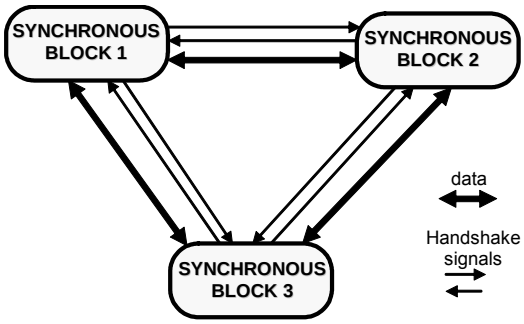

Figure 1. GALS architecture

GALS as a technique was mentioned for the first time in [CHAP84]. This work gives the fundamental basis of globally asynchronous locally synchronous systems. Many years after the first proposal, the GALS idea was reactivated and a working architecture was described in [YUN96]. Following that, there has been revived interest in the GALS idea which has continued to increase until today.

The major differentiator between the different GALS techniques is the strategy used to safely transfer data between the locally synchronous blocks and avoid metastability. In principle, a GALS approach can be implemented in three different ways: using pausible clocking, boundary synchronization or FIFO-like interface structure.

B.1.2.1.1 GALS with pausible clocking

Many GALS systems presented in the last few years are based on pausible (or stretchable) clocking [MUT00, KRS06, ZHU02, MOO02]. This GALS method relies on the application of the local clocks that drive synchronous circuit blocks. In this case, stoppable ring oscillators are used to generate the local clocks. The strategy to avoid metastability is very simple. All local clocks for the blocks involved in a single data transfer are stopped until data is transferred. Therefore, the asynchronous wrappers are performing all necessary activities for safe data transfer between the blocks. A general structure of the typical GALS system with pausible clocks is shown in Figure 2. The asynchronous wrapper contains input and output ports that perform the handshake process between the LS modules and it generates a stretch signal for stopping the activity of both clocks. The basic GALS proposal focused on point-to-point communication between blocks. However, as shown in [VIL03] the idea can also be extended to more advanced solutions that support bus or crossbar structures for data communication.

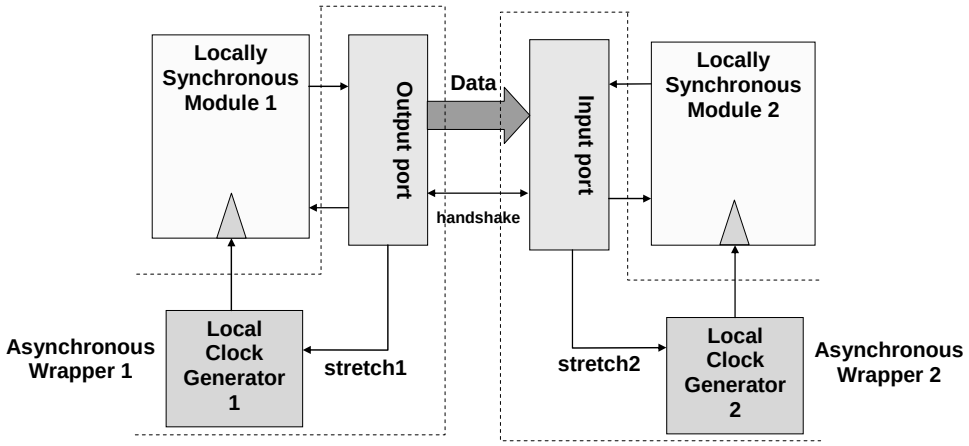

Figure 2. Block diagram of a GALS system with pausible clocking

B.1.2.1.2 GALS based on the boundary synchronization

To avoid metastability and to perform safe data transfer between asynchronously communicating blocks, it is possible to implement synchronisation mechanisms. Many of these schemes are already known and have been successfully used for decades. For example it is possible to use two-flop synchronisers or one-flop synchronisers [GIN03]. As an alternative, the adaptive synchronisation techniques [KOL98] could be used for mesochronous systems. However, this approach does not offer any power saving mechanism and introduces a relatively large hardware overhead, because a separate delay line is needed for every single data line. Also, the time overhead needed for statistical analysis of the data could be important. The problem of mesochronous system integration can be also addressed with application of an adaptive predictive synchroniser [FRA04]. In this case, the synchronisation latency is smaller than one clock cycle.

Another interesting approach is concept of locally delayed latching [DOB04]. This is a complete GALS solution with the set of the synchronizing registers at the boundaries of the synchronous blocks. The major disadvantage of this architecture is that the data cannot be transferred every clock cycle due to the synchronous handshake that is performed at the boundaries of the synchronous part of the output port. Actually, one data transfer usually needs several clock cycles. This property of the proposed architecture restricts the application of the proposed circuitry to low speed data-transfer applications.

B.1.2.1.3 FIFO-based GALS solutions

While designing GALS systems it also possible to interface blocks with specially designed asynchronous FIFO buffers as described in [CHAK03, CHE00, BEI06]. With this approach, the hardware redundancy of the FIFO is hiding the problem of the synchronisation in the system. FIFO-based GALS systems can tolerate very large interconnect delays and are quite robust with regard to metastabillity. This type of interface can be used not only for interconnection of heterogeneous (asynchronous and synchronous) systems, but also for classical synchronous-synchronous and asynchronous-asynchronous connections. Practical results confirmed that an acceptable data

throughput via such an interface can be achieved [CHE00]. The advantage of this GALS approach is that the operation of the locally synchronous module is not affected by synchronisation. However, for very wide interconnect data buses, FIFO-based GALS structures could be very expensive in terms of area. Also, the introduced latency might be significant and possibly not acceptable for some applications.

Alternatively, a GALS system can be based on a classical FIFO design using gray code. In [BEI06] such an interface is presented for the specific case of an Asynchronous Network on Chip (NoC) system. In this work, the compatibility with existing design solutions has been retained which has allowed the utilization of standard CAD tools. However, some price is paid with some performance degradation and a suboptimal architecture.

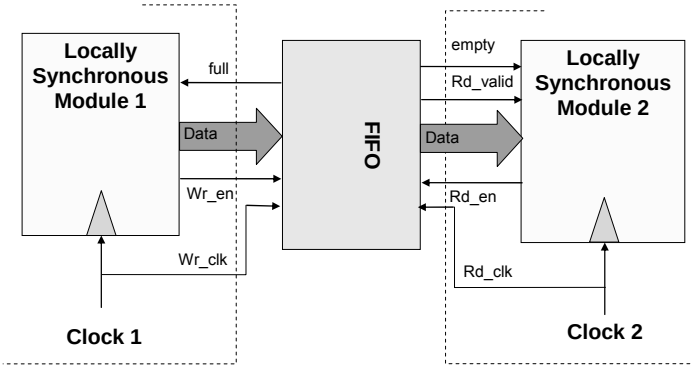

Figure 3. Typical FIFO-based GALS system

B.1.2.2 Patent search on GALS

In the previous section we introduced several architectures for GALS chip interconnect. However, most of them are developed at academies and not legally protected with patent rights. According to our knowledge, there are only few patent applications directly dealing with GALS interconnects. Two patents are submitted from Philips [CHO05, KES04], one dealing with ring-oscillator calibration and the other with "mouse-trap" pipeline synchronization. Additionally, there is a patent from University Rochester [ALB04] about GALS microprocessor. However, none of those patents are affecting significantly the work that we want to perform within the GALAXY project. Two additional patent applications are submitted from IHP [KRS04, GRA07], dealing with IHP-developed request-driven GALS technique and possibilities for EMI reduction with GALS interconnect. The circuits and methods covered by those two IHP patents may be utilized in the framework of this project and made available for non-commercial application. However, a commercial exploitation of those IHP proprietary patents is subject to licensing.

B.1.2.3 Applicability and possible problems with state-of-the art GALS design

Although GALS systems still have a great popularity among the scientific community they are not very frequently used in the commercial systems. There are different reasons for that, and our project aims to overcome those issues and offer effective solutions for a GALS design flow.

GALS is already confirmed as a powerful vehicle for improving system integration. It is clear that by partitioning a complex synchronous system into a number of the independent subsystems we can immediately profit from reduced clock skew, simpler clock tree, and easier timing closure. Eventually, this should result in a shorter design process and improved time-to-market of the product. However, there are still some challenges that must be resolved before the GALS design is established as a main-stream design technique.

In the previous subsection we have introduced three main GALS strategies. Each of them has its own properties and there is a certain price to be paid for the system integration improvement offered by any of them. In general, the designer must make a trade-off depending on IP blocks and communication requirements of the application, and choose the methodology that is most suitable. Three main parameters can be affected by this choice: latency, throughput and area [SCO07]. Generally, in the case of the boundary synchronization a major price is paid with reduced data throughput. For the FIFO-based GALS, throughput is preserved but for some applications increased data latency can be unacceptable. GALS with pausible clocking, on the other hand, introduces very

low latency but the performance loss can be significant.

One of the issues that has slowed the practical adoption of the GALS methodology is that of debugging and test flows. The classical synchronous design methodology is well supported by a number of very mature CAD tools which are constantly being improved. Commercial CAD tools (with the sole exception of asynchronous CAD provider Handshake Solutions [HS]) do not support asynchronous design. Consequently, the asynchronous design technique is followed by tools developed in academia. Such tools are usually uncoordinated, incomplete and their improvement is erratic – although the Balsa system at the University of Manchester has synthesised a complete ARM compatible processor core [PLA03]. Therefore, many steps in the design process for asynchronous circuits are still manual and there is no consistent design flow from behavioural modelling to tape-out of the circuit. For GALS systems the situation can be even worse. Although for synchronous parts of the system the support from standard tools can be used, there is no support either on the synchronous or on the asynchronous side for the mixed asynchronous-synchronous behaviour. On top of this, additional library cells such as C-elements, mutual exclusion elements, programmable delay lines or even complete handshake circuitry, need to be developed for an asynchronous design flow. A recent problem, with the advent of system level design environments using IP blocks. is the absence of a specification format for asynchronous IPs. This means that these new system level tools are unable to handle asynchronous circuits unless they are provided inside a synchronous wrapper, which would deprive them from most of the benefits obtained through an asynchronous design style. This situation contributes to the absence of asynchronous IP libraries and GALS interface libraries, which is currently the main driver in synchronous developments.

A similar problem appears with the test flow. The usual test-flow for synchronous circuits is based on the application of well-known scan-chains that can be used to control and observe all sequential elements within a design. The scan-chain approach requires a centralized clock, which is not available in standard asynchronous circuits. There are some solutions which offer a similar approach for asynchronous circuits [BER02]. However, there is significant overhead involved in such solutions. There has been some research on the test-flow for the GALS circuits. One approach is to use functional test for the asynchronous part of the system [GUR02]. Alternatively, BIST approach can be used as presented in [KRS05b]. Another problem in testing is the non-cycle accurate behaviour of some asynchronous designs. The responses of an asynchronous circuit under test may not be aligned with the test clock cycles of the automated test equipment. This can be a when mutual exclusion circuits for arbitration are used. In this case, the application of the usual hardware testers is limited due to their strictly cycle based non-reactive nature.

Most digital designers have experience limited to synchronous design. Asynchronous and GALS designs have their own properties sometimes not easily adoptable by a synchronous designer. The asynchronous interfaces frequently request small but non-standard modifications of the locally synchronous blocks.

GALS solutions based on the pausible clocking usually imply the application of ring oscillators. A ring oscillator is usually composed of an inverter chain. This structure naturally leads to the susceptibility to PVT (Process, Voltage, Temperature) variations. In many cases this property is in fact useful, since the PVT variation in the clock generator, which is located close to the actual circuit, will follow the PVT changes of the circuit as well. The application of the ring oscillators is particularly well suited for dynamic frequency scaling (DFS) in order to reduce the power consumption. On the other hand, for applications that require strict and accurate clocking of the system (as for communication systems), sensitivity to PVT introduces the need for delay line calibration as proposed in [MOO00]. Additionally, significant power is needed to run the ring oscillators.

Handshake solutions [HS] has recently released a clockless multilayer AMBA Advanced High-performance Bus (AHB). The new interconnect is a clockless implementation of the well-known multilayer ARM AMBA AHB — an interconnect scheme that enables parallel access paths between multiple masters and slaves. Although this product seems to confirm that power and EMI improvements can be expected by leveraging clockless technology, it is still far from providing a scalable solution to the problem of on-chip communication. In fact, the clockless multilayer AHB is aimed at medium performance applications. It is particularly well-suited to event- or interrupt-driven applications where its instant response and zero standby power consumption are particularly useful. However, the newly released clockless interconnect still relies on multi-layer architectural solutions that are well known to have severe scalability limitations. Our project aims at coupling the benefits of a scalable interconnect fabric (Networks-on-chip) with those of GALS design techniques.

B.1.2.3.1 Power Saving with GALS

Power saving was always considered an inherent property of asynchronous design. Therefore, the expectations from GALS designs were always very high. On the other hand, most of the practical GALS demonstrators have showed only marginal improvement in this direction. For example, the GALS baseband processor for WLAN [KRS06] showed an improvement of only 1% in comparison to the respective synchronous chip.

In retrospect, it is easy to understand this result. The inherent power reduction obtained by using a GALS-based system is essentially based on the same paradigm as the low-power techniques for synchronous circuits: trigger the locally synchronous block only when it is needed and lower the switching activity to minimum. Therefore, the achieved results are very similar.

We can expect more if the GALS approach is applied in conjunction with voltage and frequency scaling. GALS architecture is very well suited for such technique since the mutual communication between blocks is asynchronous. The boundaries of the GALS blocks are defined and the partitioning naturally leads to a hierarchical layout process. Therefore, the introduction of different power rings in the layout and insertion of DC-DC converters are easier. Theoretical investigations presented in [TAL05] show that even for GALS-based high-performance processors, which are generally not very suitable for GALS implementations, an average energy reduction of up to 33% can be obtained with only a slight performance drop of 10%.

B.1.2.3.2 EMI reduction with GALS

Another very important property of GALS designs is the reduction of electro-magnetic interference (EMI). It has been several times demonstrated that asynchronous circuits expose significantly lower level of EMI than their synchronous counterparts. One example is shown in Fig. 4 which compares the Amulet 2 asynchronous processor with an ARM9 [FUR99]. However, we believe that this property has not yet been completely explored in GALS systems. Lowering the noise generated from the digital part of the system is an important issue of complex SoC (System on Chip) integration. We have performed an initial simple study and the results are published in [GRA05]. The results, given there and shown in Figure 5, show the possibility of reducing the noise spectral components on the power supply line up to 20 dB in comparison with synchronous design. Additionally, reduction of the noise peaks can be expected up to 40%. The practical measurement given in [KRS05a, KRS06] shows lower values (5 dB) achieved in reducing the EMI. However, there is a great research opportunity in generating a reliable noise model and effective algorithms for lowering the EMI.

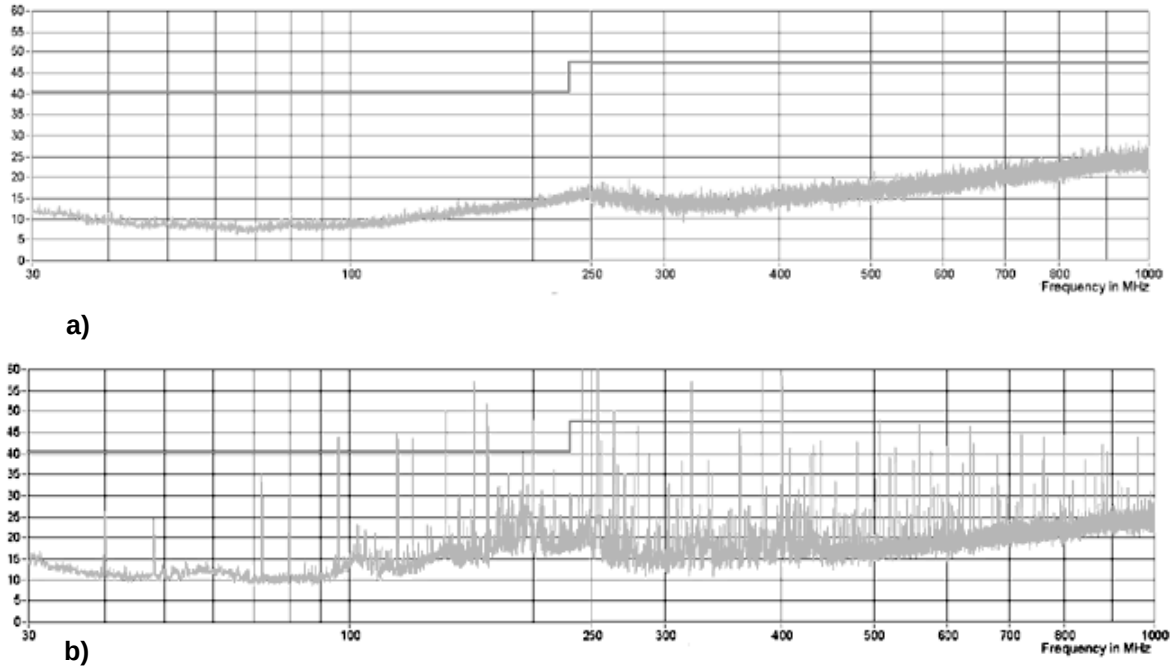

Figure 4. Comparing EMI of async. Amulet 2 (a) and compatible sync. ARM9 processor (b)

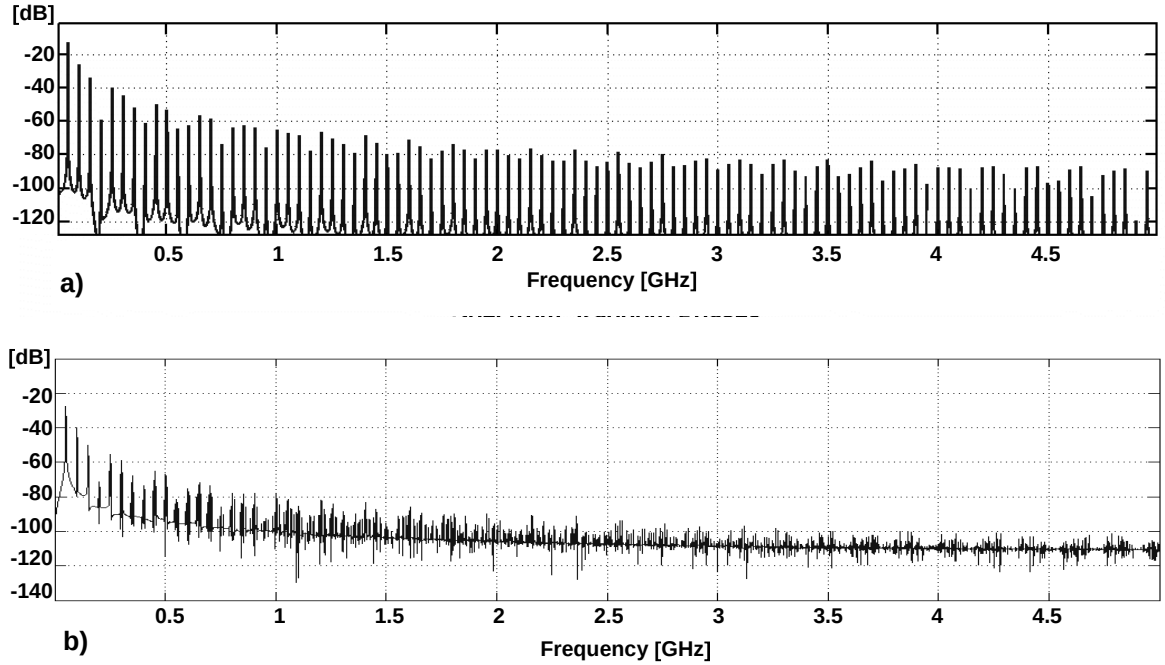

Figure 5. Power supply line spectrum of the synchronous (a) and GALS system (b)

This property can be also very useful for security application. GALS circuits have the potential to increased immunity toward Differential Power Analysis (DPA) attacks [GUR05]. The power spectrum of an asynchronous circuit does not contain large peaks at multiples of a global clock frequency and therefore is expected to present potential attackers with less information about the circuit operation. Furthermore, due to their asynchronous components GALS chips are less controllable and their timing is more non-deterministic. This is a very important feature for smart-card applications.

B.1.2.3.3 GALS and Networks on Chip (NoC)

The ENIAC strategic research agenda points out that in the "More Moore" domain, although transistor performance will continue increasing, the performance of the interconnection network is not expected to match this progress. Employing totally self-timed techniques for the interconnect is a promising means to tackle a number of on-chip interconnection issues, from power and EMI reduction to clock skew management, and modularity of design. However, only a few proposals for an asynchronous NoC have been published so far. This section gives an overview of the state-of-the-art research in asynchronous on-chip networks. The typical NoC architecture is illustrated in Fig. 6.

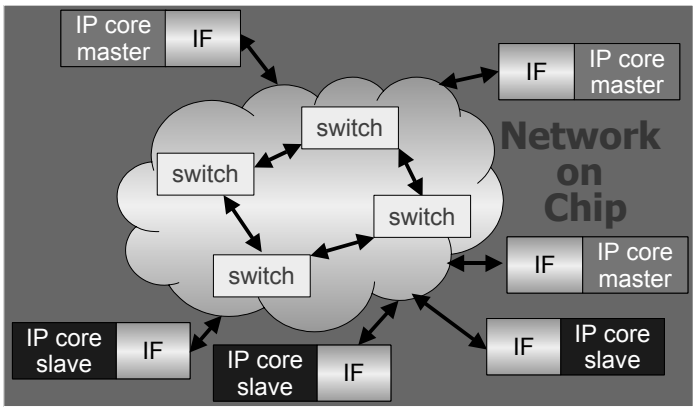

Figure 6. Typical NoC architecture

The CHAIN network [BAI02], developed at the University of Manchester, is interesting in that it is implemented entirely using asynchronous, or *clockless*, circuit techniques. It makes use of delay insensitive 1-of-4 encoding, and source routed BE (Best Effort) packets. An easy adaptation along a path consisting of links of different bit widths is supported. CHAIN is targeted for heterogeneous low power systems, in which the network is system specific. It has been implemented in a smart card,

which benefits from the low idle power capabilities of asynchronous circuits. Work from the group involved with CHAIN concerns prioritization in asynchronous networks. In [FEL03] an asynchronous low latency arbiter was presented, and its use in providing differentiated communication services in SoC was discussed, and in [FEL04] a router implementing the scheme was described.

NEXUS is another asynchronous on-chip network developed at Fulcrum Microsystems, USA [NEX04]. Their approach is based on a 16-port, 36-bit asynchronous crossbar that connects synchronous modules through asynchronous channels and clock-domain converters. Nexus is a quasi-delay-insensitive (QDI) on-chip interconnect infrastructure using one-of-four encoding and precharge domino logic. It also supports a split transaction protocol with a request burst going out and a completion burst returning.

Liljeberg et al., from the University of Turku, Finland, propose a self-timed ring architecture as a replacement for on-chip buses [LIL03]. They implemented a 12-stage bi-directional ring network with 36 pipeline sections. The network employs a two-phase signaling protocol between stages to accommodate relatively long wire segments with fewer transitions within a transaction cycle, and a four-phase signalling protocol for internal control within a stage to enable the design of fast and relatively simple control logic circuitry. The data path is encoded using a standard single-encoding scheme.

The MANGO network (*Message-passing Asynchronous Network-on-chip providing Guaranteed services over OCP interfaces*), developed at the Technical University of Denmark, is another clockless NoC, targeted for coarse-grained GALS-type SoC. MANGO provides connection-less BE routing as well as connection-oriented guaranteed services (GS) [BJE05a]. In order to make for a simple design, the routers implement virtual channels (VCs) as separate physical buffers. GS connections are established by allocating a sequence of VCs through the network. While the routers themselves are implemented using area efficient bundled-data circuits, the links implement delay insensitive signal encoding. Network adapters provide OCP-based standard socket interfaces, based on the primitive routing services of the network [BJE05]. This includes support for interrupts, based on virtual wires. The adapters also synchronize the clocked OCP interfaces to the clockless network.

A network-on-chip architecture, called ANOC, has been proposed by Beigné et al.[BEI05], which provides low-latency services. The methodology used to design the node is based on Quasi-Delay-Insensitive circuit designs. A 4-phase protocol handshaking is used for asynchronous channels, associated to a WCHB protocol for pipeline stages. Data are encoded using an n-rail code. The on-chip network interfaces are discussed in [BEI06]: they do not just handle resynchronization between synchronous and asynchronous NoC domains, but also implement NoC communication priorities and are adapted to standard implementation tools. Interestingly, a complete multi-level design framework has been developed to address the modeling challenges.

Some contributions from the open literature focus on specific network building blocks. The QNoC router designed at Technion [DOB05] features fully asynchronous implementation and supports multi-service levels, thus targeting quality-of-service provisioning. A comparison with a synchronous router also indicates that the asynchronous variant requires less area while delivering comparable data rates.

Finally, much research effort is being devoted to the electrical-level design of asynchronous links [ISO06, VIV07]. The focus is on delay-insensitivity through proper encoding techniques (e.g. dual-rail, m-of-n, Berger code), variation-tolerance, transceiver-circuits and signaling techniques.

While much research is being undertaken, there are not many demonstrations of clockless NoCs in real applications. A small, source-routed NoC for a commercial DSP audio chip is presented in [DSP06].

A working chip, called FLEETzero, to test an asynchronous switch fabric is described in [FLE01]. The switch fabric transports 8-bit data items from any of eight sources to any of eight destinations. Finally, the smart-card implementation of the CHAIN clockless network has already been discussed [PLA02].

A number of challenges lie ahead to make GALS-based NoC technology become mainstream.

Most current NoC technology assumes that on-chip logic and wires are reliable. In the best case, it is tolerant to delay variations, but it is not designed to recover from logic faults, failures or to deal with communication errors. Nanoscale technologies force a design paradigm shift, wherein fault tolerance becomes a requirement for all on-chip functions, including interconnect. Interconnect could be made fault-tolerant by building redundancy into the fabric, but it is likely to be more cost-effective to

implement error detection and retry capabilities. Another technology-related issue concerns the impact of process, supply voltage and temperature variations on the performance and reliability of long on-chip links. These variations cause the signal propagation delay through interconnects to be uncertain which in turn affects the performance and reliability of the system significantly. Fault-tolerance and process variation-immunity are two explicit objectives of this project.

Moreover, while GALS schemes provide more independence between system IP blocks, in that the overall performance need not be determined by the slowest stage, they may exhibit meta-stability, thus resulting in potentially unpredictable performance. When it comes to truly asynchronous NoCs, on one hand, they exhibit promising power and performance metrics, but on the other hand they are often less efficient in terms of area, due to the lack of established logic optimization tools for asynchronous gate-level netlists.

Even the early design steps of GALS-based networks are not yet supported by mature synthesis tools. This is key to industrial interest for this kind of solution, which is currently mostly pushed by academia in spite of the widely acknowledged potential benefits. A significant evolution of design technology for GALS systems is expected from this project.

Finally, until now all implementation examples of GALS NoCs have been limited to low-end systems and are not available in both synchronous and asynchronous variants for comparison. Hence, they are not really able to make the case for clockless NoC design. Our project targets an explicit crossbenchmarking activity between synchronous and GALS communication architectures and explores GALS interconnect design for a high-end wireless communication system.

In general, while progress in clocking structures within NoCs continues in the short term (e.g. advanced backend synthesis tools, aggressive clock-gating), this project aims at proving that a complete paradigm shift would ensure significant advantages and at making such advantages available for real-chip realizations.

B.1.2.4 GALS design improvements within the project

As described in the previous subsections, there are different GALS architectures available and there is a variety of applications where GALS can be used. In the research community most practical realizations were based on pausible clocking and the majority of theoretical work was published on applications orientated towards high-performance CPUs. We believe that that there are other implementation methods and application fields that need to be considered as well. Therefore, during the project time we plan to evaluate different GALS techniques and their applicability. As a result of this, we want to propose certain improved GALS architectures. We plan also to optimize and standardize the interfaces in order to relax the design efforts when introducing GALS design. The industry is going in the similar direction. For example, Handshake Solutions have recently announced their new product clockless HTmAHP interconnect compliant to ARM AMBA AHP protocol [HS]. This product is suitable only for the compliant systems and its runs up to the moderate 100 MHz speed. Additionally, this product is available only to HS customers and it is not open source.

The major roadblock that is stopping broader uptake of GALS within commercial applications is the design flow. In this respect we plan to facilitate the development of new mixed synchronous-asynchronous design flows by developing a framework able to coordinate the multiple tools various vendors and universities. This interoperability framework is primarily based on a co-simulation and co-visualization architecture, and will also include synthesis and layout flows. Asynchronous descriptions will be based on the existing Balsa language and simulation/synthesis flow developed at the University of Manchester and widely recognized by the asynchronous community. The other usual design languages (Verilog, VHDL, SystemC, etc.) will be supported at the system level, making it possible to model heterogeneous GALS systems in a single environment providing a suitable layout flow. The primary interoperability layer is a co-simulation backplane with plug-in system and a well-specified interface to which any simulator or emulator can be attached. This backplane will allow the co-simulation of mixed languages (especially of those asynchronous languages unsupported in traditional CAD simulation tools), mixed vendors, mixed levels of abstraction, and mixed targets (such as the co-simulation between a Verilog test harness and a software module running on an emulator board). The ability of the framework to coordinate various simulators will also enable, without any additional effort, multiple instances of the same simulator to run simultaneously on different parts of the system. This will therefore allow distributed simulations over clusters of computers. Preliminary work at UNIMAN has established the feasibility of this approach [JAN07].

The co-simulation backplane will be attached to a co-visualization environment able to merge the

information processed by the various tools in a common graphical representation, ideal for debugging large-scale system level designs. The synthesis will be controlled by the framework to handle heterogeneous GALS flows and the process will be completed by including asynchronous components in traditional synchronous net-lists able to be handled by traditional layout tools.

Test flow improvements will be carefully considered. We anticipate building a test model for GALS systems as the combination of a standard scan approach for locally synchronous blocks and functional or BIST test for the asynchronous components. However, we have to generate the fault model of asynchronous wrappers and to estimate the fault coverage of the generated tests to confirm the suggested approach. The goal is to reach the fault coverage for asynchronous wrappers comparable with the coverage of the synchronous part generated with scan methods. We will also try to propose suitable methods for functional testing the GALS systems in the classical hardware tester environment, and to overcome the problem of non-determinism.

In the previous subsection we have already suggested dynamic frequency and voltage scaling as the best option for power saving with GALS. However, until now there were no measurement results confirming this advantage. We want to model a GALS system and to investigate the possible power saving with GALS on for a typical low-power application (for example in the area of mobile communication systems).

The most promising feature of GALS can be EMI reduction. The members of consortium have done some initial research work in this direction [GRA05]. However, the developed MATLAB model is too simplified and it needs to be scalable to any GALS system and to be usable for EMI estimation at a behavioural level for any GALS system. It is already clear that the level of EMI reduction is dependant on switching scenario among the GALS blocks. We want to develop the suitable algorithms and mechanisms that will enable us to maximize the EMI reduction. Additionally, we want to explore the possibilities for estimating EMI on the RTL and gate level using the standard CAD tools such as Synopsys PrimePower. All results will be verified with the measurement on the fabricated complex GALS chip.

As regards GALS application to networks-on-chip, this project will make available a number of architectural solutions (from conservative mesochronous clocking to fully independent clock domains, from architecture variants where the links are the only asynchronous elements to those where the whole communication infrastructure is asynchronous) meeting the requirements of a large number of hardware platforms. Several GALS interfaces will be employed in the NoC context (e.g., pausible clocking, mixed-clock FIFOs) and will be analyzed from a performance, area and power viewpoint.

Moreover, architecture-level techniques as well as proper backend synthesis methodologies will be devised to account for the effects of nanoscale physics. Process variability is the most important one because it has a direct negative impact on yield and large impact on all characteristics of the system. Above all, it might locally jeopardize expected performance. We will also show how the use of NoCs helps designers to overcome the reliability issues of future technologies. On one hand, making NoCs themselves fault tolerant can be accomplished through link-level or end-to-end error detecting/correcting coding schemes. On the other hand, low-power techniques might be combined with communication reliability ones to come up with energy-efficient and reliable communication schemes. The full potentials of dynamic voltage and frequency scaling in the context of GALS-enabled NoC designs will also be explored, thus cutting down on the significant power overhead incurred by state-of-the-art NoC prototypes. In the nanometer regime, leakage power becomes a serious concern as well, and we will devise network building block architectures and synthesis methodologies able to address this problem and to effectively span the power-performance trade-off. Lastly, we will create a link between high-level tooling for GALS-based system design and the NoC backend synthesis flow, thus creating with a complete automated synthesis flow for GALS NoCs.

All architectural explorations will be based on a virtual platform, allowing accurate system-level functional simulation, and a mature synchronous NoC architecture (called xpipes) will serve as the reference infrastructure for migration to the GALS paradigm.

This modelling and simulation environment will also allow addressing the lack of real design examples that confirm proof of GALS concepts and methods and show the effectiveness of GALS. In this project we want to design a complex GALS system for the high-end communication application with supporting datarates up to 1 Gbps [GRA07b]. The purpose of this system implementation should be evaluation of the proposed novel GALS design flow, but also exploration of the GALS interfaces, and power and EMI reduction possibilities. To properly address this we will, in parallel, implement the purely synchronous version of the same system.

Until now there have been only relatively few complex GALS demonstrators developed, such as the WLAN baseband processor from IHP (0.25um CMOS) [KRS06], the FAUST processor developed at LETI (0.13um CMOS) [LAT07] and circuits fabricated in GALS group at ETHZ (0.25um CMOS) [GUR06]. We have to emphasise that this GALS system implementation is not the ultimate goal of the GALAXY project. We regard the GALS system implementation in this project a necessary vehicle to evaluate achieved improvements in the GALS design flow and architecture. However, the planned GALAXY GALS chip implementation will definitely have many competitive features in comparison with the previous approaches.

One of the key issues of the GALAXY project will be the possibility to explore GALS solutions in a deep submicron process environment provided from Infineon Technologies. GALS techniques are presumed to be the right answer for complex nanoscale system integration. However, until now there have been no GALS chips designed with processes beyond 130 nm. We want to explore the effectiveness of GALS approaches to deep sub-micron processes: this has not been covered in any work until now. Therefore, our approach will provide completely different additional merits to the GALS subject. In the context of GALAXY project we plan also improvements and optimization of NoC nodes. The planned application in our case (1 Gbit/s with OFDM scheme) seems to be very challenging because of its ad-hoc architecture with very demanding processing requirements.

The last, but very important activity of this project is the popularization of the GALS design techniques. One way is, of course, publication of the project results in eminent conferences and journals. However, we plan also to establish a project web-site and to make results, IP libraries, source code for GALS interfaces and CAD tools available for the users free of charge. In addition to that, we will establish university program that will enable students to easily get used to the asynchronous and GALS design flow. In addition to that industrial exploitation of project results will increase the impact of the project and lead to improved competitiveness of EU companies involved in the project.

B.1.2.5 Baseline of the project

As stated in the previous subsections, GALS techniques, regardless of their great potential, have not been frequently used in commercial applications. On the research side, there have been a number of effective GALS architectures proposed for ad-hoc and NoC applications. Some GALS circuits have already been implemented and tested using industrially relevant applications [GUR06, KRS06, LAT07]. Although great research effort has been done, there are still some remaining open questions and issues, which has hindered the wide-spread adoption of GALS techniques in commercial applications. Those issues are:

- **GALS Design Flow:** While the design flow for synchronous circuits is well supported by EDA companies, the asynchronous design flow is mainly based on a number of university tools and one major commercial asynchronous CAD provider [HS]. CAD support for GALS designs which require solutions for the interaction between asynchronous and synchronous components is in an even poorer state. For example, there is no framework for co-simulation of asynchronous and synchronous components, since synchronous tools support just synchronous components and, similarly, tools dedicated to asynchronous design provide no support to the classical synchronous design. Generation of a GALS design framework will allow us to define an effective GALS design flow, which is not possible at the moment.
- **Availability of Standard GALS Libraries:** Some of the classical reservations around the asynchronous/GALS approach are that it is "complicated", "ineffective" or "unreliable". The acceptance of asynchronous design methods and particularly GALS-based solutions is significantly reduced as it is extremely difficult to generate or acquire necessary support including: GALS CAD tools, asynchronous IP cores, additional asynchronous standard cells (Mutex, C-element, etc.), and practical tutorials on asynchronous and GALS design methodologies. The generation of a library that contains all those critical building blocks for a successful GALS system would increase the exploitation potentials of the GALS methodology by a larger margin.
- **Reliable Local Clock Generators:** Many current GALS approaches are based on pausible clocking [MUT00, KRS06, ZHU02, MOO02]. Some initial work on calibration of the pausible clock generators is given in [MOO00]. However, the problem how to simply and effectively control pausible clocks has remained unsolved up to now. Additionally, the control of clock jitter in such clock generators was never addressed so far.

- **Exploiting Benefits of GALS:** Research over the last decade has repeatedly shown that GALS has several superior properties when compared to the standard synchronous approach. Several papers have investigated the advantages of the GALS methodology in terms of power consumption and EMI reduction. However, experimental results were below expectations. Power reduction was frequently achieved at the cost of reduced performance. Some theoretical investigations indicated greater potential for power reduction for systems that combined GALS with dynamic frequency and voltage scaling (DVS). The estimated numbers claim up to 33% of energy saving with a slight performance drop of 10% [TAL05]. However, DVS was never proven in practice in conjunction with GALS. Similarly, according to the first theoretical estimations GALS-based systems would reduce EMI by 20 dB. The maximum reduction measured in practice was, however, much lower, at around 5 dB [KRS06]. These two examples clearly show that the current state is far from the theoretical maximum and better implementations as well as more experiments are needed to evaluate the benefits of GALS systems in practice.

Recently, Networks on Chip (NoC) has emerged as one of the important techniques to develop complex System on Chip designs. There are many parallels between the design approach of GALS systems and NoCs and NOcs are generally accepted as a great application for GALS systems. The University Bologna, being one of the leaders in NoC design, has developed a mature, fully synchronous Network-on-Chip architecture named “xpipes” [BEN05]. Their technology offers a state-of-the-art NoC architecture with an aggregate bandwidth of more than 150 GByte/s in a 5x3 mesh topology, with 32-bit links and operating at a clock frequency of 885 MHz. An equivalent state-of-the-art system interconnect for the same communication requirements does not exceed 30 Gbyte/s (32-bit links, 400 MHz maximum operating frequency) [ANG06]. xpipes switches implement 1 output queue for each output port, each consisting of 8 32-bit words. Xpipes has also been used as an exploration platform to shed light on the intricacies of interconnect design and implementation in aggressively scaled technologies (up to 65nm) and on the trade-offs that next-generation back-ends imply [PUL07]. Among other things, it has been showed that the clock tree accounts for more than 50% of the total interconnect power, thus pointing out a critical issue of all synchronous interconnect implementations [BER06]. Although some GALS NoC approaches already exist, it was never systematically evaluated what GALS methodology can bring to the NoC design process. In the context of this project, we will try to show superior properties of the GALS NoC approach, by introducing GALS techniques in xpipes and then crossbenchmarking synchronous and GALS xpipes.

In the last few years several GALS circuits have been fabricated. While several author suggested GALS as an efficient method for designing very complex submicron systems, so far all experimental GALS systems were medium scale designs of at most 3 million gate equivalents and were never designed using a process more advanced then 130 nm. Digital circuits of this complexity can also successfully developed by using standard synchronous methods without much difficulty. In addition, some effects, such as process variability and reliability, become visible using very advanced process technologies. Therefore, until now it is not clear to which extent GALS can address such challenges. Implementing a complex GALS and an equivalent synchronous circuit in a state-of-the-art 45 nm CMOS process will certainly give a better view on GALS properties in cutting-edge technologies. This will give us the opportunity to compare design processes in terms of system integration, but also to evaluate properties of the fabricated GALS and the synchronous chip.

The motivation for the GALAXY project is to remove all barriers for commercial GALS application.

B.1.2.6 Performance/research indicators

The main point of the project is to demonstrate superior properties of the GALS approach in comparison with state-of-the-art low-cost synchronous approaches. As definition of success for the GALAXY project, the following criteria and "performance/ research indicators" have to be reached:

- Development of the software needed to establish an interoperability framework between existing open and commercial tools. The measurable criteria for this will be ability for co-simulation and visualisation of heterogonous systems described using Balsa (for asynchronous part) and standard languages such as Verilog, SystemC and VHDL (for synchronous part).
- Improve the current methodology for calibration and jitter control for pausible clocking in NoC applications. The measurable criteria for this will be a precision in clock calibration, possibilities for a jitter setting and complexity of suggested approach.
- Demonstration of the superior properties of the GALS methodology in comparison to the state-

of-the-art synchronous solutions in practice. The main parameters to confirm this are the power consumption, EMI reduction and immunity against process variation.

- Demonstration of the superior properties of a GALS NoC node in comparison with a synchronous one. The main parameters to confirm this are the power consumption, speed, QoS, latency, data throughput, and needed hardware resources.
- Demonstration of the superior performance of the GALS design process and design flow for medium-performance high-complexity digital systems with low-time to market. The main parameters for comparison are design time, number of design iterations, achieved clock skew, complexity and performance of the fabricated GALS and synchronous system. Those parameters must be extracted from measurements performed on implemented GALS and synchronous system with the same functionality.

It is expected that fulfilment of those parameters will lead to the great impact of project results and excellent chances for the commercial exploitation of the deliverables and GALS concept in general.

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B.1.3 S/T METHODOLOGY AND ASSOCIATED WORK PLAN

B.1.3.1 Overall strategy and general description

GALAXY project is planned to run for 36 months. The work performed in the framework of this project is organized in nine different work packages with expected significant synergy between them. Four major activities are covered by the planned work packages.

First activity is management and dissemination that will be covered for the whole duration of the project. In this context we have foreseen technical and administrative management activities and all activities directed to creation of impact of the project results.

Second activity is dedicated to analysis, optimization and evaluation of GALS methods and architectures. Those activities will be covered in WP2, WP6 and WP7. Work package 2 (GALS Interface Evaluation and Application Scenario) is planned as introductory activity where we plan to analyze, evaluate and possibly optimize the existing GALS interfaces. This WP is planned to be the basis for other two WPs and most of its activities should be finished within the first 8 months of the project duration. Work package 6 (Application of GALS to NoC Environment) and work package 7 (Evaluating Advantages of GALS-based Design for Nano-scale Integrated Circuit Fabrication) will be based on results of work package 2. In those two work packages we will explore GALS application to today very attractive NoC platform, and possibilities that GALS methods are effectively used for nano-scale processes in order to cope with problems of power consumption, EMI, process variability and reliability.

Third activity is related to design flow of GALS systems and integrates activities covered by work packages 4 (Architecture for interoperability with external tools) and 5 (GALS Integrated Design Environment). Those activities will run more or less in parallel, one covering co-simulation and co-emulation aspects, and other offering design environment and support for testing, synthesis and layout.

Finally, **fourth activity** that includes WP3 (Development of GALS IP Library) and WP8 (GALS System Design and Evaluation), is oriented towards practical application of GALS methodology and should be based on results achieved in second and third activity. As a result we plan to offer a GALS library of tools, tutorials and components in the framework of work package 3. Additionally, in work package 8 we will try to cope with the GALS system design aspects of an example complex digital communication processor. In the context of this work package we will also directly compare the effectiveness of the GALS compared to traditional synchronous technique.

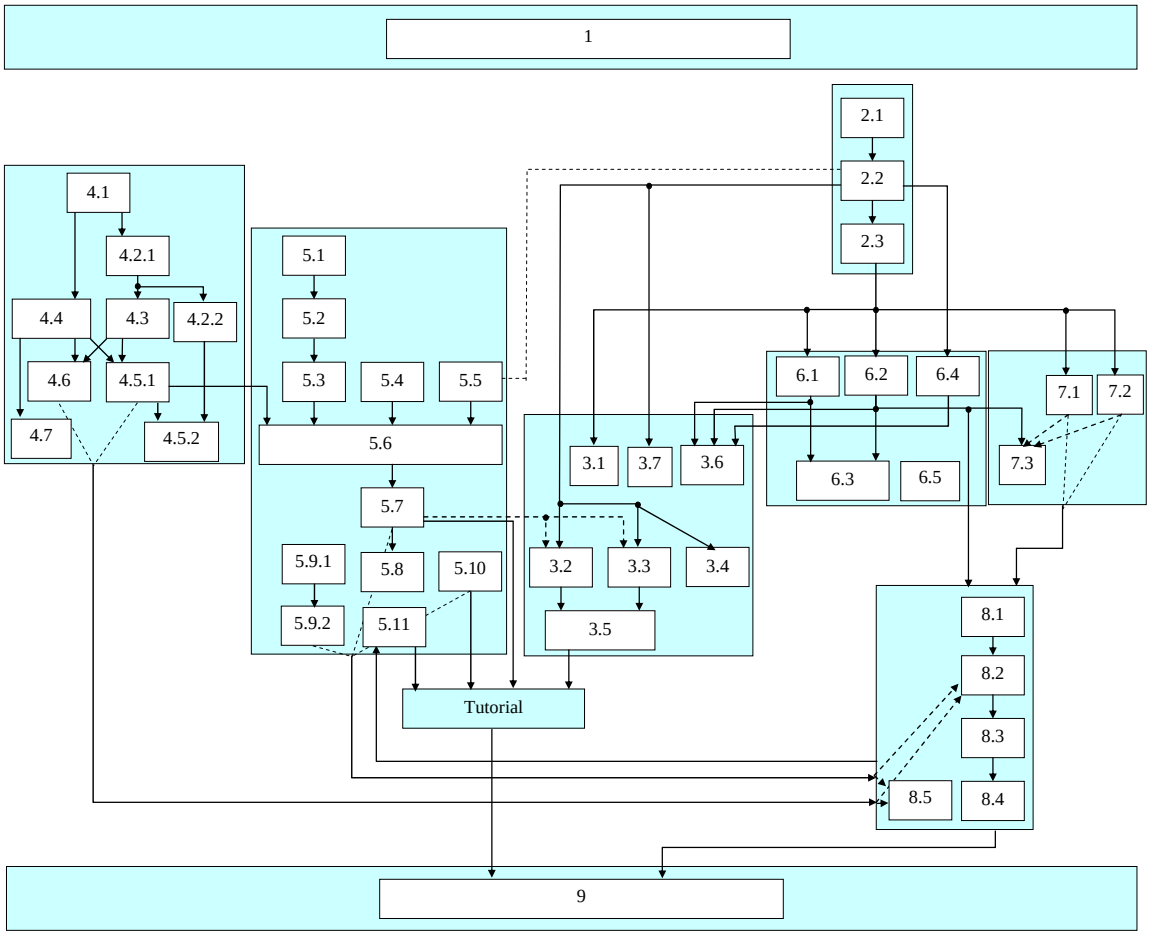
Workpackage 3 (Development of GALS IP library) also partly includes some dissemination actions (generation of design flow tutorials, open source IPs, and establishing a GALS internet forum). Therefore, the efforts needed for such activities, which naturally belong to dissemination, are counted only in WP3 and not in WP9.

In the context of GALAXY project we plan several IC integrations in 0.13 um CMOS process from IHP and 45 nm CMOS process from INFINEON. Those integrations are planned as deliverables of WP7 and WP8, but they should be the result of the synergy of the whole consortium and based on the activities of several WPs. More details about the IC integrations are given in subsection B.1.1.3.

The main dependencies between work packages are following:

- The results from WP2 are basis for work in WP3, WP6 and WP7
- The results from WP4 (4.5.1 and 4.6) are basis for WP8 (8.2 and 8.5)
- The results from WP5 (5.7, 5.10 and 5.9.2) are basis for WP8 (8.2)
- The results of WP7 (7.1 and 7.2) are basis for WP8
- The results from WP3 (3.7) are important for WP8 (8.2)
- The results from WP6 (6.2) are basis for WP8
- WP5 and WP3 are important for tutorial
- There is a dependency between 2.2 and 5.5

The following diagram illustrates dependencies between the tasks in our project.



In the following tables we will identify the significant risks for every work packages and the plans for their avoiding and contingency actions.

WP1 (Project Management)	**Comment**
Risk	Not enough time/resources to fulfil the project tasks in WPs
Effect	Time delay, inability to complete project within the provided time and on or within budget
Critical Level	High
Actions	Frequent progress and spending checks will allow project management to anticipate the problems, reschedule tasks and reallocate resources

WP2 (GALS Interface Evaluation and Application Scenario)	**Comment**
Risk	Late agreement between the partners regarding requirements
Effect	Time delay
Critical Level	Moderate-Low
Actions	Organize project management meeting to early reach compromise regarding requirements for the GALS interfaces

WP3 (Development of GALS IP Library)	**Comment**
Risk	Standard cells delayed, not enough time allocated
Effect	Time delay
Critical Level	Moderate-low
Actions	Clear specification and agreement as to which cells will be available, and their characteristics required up-front before too much logical design is performed.

WP3 (Development of GALS IP Library)	**Comment**
Risk	Without IP libraries: there is no possibility of rapid design.
Effect	No adoption of our tools by the design community
Critical Level	Moderate-High
Actions	High priority will be given to ensure completion of this WP.

WP4 (Architecture for Interoperability with External Tools)	**Comment**
Risk	Interoperability not achieved.
Effect	One of the main targets of the call “Increased interoperability of tools from SME vendors” will not be achieved
Critical Level	High
Actions	Preliminary work has established that all the important simulators possess the appropriate capabilities to be connected as plug-ins to external frameworks such as ours, and previous experience in developing the Balsa system has given expertise in interfacing with commercial tools such as the Cadence Framework, Synopsys and Xilinx design kits. An efficient (in terms of speed) co-simulation backplane is targeted. If this fails, interoperability will still be achieved with lower performance.

WP5 (GALS Integrated Design Environment)	**Comment**
Risk	Main risk is the inability to establish a proper design flow. It will not be easy to design a framework that interfaces to closed industry tools.
Effect	This part of the design system will be of little use
Critical Level	High: (basis of the tools and call)
Actions	Previous experience in developing the Balsa system has given expertise in developing such a framework. Most attention will be given to the system’s architecture and a long analysis period has been allocated in the work package in order to avoid any unforeseen implementation delay.

WP6 (Application of GALS to NoC Environment)	**Comment**
Risk	Inefficient implementation of GALS NoC interfaces
Effect	underestimate potential impact of GALS on NoCs, shadow project outcomes
Critical Level	Medium-low
Actions	Tight interaction between NoC experts, GALS experts and experienced designers

WP7 (Evaluating Advantages of GALS-based Design for Nanoscale Integrated Circuit Fabrication)	**Comment**
Risk	The chosen design examples may be unsuitable to

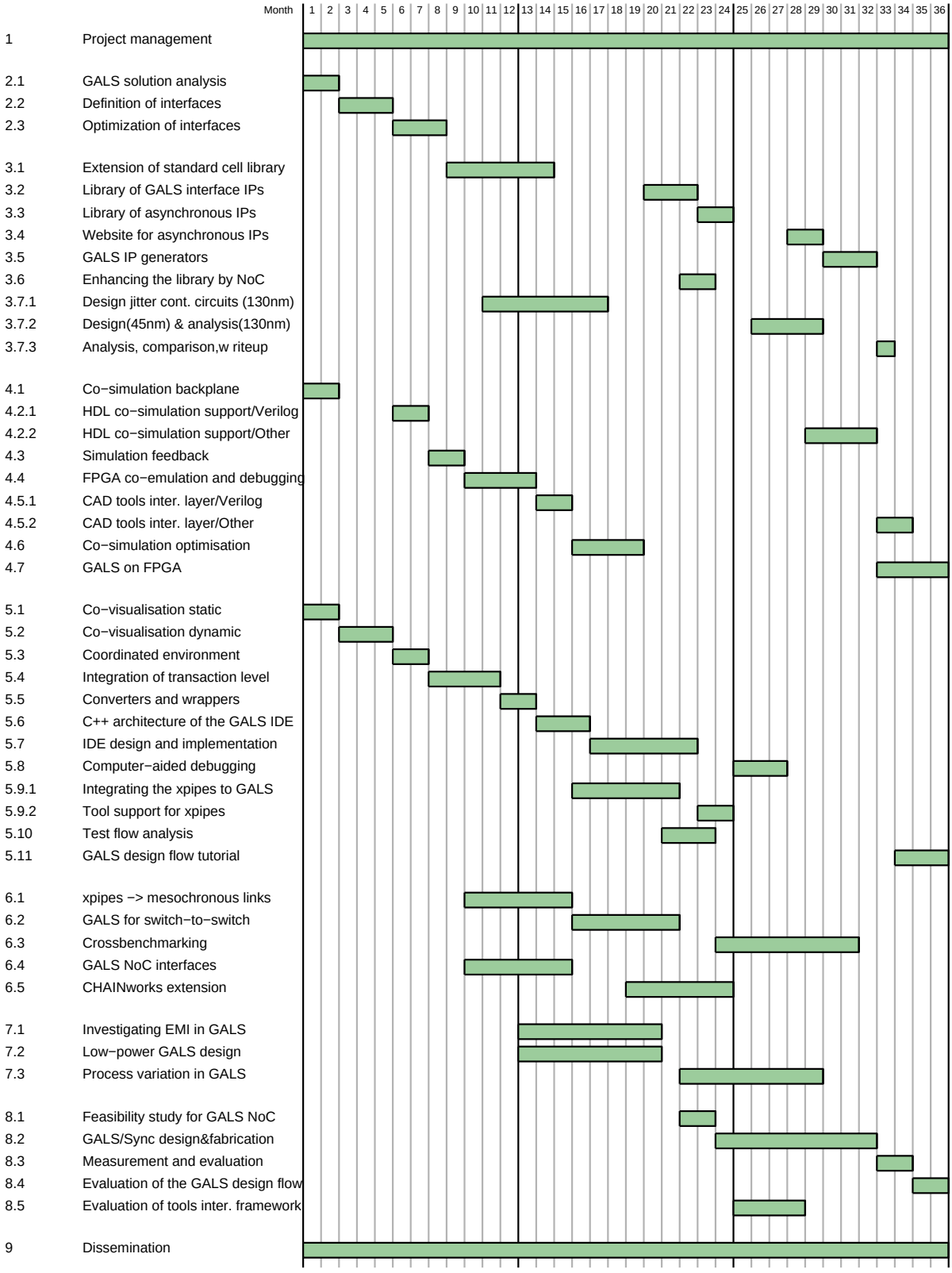
	demonstrate potential advantages of the GALS methodology;
Effect	Unable to justify or quantify advantages of GALS in selected fields
Critical Level	Low
Actions	Members participating in the WP have significant prior experience in this field. Adequate time will be allocated to find suitable design examples

WP8 (GALS System Design and Evaluation)	**Comment**
Risk	Chip design unsuccessful
Effect	Project delayed
Critical Level	Moderate
Actions	Provide the design kit to designers early enough, make peer reviews of the designs before tape-out, organize trainings for new developed tools, Team members included in this WP have already extensive experience in chip fabrication.

WP9 (Dissemination)	**Comment**
Risk	covered in section B.3.1.4

In the following subsections we will present the Gantt chart, structure of the work packages, and efforts needed to fulfil those tasks.

B.1.3.2 Timing of work packages and their components



B.1.3.3 Work package list

Work package list

Work package No	Work package title	Type of activity	Lead beneficiary No	Person-months	Start month	End month
1	Project Management	MGT	1	17.6	1	36
2	GALS Interface Evaluation and Application Scenario	RTD	1	25	1	8
3	Development of GALS IP Library	RTD	5	43.6	9	33
4	Architecture for Interoperability with External Tools	RTD	2	29	1	36
5	GALS Integrated Design Environment	RTD	2	56	1	36
6	Application of GALS to NoC Environment	RTD	3	46.7	10	31
7	Evaluating Advantages of GALS-based Design for Nano-scale Integrated Circuit Fabrication	RTD	4	47	13	29
8	GALS System Design and Evaluation	RTD	1	34.7	22	36
9	Dissemination	RTD	6	13	1	36
	TOTAL			**312.6**		

B.1.3.4 DELIVERABLES LIST

List of Deliverables - to be submitted for review to EC

Del. no.	Deliverable name	WP no.	Lead beneficiary	Estimated indicative person-months	Nature	Dissemination level	Delivery date (proj. month)
D1	Project management reports	1	IHP	14.6	R	CO	6, 12, 24, 36
D2	Asynchronous IP Packaging: specifications	2	UNIMAN	5	R	PU	5
D3	Specification of optimized GALS interfaces and application scenarios	2	IHP	20	R	PU	8
D4	Extension of standard cell library for 130 nm CMOS (IHP) and 45 nm CMOS (INFINEON) processes	3	INFINEON	15	P	RE	14
D5	Specification of characterization for the additional asynchronous standard cells for INFINEON 45 nm CMOS process	3	INFINEON	2	R	PU	14
D6	SystemC-based virtual platform for functional simulation of NoCs with mesochronous links	6	UNIBO	6	P	CO	15
D7	Synthesizable models of optimized GALS network interfaces for NoC design	6	UNIBO	10	P	CO	15
D8	Test chip for evaluating GALS methodology in 130 nm CMOS process provided from IHP	7	IHP	10	P	CO	17
D9	Basic plan for the use, exploitation, and dissemination of foreground	9	INFINEON	1	R	CO	18
D10	Internal version of co-simulation software and plug-ins	4	UNIMAN	17	P	CO	19
D11	Report on EMI reduction with GALS	7	IHP	6	R	PU	20
D12	Report on testing and measurements of test chip in 130 nm CMOS process provided from IHP	7	IHP	5	R	PU	20
D13	SystemC-based virtual platform for functional simulation of NoCs with multi-clock domains	6	UNIBO	6	P	CO	21
D14	Internal version of IDE software,	5	UNIM	33	P	CO	22

	supported with enhanced xpipes flow		AN				
D15	GALS NoC library	3	UNIBO	3	P	PU	23
D16	Report on GALS test flow	5	IHP	9	R	PU	23
D17	Feasibility study for using GALS NoC in the GALS system implementation	8	EPFL	4	R	PU	23
D18	IP libraries	3	UNIMAN	5	P	PU	24
D19	Software tools released under GPL	5	UNIMAN	5	P	PU	27
D20	Report on tools interoperability framework	8	UNIMAN	4	R	PU	28
D21	Ability to have clocked/async boundaries within the switching fabric of the CHAIN network	6	STX	6	P	CO	29
D22	Report on architectural level techniques for process variation tolerance in NoCs	7	UNIBO	17	R	PU	29
D23	Website to publish and exchange compliant IPs/ Internal project website;	9	UNIMAN/ IHP	5	O	PU/CO	29/1
D24	Advantages for GALS based design	7	EPFL	9	R	PU	30
D25	Report on the crossbenchmarking results of fully synchronous vs GALS NoC implementations and GALS-oriented Interfaces for NoC Design	6	UNIBO	18.7	R	PU	31
D26	Web-site and software tools (3.4-3.5) under GPL	3	UNIMAN	3.6	P	PU	32
D27	GALS and synchronous version of the hardware accelerator in 45 nm CMOS process provided from INFINEON	8	IHP	16.7	P	CO	32
D28	Pausible clock dll with self-calibration, jitter, frequency and drift control: report	3	STX	15	R	CO	33
D29	Test and measurement report of GALS and synchronous hardware accelerator chips	8	IHP	6	R	PU	34
D30	Final project report	1	IHP	2	R	PU	36
D31	Additional co-simulation plug-ins under GPL	4	UNIMAN	12	P	PU	36

D32	Tutorial on GALS simulation, synthesis and layout flow	5	EPFL	9	R	PU	36
D33	Report on "System integration based on GALS design flow"	8	IHP	4	R	PU	36
D34	Report containing summary of all publication, presentations and patent applications generated within the project	9	IHP	5	R	PU	36
D35	Conference Tutorials	9	UNIMAN	1	R	PU	36
D36	Final plan for the use, exploitation, and dissemination of foreground	9	INFINEON	1	R	CO	36
D37	Report "Awareness and wider societal implications"	1	IHP	1	R	PU	36
			TOTAL	312.6			

B.1.3.5 WORK PACKAGE DESCRIPTION

Work package number	**1**		**Start date or starting event:**		**Month 1**	
Work package title	***Project Management***					
Activity type	**MGT**					
Participant id	**IHP**	**UNIMAN**	**STX**	**UNIBO**		
Person-months per participant	**15**	**1.1**	**0.5**	**1**		

Objectives

- Managing and monitoring the project activities in general.
- Ensuring fulfilling of committed milestones and generation of deliverables.
- Preserving technical consistency of the project.
- Providing synergy between different Work Packages and different teams working on them.
- Promoting acceptance of project results.
- Establishing the right basis for the successful utilization of project results.
- Resolving internal conflicts within the project.
- Organising and co-ordinating project meetings.
- Managing project resources and monitor spending
- Managing risks and coping with unexpected events.

Description of work and role of partners

- Organisation of the regular management and technical meetings, audit preparation meetings, audits.
- Monitoring of the project milestones and resource consumption. Providing progress reports for EC.
- Information sharing to the project partners.
- Preparation and maintenance of the internal web-based project folder.
- Contact with the EC for every important issue of the project; convey the information to the partners for issues regarding payments, timely delivery of project documents, etc.

IHP (task leader) *– Consortium management activities (legal, ethical, financial and administrative management). Duration: 8 person-months*

UNIMAN – Support in consortium management activities (legal, ethical, financial and administrative management). Duration: 1.1 person-months

STX – Support in consortium management activities (legal, ethical, financial and administrative management). Duration: 0.5 person-months

UNIBO – Support in consortium management activities (legal, ethical, financial and administrative management). Duration: 1 person-month

IHP – Technical project management (coordination of research and technological development

activities). Duration: 7 person-months

IHP is a work package leader and coordinates management activities.

Deliverables and month of delivery

- D1 Project management reports (6th Month, 12th Month, 24th Month, and 36th Month)
- D30 Final project report (36th Month)
- D37 Report "Awareness and wider societal implications" (36th Month)

Work package number	**2**		**Start date or starting event:**	**Month 1**		
Work package title	***GALS Interface Evaluation and Application Scenario***					
Activity type	**RTD**					
Participant id	**IHP**	**INFINEON**	**UNIMAN**	**STX**	**EPFL**	
Person-months per participant	**12**	**6**	**3**	**2**	**2**	

Objectives

- Selecting the optimal GALS architectures for the different target applications
- Analyzing the possibilities for standardized and simplified GALS communication interfaces.
- Considering potential optimization of the available GALS interfaces in terms of hardware complexity, performance, reduced power dissipation, ease of use.
- Specifying open formats for asynchronous IPs (or extension of existing synchronous formats) to consolidate asynchronous IPs dissemination and re-use. The IP format will be able to describe hardware/software entities at multiple levels of abstraction in multiple languages (SystemC, C, Verilog, VHDL, Balsa, gate-level netlist,...), with both synchronous and asynchronous interfaces. The IP format will contain enough information to transparently convert signals between varying levels of abstraction, enabling:
    - a transparent co-simulation of IPs at different levels of abstraction,
    - the visualisation of signals at levels of abstraction independently of the simulated level of abstraction,
    - the exploitation of transaction level stuff during hardware-software co-design and in the visualisation.

Description of work and role of partners

- **GALS solution analysis (2.1):** This work package is dedicated to the specification and design of GALS interfaces. In this work package we plan to analyze current GALS solutions and target applications. On the basis of this analysis we plan to generate a report describing optimal GALS architectures in conjunction with the target application.

  IHP (task leader) *– Analysis & Report Generation. Duration: 4 person-months*

  INFINEON – Providing industry requirements. Duration: 3 person-months

- **Definition of interfaces (2.2):** We will explore the possibilities for adapting the GALS interfaces between locally synchronous blocks to be compliant with the existing standardized protocols. We will evaluate the feasibility for building a wrapper logic template for some of the standard protocol interfaces (OCP, AMBA-AXI, etc.). We will explore further simplification of GALS interfaces to the synchronous parts of the design. This way we will be able to utilize GALS interfaces that are also user-friendly to designers without asynchronous experience.

  We will establish the specifications of an open format for mixed synchronous-asynchronous IPs, in order to consolidate asynchronous IPs dissemination and re-use. The IP format will be able to describe hardware/software entities at multiple levels of abstraction in multiple languages (SystemC, C, Verilog, VHDL, Balsa, gate-level netlist), with both synchronous and asynchronous interfaces. The IP format will contain enough information to transparently convert signals between varying levels of abstraction, enabling:

  - a transparent co-simulation of IPs at different levels of abstraction and
  - the visualisation of signals at levels of abstraction independently of the simulated level of abstraction.

This IP format will probably be an extension of the existing SPIRIT IP packaging format.

IHP (task leader) *– Exploring and adapting the interfaces. Duration: 4 person-months*

EPFL – Supporting interface definition for pausible clocking scheme. Duration: 2 person-months

UNIMAN – IP packaging format. Duration: 3 person-months

INFINEON – Providing industry view to interface adaptation. Duration: 3 person-months

STX – Supporting interface and IP packaging definition with industry interconnect requirements. Duration: 2 person-months

- **Optimization of interfaces (2.3):** We will analyze possibilities for optimization of the existing GALS interfaces. This work will have several possible targets. We will consider the application of GALS interfaces in a realistic target scenario. We will target performance improvements including latency, throughput and performance degradation issues.

  IHP (task leader) *– Possibilities for interface optimization. Duration: 4 person-months*

All specifications describing GALS interfaces will be offered freely for non-commercial use.

IHP is a work package leader.

Deliverables and month of delivery

- D3 Specification of optimized GALS interfaces and application scenarios (8th Month)
- D2 Asynchronous IP Packaging: specifications (5th Month)

Work package number	3		Start date or starting event:	Month 9		
Work package title	*Development of GALS IP Library*					
Activity type	RTD					
Participant id	STX	INFINEON	UNIMAN	IHP	EPFL	UNIBO
Person-months per participant	16	12	8.6	4	2	1

Objectives

- IHP library of standard cells for 0.13 um CMOS process will be extended with additional asynchronous cell: Mutex, C-element, etc. This feature will be offered to all research and academic institutions across Europe via Europractice program.
- INFINEON library of standard cells for 45 nm CMOS process will be extended with additional asynchronous cell: Mutex, C-element, etc.
- Library of GALS interface IPs making the plug-and play of synchronous and asynchronous IPs together trivial.
- Library of asynchronous IPs allowing new users to easily build a functional asynchronous or GALS system. Very small library limited to components needed in a tutorial. Expected to grow by encouraging community sharing of IPs via a website (similarly to opencores.org).
- Enhancement of GALS IP library by NoC building blocks with GALS interfaces .
- Design of wrappers for network interfaces and of optimized GALS-oriented network interfaces including transactors and GUI able to control IPs'.
- Development of calibration and jitter control circuits for pausible clocking.

Description of work and role of partners

- **Extension of standard cell library for asynchronous components (3.1):** IHP will generate a new set of standard cells supporting asynchronous design (C-element, mutex, etc.) for their 0.13 um CMOS process. Additionally, we will include some of the simpler GALS handshake and interface components as hard macros and offer them to the users. Those extended set will be offered over Europractice in case of IHP CMOS process. INFINEON will publicly make available specification of characterization for the additional asynchronous standard cells for its 45 nm CMOS process, in order to ease the effort needed from other research groups to design similar cells for other processes.

  IHP – Extension of the standard cell library for IHP 0.13 um CMOS process. Duration: 4 person-months

  ***INFINEON (task leader)** – Extension of the standard cell library for INFINEON 45 nm CMOS process. Duration: 12 person-months*

  STX – Specification of cells to be created. Duration 1 person-month

- **Implement library of GALS interface IPs (3.2)** following the specified async IP format: multiple levels of abstraction, multiple languages for proper debugging in the IDE.

  ***UNIMAN (task leader)** – Generation of GALS interface library. Duration: 3 person-months*

- **Implement library of asynchronous IPs (3.3)** allowing new users to easily build a functional asynchronous or GALS system. Very small library limited to components needed in a tutorial. Expected to grow by encouraging community sharing of IPs via a website (similarly or in collaboration with to opencores.org).

  ***UNIMAN (task leader)** – Generation of asynchronous IP library. Duration: 2 person-months*

- Set up a **website to publish and exchange "compliant"** (i.e. following the "Asynchronous IP

packaging" specifications) **asynchronous IPs (3.4)**. Package properly a set of asynchronous IPs as an example.

UNIMAN (task leader) *– Setup of the public web-site. Duration: 0.6 person-months*

- **GALS IP generators (3.5)**

  GALS IP generators are able to import circuits described in other languages within a GALS project. They automatically distinguish the processing blocks from the interconnect and convert the original description (Verilog, Balsa, ...) into a GALS interconnect format and GALS IP wrappers.

  The principal converter will be one able to analyse Verilog projects and convert them to our GALS format.

  UNIMAN (task leader) *– Creation of GALS IP generators. Duration: 3 person-months*

- **Enhancing the GALS IP library by NoC components (3.6):**

  Work package 6 of this project is dedicated to investigate the application of NoC concept in the GALS methodology. As part of this work package, new GALS components will be developed in Task 6.4. These new NoC interface components will be made available as part of the GALS IP library. In this task the necessary CAD views to use the GALS-based NoC interface components in the new design flow will be provided.

  UNIBO (task leader) *– Contribution of GALS NoC building blocks (architectural models). Duration: 1 person-months*

  EPFL – Developing the NoC specific cells and or macros as specified by UNIBO. Duration: 2 person-months

- **Calibration and jitter control circuits for pausible clocking (Part 1, 2 and 3) (3.7):**
  Silistix' existing pausible clock NoC interface wrappers will be extended with a range of new features including support for automatic calibration against free-running clocks, and dynamically varying the generated clock frequency to facilitate power reduction. Special attention will be paid to managing the drift and jitter in the generated clocks – an essential, and largely unaddressed requirement to allow this type of GALS wrapper to be used with conventional clocked designs. The effects of scaling will be explored by performing the same analysis of the same circuits on both the IHP 130nm and the INFINEON 45nm processes.

  STX (task leader) *– Part 1 – Design and layout in 130 nm CMOS process of pausible clock circuits, and supporting evaluation circuits. Duration: 10 person-months*

  STX – Part 2 – Layout of pausible clock circuits in 45 nm CMOS process; Analysis of fabricated circuits in 130 nm. Duration: 4 person-months

  STX – Part 3 – Analysis, comparison, write-up, measurements of fabricated circuits. Duration: 1 person-months

  STX is a work package leader.

Deliverables and month of delivery

- D4 Extension of standard cell library for 130 nm CMOS (IHP) and 45 nm CMOS (INFINEON) processes (14th Month)
- D5 Specification of characterization for the additional asynchronous standard cells for INFINEON 45 nm CMOS process (14th Month)
- D18 IP libraries (3.2-3.3) (24th Month)
- D26 Web-site and software tools (3.4-3.5) under GPL (32nd Month)
- D15 GALS NoC library (23rd Month)
- D28 Pausible clock dll with self-calibration, jitter, frequency and drift control: report (33rd Month)

Work package number	4		Start date or starting event:		Month 1	
Work package title	Architecture for Interoperability with External Tools					
Activity type	RTD					
Participant id	UNIMAN	INFINEON				
Person-months per participant	26	3				

Objectives

- Open framework with plug-in system facilitating new entrants for co-design, co-simulation and co-visualization.
- The HLA co-simulation backplane should provide interesting functionalities in terms of simulation time management and an unlimited number of clients.
- Link between simulators/emulators and the debugging environment for real time simulation traces analysis.
- The ability to co-simulate any number and type of targets (simulators/emulators/software) should allow the use of cluster resources for distributed simulations. Research on partitioning strategies is not included in this document, as it is assumed that a manual partitioning of the system will be sufficient due to the coarse granularity of the IPs.
- Code generation for automation of the following tasks:

  - Automated generation of co-simulation/co-emulation interfaces.

  - Automated insertion of signal converters for mixed-mode co-simulation.
- Hardware-software co-simulation, by allowing not only HDL and CAD tools, but also software languages and compilers.
- Prototyping: FPGAs play an increasingly important role in circuit prototyping and even final implementation. The use of FPGAs in a co-simulation framework raises a series of problems needing to be addressed: how should the I/Os of the FPGA be interfaced to the co-simulation backplane? Is it possible to keep the same CLB organisation with and without the co-simulation interface? Is it possible/desirable to monitor internal signals on the FPGA for real-time display in the IDE? Also, asynchronous circuits on FPGAs come with their own problems, which will need to be looked into.

Description of work and role of partners

- **Co-simulation backplane (4.1)**
  The HLA (High Level Architecture) library should provide interesting functionalities in terms of simulation time management and an unlimited number of clients.

  UNIMAN (task leader) *– Implementing co-simulation backplane. Duration: 2 months*
- **HDL co-simulation support (part 1 and part 2) (4.2)**

  Generation of co-simulation interfaces to link the following languages&simulators to the co-simulation backplane.

  - Verilog: Icarus Verilog, Cver, Synopsis VCS, Cadence NC Verilog, Cadence Verilog XL, Modeltech Modelsim
  - Balsa/breeze
  - SystemC: OSCI's base implementation, Synopsis', Cadence's.
  - VHDL: LIP6's freely available Alliance CAD system

Verilog simulators can be linked to the HLA library via their PLI/VPI interface.

UNIMAN (task leader) *– Part 1 – Verilog co-simulation interface generation. Duration: 2 person-months*

UNIMAN – Part 2 – Secondary languages interface generation. Duration: 4 person-months

(1 month per language + 1 week per simulator)

- **Simulation feedback (4.3)**

  Interaction between simulators and the debugging environment for real time simulation traces analysis.

  Establish the requirements for controlling the simulations from the GUI and linking the simulation traces to the GUI.

  UNIMAN (task leader) *– Embedding control of the simulation. Duration: 2 person-months*

- **FPGA co-emulation and remote debugging (4.4)**

  The use of FPGAs in a co-simulation framework raises a series of problems that need to be addressed: how should the I/Os of the FPGA be interfaced to the co-simulation backplane? Is it possible to keep the same CLB organisation with and without the co-simulation interface? Is it possible/desirable to monitor internal signals on the FPGA for real-time display in the IDE? Specific problems of asynchronous circuits on FPGAs.

  Different boards will require different implementations of the board-backplane link. We will start with 2 FPGA boards: APT's standalone board, and Cray XT1's boards.

  - Establish the requirements for controlling the FPGA boards from the GUI and linking the execution traces to the visualisation system.
  - Generation of the co-simulation interface and link to the co-simulation backplane for the FPGA board.

  UNIMAN (task leader) *– Co-emulation for FPGA and debugging. Duration: 4 person-months*

- **CAD tools interoperability layer (Part 1 and Part 2) (4.5)**

  - ***Tool flow automation***

  (Automation of the simulation flows for various languages and simulators/emulators)

  Appropriate tools are transparently called for the chosen simulator/emulator (compilers are automatically called before simulation, and bit-stream generators+board programmers are automatically called when using an emulation board)

  Tool flows would allow an IP to refer to a real source code file (e.g. Balsa, Verilog, SystemC, etc.) and to compile it automatically in the format expected by the simulator (Balsa → Breeze → breeze-sim, Verilog → netlist → spice, Verilog → Xilinx formats → ... → bitstream → FPGA loader, etc.). Research needs to be done on how tool flows can be described and how a compilation path is chosen (multiple paths may be available), remembered and executed.

  - ***Specification of plug-in interface for connecting external tools to the framework***
  - ***Tool flows description***
  - the Xilinx FPGA flow, from compilation to bitstream loading
  - Verilog tool flows
  - Balsa tool flow
  - VHDL tool flows
  - ***Integration of tool flow controls in the GUI***

  Specify requirements for GUI.

  UNIMAN (task leader) *– Part 1 – Verilog tool flow automation. Duration: 2 person-months*

UNIMAN – Part 2 – Tool flow automation for secondary languages and GUI. Duration: 2 person-months

INFINEON – Part 1 & Part 2 – Will provide industry requirements for CAD tools interoperability and will provide the technology, industry support and feedback regarding the tool development. Duration: 3 person-months

- **Co-simulation optimisation (4.6)**

  The HLA library is expected to lead to slow co-simulations. Optimise this up to a desirable speed for distributed simulation on a cluster.

  UNIMAN (task leader) *– Optimizing co-simulation. Duration: 4 person-months*

- **GALS on FPGA analysis and optimisation (4.7)**

  Targeting FPGA boards with GALS circuits is expected to reveal a series of unoptimised situations. Although performance in prototyping is not a requirement, we will analyse here how to optimise area and performance of GALS circuits on FPGAs.

  UNIMAN (task leader) *– GALS on FPGA optimisations. Duration: 4 person-months*

UNIMAN is a work package leader.

Deliverables and month of delivery

- D10 Internal version of co-simulation software and plug-ins (19th Month)
- D31 Additional co-simulation plug-ins under GPL (36th Month)

Work package number	5		Start date or starting event:		Month 1	
Work package title	GALS Integrated Design Environment					
Activity type	RTD					
Participant id	UNIMAN	EPFL	IHP	UNIBO	INFINEON	STX
Person-months per participant	29	8	7	6	3	3

Objectives

- Framework providing interoperability between CAD tools from various vendors or universities (compilers, simulators, debuggers, emulators).
- Design environment based on a representation of the system and its properties in a small number of graphical views. The information processed by the various tools is extracted and merged to provide a simultaneous visualisation of both static and dynamic data from multiple languages, multiple levels of abstraction and multiple simulator traces. It should ultimately provide a powerful design exploration mechanism facilitating the debugging of GALS circuits. Links to the original file formats and tools are preserved as hyperlinks between views.
- User-friendly for designers without experience in asynchronous design in order to promote GALS interest.
- Open environment with plug-in system facilitating new entrants.
- Automated generation of the source code for the graphically-described interconnect between IPs.
- Hardware-software co-design, by allowing not only HDL and CAD tools, but also software languages and compilers.
- Ability to describe, visualise and simulate very large systems such as SpiNNaker's on-chip and inter-chip networks connecting twenty to thousands of ARM cores.
- Research on assisted debugging: exploitation of this unique visualisation system to improve debugging.
- Documentation: tutorial, manual
- Evaluating GALS test, synthesis and layout flow
- Advance design technology for GALS Network-on-Chip design through integration of xpipes into the GALS flow

Description of work and role of partners

- **Co-visualisation backplane, static (5.1)**: Static representation of the circuit exposing the whole circuit and properties in one main graphical view merging multiple languages, abstractions, back-ends and tools.

  Establish the requirements of the visualisation backplane to be able to visualise static Verilog, Balsa and SystemC descriptions integrated inside the IDE views.

  This includes a C++ architecture design of the graph visualisation module (to be done in collaboration with the next work package).

  UNIMAN (task leader) *– Specification of co-visualisation backplane. Duration: 2 person-months*

- **Co-visualisation backplane, dynamic (5.2)**: Evolution of circuit properties (e.g. temperature) over time, animation of the static view by superposing colour-coded property values and events from simulation traces in order to provide debugging functionalities.

Establish the requirements of the visualisation backplane to be able to visualise dynamic simulation activity in the GUI.

This includes an update of the C++ architecture design of the graph visualisation module.

UNIMAN (task leader) *– Specification of dynamic co-visualisation backplane. Duration: 3 person-months*

- **Coordinated multi-view environment (5.3)** able to show the design from different viewpoints simultaneously and interact with external devices (simulators and emulators) in real time.

  UNIMAN (task leader) *– Specification of coordinated multi-view-environment. Duration: 2 person-months*

- **Integration of transaction level and Programmer's View models for co-design and visualisation in GUI (5.4)**

  UNIMAN (task leader) *– Transaction level modelling. Duration: 4 person-months*

- **Converters and wrappers (5.5)**

  Analyse the problem of automatic insertion of converters and wrappers during design in the GALS graphical framework, a way to describe their properties (compliant with the "Asynchronous IP Packaging") and how they can be automatically placed or suggested, and saved when changing configurations (for example when switching a module from one protocol to another and back).

  UNIMAN (task leader) *– Asynchronous wrappers. Duration: 2 person-months*

- **C++ architecture of the GALS IDE (5.6)**

  Based on the requirements gathered for the various parts of the IDE, establish a modular C++ architecture.

  Requirements: - User-friendly graphical manipulation and interconnection of IP blocks.

  UNIMAN (task leader) *– C++ design. Duration: 3 person-months*

- **IDE design and implementation (5.7)**

  Based on the above topics' requirements and architecture, design and implement the IDE.

  UNIMAN (task leader) *– Implementation of IDE. Duration: 6 person-months*

- **Computer-aided debugging (5.8)**

  Exploitation of this unique visualisation system to improve debugging (using visualisation of co-simulation and co-emulation traces)

  - Research on understanding a particular state by visualising the appropriate historic decisions leading to this state.
  - Implementation in the IDE.

  UNIMAN (task leader) *– Debugging. Duration: 3 person-months*

- **Integrating the xpipes flow with the GALS design flow (part 1 and part 2) (5.9);** Xpipes is a well established complete design flow for NoC systems. As part of this task, the Xpipes design flow will be enhanced to include GALS compatible components

  UNIBO (task leader) *– Part 1 – Enhancing the Xpipes flow to support GALS. Duration: 6 person-months*

  EPFL – Part 1 – Backend design and verification aspects. Duration: 3 person-months

  IHP – Part 1 – Technology support. Duration: 2 person-months

  UNIMAN – Part 2 – Support for the asynchronous tools. Duration: 2 person-months

- **Test flow analysis (5.10):** We will consider possible GALS test flow and propose the appropriate test methodology. We will develop a multi-level test strategy for GALS compatible NoC systems. Individual locally synchronous modules will have their own test solutions (Scan-test, functional or BIST). The GALS system will provide automatic test equipment (ATE) access

to each module. We will develop methods to generate functional test patterns to provide test coverage equivalent to that achieved by scan-test based methods for the asynchronous interfaces.

EPFL – Functional test pattern generation for asynchronous interfaces. Duration: 2 person-months

***IHP (task leader)** – Analyzing possibilities for GALS test-flow; BIST DfT approach in GALS environment; Duration: 3 person-months*

STX – Evaluating test flow and pattern generation to determine it's applicability to GALS systems using a self-timed NoC with large amounts of self-timed interconnect logic. Duration: 2 person-months

INFINEON – Evaluating test flow from industrial perspective. Duration: 2 person-months

- **GALS design flow tutorial (5.11):** Preparation of a tutorial explaining how to use the tools, how to plug new back-ends in, and how to tailor the synthesis flow to one's own cell libraries. Based on design experience from WP8 we will document the most effective approaches for synthesis and layout of GALS chip. This will include strategy co-synthesis of asynchronous and synchronous components, a strategy for successful constraining of the GALS design and possible optimization and automation of synthesis flow for GALS designs. Additionally, we will illustrate strategies for GALS system layout using hierarchical and flat approach. We will explain the insertion of asynchronous components as hard macros and as a set of standard cell components.

  ***EPFL (task leader)** – Describing automation of synthesis flow for GALS; describing strategies for layout of GALS circuits. Duration: 3 person-months*

  IHP – Describing constraining of GALS design; describing timing closure in GALS layout process. Duration: 2 person-months

  UNIMAN – Preparation of tutorial covering usage of software tools under GPL. Duration: 2 months

  INFINEON – Evaluating tutorial from industrial perspective. Duration: 1 person-months

  STX – Evaluating tutorial from an SME industrial perspective. Duration: 1 person-months

UNIMAN is a work package leader.

Deliverables and month of delivery

- D14 Internal version of IDE software, supported with enhanced xpipes flow (22nd Month)
- D19 Software tools released under GPL (27th Month)
- D16 Report on GALS test flow (23rd Month)
- D32 Tutorial on GALS simulation, synthesis and layout flow (36th Month)

Work package number	6		Start date or starting event:	Month 10		
Work package title	*Application of GALS to NoC Environment*					
Activity type	RTD					
Participant id	UNIBO	EPFL	STX	INFINEON		
Person-months per participant	26	9.7	8	3		

Objectives

- Leveraging a mature synchronous NoC architecture developed at University of Bologna (called xpipes), the idea is to progressively GALSify it by introducing more and more severe clocking constraints.
- At first, the synchronous clocking scheme will be relieved and mesochronous clocking will be assumed between network switches. IP cores and their switches will be considered as unique locally synchronous domains featuring the same frequency but undefined phase shifts. The objective is to assess the impact of mesochronous communication links on network area and power, while keeping maximum achievable data rate under close control.
- We aim at exploring how switch design is affected by the support for asynchronous communication. In particular, input/output buffering stages and flow control stages are the main candidates for high-impact modifications required by the GALS paradigm. Mesochronous links and long pipelined links of synchronous networks have also to be compared in terms of area, power and performance.
- We target the improvement of synchronous NoC designs and design flows by aggressively modifying NoC architectures in the GALS direction. In other words, we consider locally synchronous domains as fully independent with distinct, individually optimized operating frequencies. We aim at proving that, although this approach heavily affects switch boundary design, it simplifies overall system design (e.g., timing closure), while paving the way for power optimizations.
- We intend to compare synchronous vs GALS NoC architectures in order to prove on the field that GALS designs can overcome the limitations of synchronous realizations while constraining area and performance overheads.
- Consider integration issues of GALS wrappers into the Network Interfaces of NoC architectures
- Starting from the opposite extreme, of already having a GALS system framework based around a delay-insensitive self-timed NoC using truly self-timed switch components, with clocked endpoints, we will also explore the issues of relaxing timing robustness within the network itself to use clocked components interspersed within the switching fabric.
- Extend STX's CHAINworks with clocked additions to the NoC transport layer

Description of work and role of partners

- **Xpipes extension with mesochronous links (6.1):**

  The network backbone operates at a higher clock rate using a dedicated network clock. This latter is distributed over the core network without any mechanism for skew compensation, and packet transmission is performed using mesochronous communication. When a packet is transmitted from one clock domain to another, a strobe signal (STB) is transmitted together with the packet as a timing reference. A synchronizer compensates the phase difference between the STB signal and the local CLKNET. Data transmission using STB signal has one problem: the STB signal has to drive lots of D-FFs so that signal skew occurs which limits maximum operation frequency of the network clock. In order to solve this problem, matched-delay architectures have to be devised wherein the STB skew is properly compensated and

high-speed mesochronous communication is enabled.

UNIBO (task leader) *– Design and functional simulation of mesochronous links within the xpipes NoC architecture. Duration: 6 person-months*

- **On-Chip GALS interfaces for switch-to-switch asynchronous communication (6.2):**

  In GALS NoCs, synchronous units belonging to different clock domains communicate to each other by means of asynchronous channels. There are two main approaches for building GALS NoCs: one where the links are the only asynchronous elements, and one where the whole communication infrastructure is asynchronous and the IP-cores are the only fully synchronous units. Since the latter approach involves a huge re-design effort of traditional synchronous NoC building blocks, this activity targets the former approach. A wrapping activity of NoC switches will allow their asynchronous communication. Several wrapping techniques explored in WP2 (GALS interfaces evaluation), such as mixed-clock FIFOs and pausible clocks, will be applied to switch design, capturing their impact on NoC power, area and performance metrics.

  UNIBO (task leader) *– Design and functional simulation of asynchronous switch-to-switch communication schemes within the xpipes NoC architecture. Duration: 6 person-months*

- **Crossbenchmarking of synchronous vs GALS xpipes NoC variants (6.3):**

  The availability of a mature synchronous NoC architecture (xpipes) and some asynchronous variants (mesochronous, mixed-clock) developed within the project activities make it possible to come up with a comparison between these competing solutions. The comparison framework will regard architecture design and backend synthesis flow. We will be therefore able to investigate whether GALS implementations are really able to overcome clock distribution problems, reduce power dissipation and effectively deal with dynamic bit errors, while at the same time comparing performance and area figures. Power and critical path of the designs will be assessed at gate level through dedicated synthesis flows for each architecture variant. . The benchmarks created will wherever possible be aligned with the actions of the OCP-IP benchmark activity, and the partners will attempt to have input into that forum. Portability of the two design styles to ultra-scaled 45 nm technology provided by Infineon Technologies will be also investigated.

  UNIBO (task leader) *– Crossbenchmarking of synchronous vs GALS xpipes variants in presence of different traffic patterns. Duration: 8 person-months*

  EPFL – Support for the benchmark design. Duration: 5.7 person-months

  STX – Support for benchmark design so they can be run on Silistix CHAIN networks too (although results will have to remain confidential). Duration: 2 person-monhs

  INFINEON – Support for successful design on 45nm technology libraries. Duration: 3 person-monhs

- **Building GALS compatible Network-on-a-Chip interfaces (6.4):**
  GALS and NoCs share the same design principle: in both systems functionality and communication are clearly separated. In a GALS system, communication between functional modules is asynchronous. In theory, existing NoC interfaces can be 'GALSified' by using a simple asynchronous wrapper. However, we believe more efficient realizations can be designed, if the network interfaces (NIC) of the NoC system can be integrated into the asynchronous wrapper surrounding the locally synchronous resource. Such network interface optimization process for GALS NoCs will address issues such as support for standard synchronous protocols (AMBA AXI, OCPv2.0), synchronous-asynchronous conversion boundary, packet composition, flow control issues, support for a variety of asynchronous protocols in the network fabric.

  EPFL – Design of asynchronous wrappers for GALS compatible NoC systems. Duration: 4 person-months

  UNIBO (task leader) *– Design of GALS network interfaces compatible with standard end-to-end communication protocols (AMBA AXI, OCP). Duration: 6 person-months*

- **CHAINworks extension with clocked additions to the NoC transport layer (6.5)**
  Silistix CHAIN network technology is currently implemented using a fully-self-timed switching

transport layer, surrounded with clocked protocol converters for connecting IP blocks. We believe that in some scenarios, this can be improved upon by implementing parts of the system using clocked components, to avoid unnecessary clocked/self-timed crossings. To do so requires this crossing to then happen on the links within the network, and will require clocked versions of the existing CHAIN network components, in addition to use of our in-house developed GALS converters and/or those created in WP3.

STX (task leader) *– Design of clocked CHAIN network components, and application of GALS techniques to allow their use within the CHAINworks. Duration: 6 person-months*

UNIBO is a work package leader.

Deliverables and month of delivery

- D6 SystemC-based virtual platform for functional simulation of NoCs with mesochronous links (15th Month)
- D13 SystemC-based virtual platform for functional simulation of NoCs with multi-clock domains (21st Month)
- D25 Report on the crossbenchmarking results of fully synchronous vs GALS NoC implementations and GALS-oriented Interfaces for NoC Design (31st Month)
- D7 Synthesizable models of optimized GALS network interfaces for NoC design (15th Month)
- D21 Ability to have clocked/async boundaries within the switching fabric of the CHAIN network (29th Month)

Work package number	7		Start date or starting event:		Month 13	
Work package title	*Evaluating Advantages of GALS-based Design for Nano-scale Integrated Circuit Fabrication*					
Activity type	RTD					
Participant id	EPFL	IHP	UNIBO	INFINEON	STX	
Person-months per participant	15	14	6	6	6	

Objectives

- Investigate the advantages of GALS design methods on the Electromagnetic Interference (EMI) of a system. Developing GALS methods to realize systems with lower EMI.
- Combine GALS techniques with Dynamic Voltage Scaling (DVS) methods for minimizing power consumption of systems.
- Determine how GALS-based designs perform in deep-nanometer technologies which exhibit large process variations. Study reliability issues of GALS-based designs in deep sub-nanometer technologies.

Description of work and role of partners

- **Investigating EMI in GALS-based systems (7.1);**

  Electromagnetic Interference is a major contributor of noise in modern integrated circuits, especially in mixed-signal systems. Pure asynchronous circuits which do not use a clock signal are known to have a power spectrum devoid of large peaks. Initial studies have shown that GALS based circuits have significant potential to reduce EMI as well. However until now, no methodology has been developed to analyze EMI in GALS-based systems. The goal of this task will be to methodically analyze EMI in GALS-based systems and provide guidelines and tools to reduce EMI in GALS-based systems.

  IHP (task leader) *– Generating a scalable abstract model in Matlab of the EMI generated from the power supply variations in a GALS system. Develop the optimal algorithms for reducing the EMI. Evaluate the proposed EMI reduction algorithms theoretically and in practice. Fabrication of simple test chip in IHP 0.13 um CMOS process for evaluation of the developed techniques and algorithms (common deliverable for 7.2 and 7.3); Characterizing EMI of the fabricated test chip; Evaluation of measurement results and comparison with theoretical estimations. Duration: 14 person-months*

- **Low-power GALS design (7.2):**

  GALS design has always been known for its low-power potential. Up to now, this potential has been largely unfulfilled, and research in this area has been more on high-level analyses of processor architectures. In this task we plan to combine state-of-the-art low-power methods like dynamic voltage scaling (DVS), and subthreshold logic design with GALS techniques.

  EPFL (task leader) *– Investigating low-power realization of GALS components; Test chip fabrication to evaluate low power techniques in IHP 0.13 um CMOS process (common deliverable for 7.2 and 7.3) Duration: 12 person-months*

- **Circuit and architecture level techniques for process variation tolerance in GALS systems (7.3):**
  Deep-nanometer technologies (65nm and beyond) will offer designers an unparalleled level of integration density. The manufacturing processes required to enable these technologies will be increasingly complex. Despite the best efforts of process engineers, large variations in device parameters will be inevitable in these technologies. In the extreme case, reliable and/or redundant design techniques will be required to cope with increasing device failures to

manufacture integrated circuits with an economically acceptable yield.

Traditional synchronous design methodologies, that require the system to adhere to strict timing constraints over the entire chip area, suffer badly from wide ranging parameter variations. The need to satisfy worst-case timing constraints will limit the performance of future designs severely. GALS systems may offer significant advantages in this field, as they essentially divide a complex global system into small, independent modules. The main contribution of this work is to develop high-level methods in GALS system partitioning to improve the system performance and reliability under large process variations.

EPFL – Investigating reliable circuit architectures, developing test structures that will be fabricated using the IHP 130nm and INFINEON 45nm technologies. Consider effect of further technology scaling (32 nm and beyond) on GALS subject. *Duration: 3 person-months*

UNIBO (task leader) *– Architecture-level solutions for process variation tolerant GALS systems. Duration: 6 person-months*

INFINEON – Technology support for process variation research and reliable architectures; Support for test chip fabrications. Duration: 6 person-months

STX – Investigation of techniques to mitigate process-variation in self-timed NoC transport layer. Duration 6 person-months

EPFL is a work package leader.

Deliverables and month of delivery

- D24 Report on “Advantages of GALS-based design”, concentrating on the impact of different GALS design decisions on performance metrics. (30th Month)
- D11 Report on EMI reduction with GALS (20th Month)
- D8 Test chip for evaluating GALS methodology in 130 nm CMOS process in 130 nm CMOS process provided from IHP (17th Month)
- D12 Report on testing and measurements of test chip in 130 nm CMOS process provided from IHP (20th Month)
- D22 Report on architectural level techniques for process variation tolerance in NoCs (29th Month)

Work package number	8		Start date or starting event:		Month 22	
Work package title	GALS System Design and Evaluation					
Activity type	RTD					
Participant id	IHP	INFINEON	UNIMAN	EPFL	UNIBO	
Person-months per participant	20	4.7	4	4	2	

Objectives

- Performing GALS partitioning of the target (complex synchronous design).
- Evaluation of NoC involvement for the target architecture.
- Insertion of the GALS interfaces to the synchronous target.
- Evaluating tools interoperability framework and in general GALS design flow.
- Show the advantages of GALS-based design for rapid system integration in deep-nanometer technologies on industry relevant IC design examples.
- Design of the complex GALS and equivalent synchronous chip in deep-nanometer technology.
- Evaluation and measurement of the fabricated GALS and synchronous chips.

Description of work and role of partners

- **Feasibility study for using GALS NoC in the GALS system implementation (8.1)**
  The Network-on-a-Chip methodology has been developed with large SoCs in mind. Systems that are not composed of many components, or systems which consist of several tightly coupled modules may not benefit from an NoC application as much as large systems with multiple independent IP modules. Moreover, the effectiveness in the use of NoCs heavily depends on the memory architecture and on the possibility to parallelize memory accesses. A preliminary analysis of traffic patterns and of feasible memory architectures will be needed to assess the applicability of the NoC solution to the GALS implementation proof of concept. Within WP6 we will evaluate how the GALS methodology can be paired with NoC implementations. Based on the result of this work, the system planned to be GALSified will be investigated and a report stating whether or not this system would benefit from a NoC implementation will be compiled.

  Additionally, we will analyze the optimal GALS interface architecture for targeted application.

  EPFL (task leader) *– Study implementation. Duration: 2 person-months*

  UNIBO – Support work and enabling expertise in NoC design. Duration 2 person-months

- **Design and fabrication of the GALS and synchronous version of the target system in 45 nm CMOS process (8.2):** Target is GALSification of the hardware accelerator for the state-of-the-art communication system developed in IHP. The goal is to implement GALS based interfaces in the hardware accelerator and improve the system integration and EMI characteristic. Therefore, we will consider implementation of EMI reduction algorithms in the GALS demonstrator. Application in the area of wireless communications requests power saving features. Consequently, the developed system should integrate power saving mechanisms. We will implement DfT logic for testing of the GALS systems. Finally, this complex GALS system including the additional logic for evaluation should be fabricated as an ASIC in INFINEON 45 nm CMOS process. In parallel, to have the fair approach we will design the synchronous version of the same system.

  IHP (task leader) *– Generating behavioural model, GALS partitioning, validation, synthesis,*

layout, DfT, generation of test vectors and test specifications. Duration: 14 person-months

INFINEON – Technology support for chip design and fabrication. Duration: 2.7 person-months

- **System measurement and evaluation (8.3):** After fabrication those chips will be thoroughly tested. After that we will make EMI measurements to evaluate implemented techniques.

  ***IHP (task leader)** – Evaluation and measurement of the chips. Duration: 4 person-months*

  INFINEON – Technology support for test and measurements. Duration: 2 person-months

- **Evaluation of the GALS design flow (8.4):** The complete process of chip design will be evaluated and we will make comparison between standard synchronous and GALS design process.

  ***IHP (task leader)** – Evaluation of GALS design flow based on design experience while designing GALS and synchronous system. Duration: 2 person-months*

  EPFL – Comparison of system integration aspects. Duration: 2 person-months

- **Evaluation of tools interoperability framework (8.5):** The following aspects of our design framework will be evaluated:
  - ease of rapid design and prototyping
  - building embedded systems from mixed components (mixed description languages, mixed synchronous-asynchronous and mixed provenance industry/open-source world)
  - making use of multiple tools from independent vendors: simulators from multiple sources (industry or open-source) will be used together for the simulation and debugging of mixed components
  - prediction of circuit properties (such as performance, robustness, EMI, power) and circuit tuning by using the visualization and debugging interface
  - demonstration of fast distributed simulation (and distributed compilation) on clusters

  ***UNIMAN (task leader)** – Evaluation of tools interoperability framework. Duration: 4 person-months*

IHP is a work package leader.

Deliverables and month of delivery

- D17 Feasibility study for using GALS NoC in the GALS system implementation (23rd Month)
- D27 GALS and synchronous version of the hardware accelerator in 45 nm CMOS process provided from INFINEON (32nd Month)
- D29 Test and measurement report of GALS and synchronous hardware accelerator chips (34th Month)
- D33 Report on "System integration based on GALS design flow" (36th Month)
- D20 Report on tools interoperability framework (28th Month)

Work package number	**9**		**Start date or starting event:**	**Month 1**		
Work package title	***Dissemination***					
Activity type	**RTD**					
Participant id	**INFINEON**	**UNIMAN**	**EPFL**	**UNIBO**	**STX**	**IHP**
Person-months per participant	**3**	**3**	**2**	**2**	**2**	**1**

Objectives

- Promote GALS chip interconnect advantages for complex system design
- Popularize GALS design flow
- Disseminate the project information in general press
- Make scientific contribution to the area of GALS design flow, power & EMI reduction with GALS, improvement of the GALS interfaces, GALS in conjunction with NoC, approach nanoscale challenges as variability and reliability
- Work on standardization of GALS NoC interfaces and on extension of the SPIRIT packaging format for mixed synchronous-asynchronous IPs.
- Commercially exploit the project results

Description of work and role of partners

- We will organize and attend workshops and summer schools for enabling the impact of GALS design methodology. IHP will in the framework of annual Summerschool of Microelectronics for PhD students from Eastern Europe organize GALS lectures and popularize GALS design flow.
- We will provide tutorials and documentation for GALS design flow. Project web-page will be created and it will serve as a community forum for exchanging IP cores, design scripts and sharing experiences among GALS design community. In order to increase the impact of the project results, the GALS design flow and some GALS IPs will be offered as open-source over this web-portal. Additionally, we will enable the use of necessary asynchronous standard cells over university Europractice program with discounted prices.
- Project public relations will be based on the publications in the global and especially in the local media. In this way the project participants will not only disseminate scientific results of the project, but also promote the values of European Union and importance of scientific support coming from EU to local community. In particular, IHP, UNIMAN, and STX will generate an ambitious plan for communication with the local media of Manchester and Frankfurt (Oder). A financing coming from EU has special importance for those two cities. For example, two legal entities (and one is SME) from Manchester will be financed over the GALAXY project. Similarly, for Frankfurt (Oder) is the investment in new technological development an important chance to cope with the high unemployment rate. One good opportunity for such contact with media is the annual "Day of open doors" in IHP where the project results will be presented to the journalists. More details on general press dissemination can be found in section B.3.2.1.
- The result of our project should be also a number of journal, conference papers and possibly patents. We will propose a tutorial on GALS-NoC design at some major conference (DATE, ASYNC, NoC symposium). This work will be strongly encouraged and supported during the project.

- We will try to influence standardization of the GALS NoC interfaces. We will propose our vision of standard NoC GALS interface. Extend the existing SPIRIT IP packaging format with specifications of a format for mixed asynchronous-synchronous IPs.
- We will generate the plans for commercial exploitation of the project results. An interim plan will be generated after the first half of the project. This plan will include the basic ideas about the future exploitation. The final plan is planned for the end of the project. Initially, we have planned four different ways of the commercial exploitation. One is exploitation of CAD software tools planned to be offered as open-source. The second is exploitation of GALS and NoC circuits, methods and algorithms. Third way is providing the design services. Finally, the most important aspect is the exploitation over the industrial partners of the project. Consequently, STX will directly apply the project deliverables in their products. Infineon will use the developed asynchronous libraries in their design flow and enable their possible future GALS products. Finally, our industrial partners will have the priority in exploitation of the project foreground. Otherwise, the other partners will consider exploitation of their deliverables over an industrial partner or by creating a start-up. More details can be found in section B.3.2.4 Plan for the exploitation of the project results (page 79).

INFINEON is a work package leader and coordinates fulfilments of dissemination tasks.

Deliverables and month of delivery

- D34 Report containing summary of all publications, presentations and patent applications generated within the project (36th Month)
- D23 Website to publish and exchange compliant IPs; Internal project website; (29th Month; 1st Month)
- D35 Conference Tutorials (36th Month)
- D9 Basic plan for the use, exploitation, and dissemination of foreground (18th Month)
- D36 Final plan for the use, exploitation, and dissemination of foreground (36th Month)

B.1.3.6 EFFORTS FOR THE FULL DURATION OF THE PROJECT

The following table integrates the summary of staff effort for the GALAXY project. Work package leaders are indicated by showing their relevant person-month figure in bold.

Project Effort Form 1 - Indicative effort per beneficiary per WP

Project number GALAXY: 214364

Workpackage	WP 1	WP 2	WP 3	WP 4	WP 5	WP 6	WP 7	WP8	WP 9	TOTAL per Beneficiary
IHP	**15**	**12**	4	0	7	0	14	**20**	1	**73**
UNIMAN	1.1	3	8.6	**26**	**29**	0	0	4	3	**74.7**
EPFL	0	2	2	0	8	9.7	**15**	4	2	**42.7**
UNIBO	1	0	1	0	6	**26**	6	2	2	**44**
STX	0.5	2	**16**	0	3	8	6	0	2	**37.5**
INFINEON	0	6	12	3	3	3	6	4.7	**3**	**40.7**
Total	**17.6**	**25**	**43.6**	**29**	**56**	**46.7**	**47**	**34.7**	**13**	**312.6**

Project Effort Form 2 - indicative efforts per activity type per beneficiary

Project number GALAXY: 214364

Activity Type	IHP	UNIMAN	EPFL	UNIBO	STX	INFINEON	TOTAL ACTIVITIES
RTD/Innovation activities							
WP 1 Project Management	7	0	0	0	0	0	7
WP 2 GALS Interface Evaluation and Application Scenario	12	3	2	0	2	6	25
WP 3 Development of GALS IP Library	4	8.6	2	1	16	12	43.6
WP 4 Architecture for Interoperability with External Tools	0	26	0	0	0	3	29
WP 5 GALS Integrated Design Environment	7	29	8	6	3	3	56
WP 6 Application of GALS to NoC Environment	0	0	9.7	26	8	3	46.7
WP 7 Evaluating Advantages of GALS-based Design for Nano-scale Integrated Circuit Fabrication	14	0	15	6	6	6	47
WP 8 GALS System Design and Evaluation	20	4	4	2	0	4.7	34.7
WP 9 Dissemination	1	3	2	2	2	3	13
Total 'research'	65	73.6	42.7	43	37	40.7	302.0
Demonstration activities							
Total 'demonstration'	0	0	0	0	0	0	0
Consortium management activities							
WP 1 Project Management	8	1.1	0	1	0.5	0	10.6
Total 'management'	8	1.1	0	1	0.5	0	10.6
Other activities							
Total 'other'	0	0	0	0	0	0	0
TOTAL BENIFICIARIES	73	74.7	42.7	44	37.5	40.7	312.6

B.1.3.7 LIST OF MILESTONES AND PLANNING OF REVIEWS

List and schedule of milestones

Milestone number	Milestone name	WP no's.	Lead beneficiary	Delivery date from Annex I	*Comments*
M1.1	Project meetings, quarterly	1	IHP	Quarterly from 3	
M2.1	GALS interfaces specified	2	IHP	8	Specification of interfaces generated
M3.1	Standard cell library enhanced to asynchronous components	3	INFINEON	14	Library files generated, characterization done, documentation available
M4.1	Internal version of co-simulation software and plug-ins available	4	UNIMAN	19	Release of internal version of co-simulation software tools featuring the automated generation of Verilog co-simulation interfaces
M5.1	Internal version of IDE software available	5	UNIMAN	22	Release of internal version of tools, with a fully functional graphical IDE able to use IPs as defined in WP2 and the co-simulation tools from milestone 4.1
M5.2	Software tools released under GPL.	5	UNIMAN	27	Public release of software under GPL license
M6.1	GALS NoC mesochronous interface implemented	6	UNIBO	15	release of virtual platform for modelling and simulation of mesochronous NoCs
M6.2	GALS NoC asynchronous interface implemented	6	UNIBO	21	release of virtual platform for validation (modelling and simulation) of multi-clock domain NoCs
M6.3	Comparison between fully synchronous vs GALS NoCs	6	UNIBO	31	report validating the improvements of NoC technology enabled by GALS design techniques
M7.1	EMI and power reduction with GALS algorithms and interfaces ready	7	EPFL	21	Reports validating the improvements with GALS methodology delivered, source IP ready
M7.2	Architecture and circuit-level techniques for noise- and process variation-tolerant NoC design	7	UNIBO	29	Reports validating the improved robustness of NoC architectures with respect to noise sources and process-variations.
M7.3	Test chip taped-out in 130 nm CMOS process	7	IHP	17	Design validated, layout ready
M8.1	Sync / GALS system examples taped-out in 45 nm process	8	IHP	29	Design validated, layout ready

In the GALAXY project we have planned 13th milestones. Work-packages 1-8 are covered with at least one milestone.
In WP1 (management) we have planned a repetitive milestone - quarterly organized project meetings.
A significant milestone for WP2 is generation of the GALS interfaces specification (8th month). This work is very important and affects other WPs (see Perth chart) and therefore is successful completion of outmost interest.
In WP3 (GALS libraries) we have defined a milestone - generation of CMOS library for IHP's and INFINEON's processes (14th month). To reach this milestone we have to generate library files, make characterization, and provide documentation. Without this library, further GALS fabrications won't be possible.
In WP4 we have planned a milestone in 19th month of the project. Until that deadline an internal version of software CAD tools (co-simulation software tools featuring the automated generation of Verilog co-simulation interfaces) should be available. This software tool is needed to start with the chip implementation planned in WP8.
In WP5 we have planned a milestone in 22nd month of the project. Until that deadline an internal version of software CAD tools (Release of internal version of tools, with a fully functional graphical IDE able to use IPs as defined in WP2 and the co-simulation tools from milestone 4.1) should be available. This software tool is needed to start with the chip implementation planned in WP8.
In WP6 we have planned three milestones. Firstly, we want to build mesochronous (15th month),and after that, a complete asynchronous (21st month) GALS NoC platform. Finally, we will make comparison between synchronous and GALS NoC approach (31st month).
WP7 also assembles three milestones. First is to generate and verify algorithms for EMI and power reduction with GALS (21st month). Second milestone is to develop architecture and circuit-level techniques for noise-and process variation-tolerant NoC design (29th month). Finally, we plan to fabricate test chip in order to evaluate developed algorithms (17 month).
Final milestone is in WP8, and according to this we have to tape-out Synchronous and GALS system examples in 45 nm CMOS process (29th month). Reaching this milestone will enable us to verify developed circuits, techniques and tools and collect final results of the project. Consequently, reaching this milestone is of key importance for the project success.

Tentative schedule of project reviews

Review no.	Tentative timing, i.e. after month X = end of reporting period	*planned venue of review*	*Comments, if any*
1	After project month: 6	Brussels, Belgium	
2	After project month: 12	Brussels, Belgium	
4	After project month: 24	Manchester, UK	
7	After project month: 36	Frankfurt (Oder), Germany	

B2. IMPLEMENTATION

B.2.1 MANAGEMENT STRUCTURE AND PROCEDURES

B.2.1.1 Overall approach to management

In order to guarantee the successful implementation of all GALAXY project goals, we will apply the following management methodology:

- Generation of a consortium agreement, that will define the access to and ownership of existing and future intellectual property used in the project, as soon as possible.
- Clear identification of all objectives, specifications, deliverables, and milestones.
- Generation of special plans for all objectives, specifications, deliverables, and milestones.
- Monitoring of project progress and establishing check/review points to prevent time delays and cost overruns.
- Efficient and periodic exchange of communication and ideas among the project partners, including technical status and quarterly project meetings.
- Initiation of appropriate corrective measures, whenever and wherever needed, and careful observation of high risk activities.
- Getting the formal confirmation from all project partners to fundamental documents at the different stages of the project preparation and execution.

B.2.1.2 Decision making mechanisms

We will establish within the project a Coordinating Committee (CC). Every member of consortium will delegate one member to CC. The role of committee will be:

- To monitor the project implementation and make decisions in order to meet the project plan and generate committed deliverables.
- To control the funding of the project
- To decide about the possible changes to the originally proposed project plan

Project decisions will be made by consensus. When consensus cannot be reached, decision will be made by consensus in CC. In case no consensus can be found the following procedure shall apply:

- If the conflict is of technical nature and has negligible impact on cost and/or time-schedule, the decision shall be taken by the Coordinator.

- If the conflict is of non-technical nature and has negligible impact on cost and/or time-schedule, the decision shall be taken by majority vote of the representatives in the CC present at the meeting.

- If the conflict is likely to have a non-negligible impact on cost and/or time-schedule, the decision shall be taken by weighted vote of all partners of the project. The weight of each vote shall correspond to the agreed project share prior the vote.

“Negligible” in this context means that the likely impact on cost and/or time remains within the normal planning accuracy of such undertakings. A Member which can show that its own work, time for performance, costs, liabilities, intellectual property rights or other legitimate interests would be severely affected by a decision of the Coordinating Committee may exercise a veto with respect to the corresponding decision or relevant part of the decision. When conflict between members appears we will follow procedure of conflict resolution described in 2.1.5.

The Coordinating Committee will organize a Management Support Team with the role to follow scientific, technical progress and management of the project on the daily basis. This committee will be open to any project member. Management Support Team will be chaired by the project coordinator and will be dedicated to the resolution of transient administrative and technical problems between the different work packages or affecting more than one work package.

Every work package will have designated WP leader. The role of the leader will be to monitor the progress and control decision making of the respective WP. WP leadership is distributed over the partners and normally is dedicated to the partner with leading activity in the respective WP. In this project we have the following WP leaders:

- WP 1 - Project Management: IHP
- WP 2 - GALS Interface Evaluation and Application Scenario : IHP
- WP 3 - Development of GALS IP library : STX
- WP 4 - Architecture for interoperability with external tools: UNIMAN
- WP 5 - GALS Integrated Design Environment: UNIMAN
- WP 6 - Application of GALS to NoC Environment: UNIBO
- WP 7 - Evaluating Advantages of GALS-based Design for Nanoscale Integrated Circuit Fabrication: EPFL
- WP 8 - GALS System Design and Evaluation: IHP
- WP 9 - Dissemination: INFINEON

While planning the management activities, proposing consortium bodies and decision-making mechanisms we have had in mind that all the structures for these procedures have to match the project type (STREP) and the number of participants. For such a size of project, the generation of any further management bodies will be far too expensive and ineffective. On the other hand, additional simplification of the management procedure would lead to incoherent project execution and potentially to an inability for fine-grained management actions.

B.2.1.3 Funding flow

Project coordinator (IHP) will coordinate also administrative activities and funding flow within the project. This will include the following:

- Contact with EC administrative officers regarding all financial issues and reports.
- Monitoring of resources used by the used by the partners (cost-statements).
- Distribution of the funding.

UNIBO, UNIMAN and STX will assist IHP in administrative management activities.

B.2.1.4 Communication among the project partners

The project coordinator (IHP) will provide following services during the project:

- Establish the exchange of the information between the project partners.
- Ensure the correct data and information flow among the project partners and between different work packages.
- Generate project documentation.
- Generate project minutes from CC meetings.

The project coordinator will enable project internal internet page serving for information distribution and support for the project partners. The project web page will consist of internal and external parts. The internal part will be open only to the project members and the external will be freely open. Internal project web-site will store all relevant project documents. This includes project proposal, technical reports, datasheets, technical documentations, minutes from the committee meetings, work schedules, deliverables and their drafts, project reports, contributions to forums and standardization bodies, scientific/technical publications and presentations. Our internal page will serve also as a server for exchanging the source code, software, etc. In this way we will enable effective synergy between the project partners and easier and more reliable common work.

We will also produce common project templates and guidelines for the project documentation. The purpose is to have a consistent and reliable framework for enabling project progress.

We will encourage direct project meetings in order to assure good cooperation between the partners

and ease the sharing of information. Initially we plan a kick-off meeting in order to enable project partners to know better each other and to discuss general project goals and deliverables. We also plan to organize regular CC meetings. If there is a need (for example, conflict in the project, difficulties in reaching milestones and delivering) special sessions will be organized. During the direct face-to-face meetings we plan to organize some social event to ensure that partners know better each other and overcome the problems related to work in different EU countries. Inside the work packages, internal work package meetings may be organized.

B.2.1.5 Changes to the project plan

Changes to the originally proposed plans have to be agreed on several levels. Changes from the originally proposed deliverables have to be agreed at a CC meeting and approved by the EU commission. Internal changes of the project plans have to be approved from the CC if the proposed change affects more than a single WP. If there is a change proposed within a single WP, which won't affect any other WP, the work package leader can approve this and all other partners via CC can be just informed about the change.

B.2.1.6 Resolution of conflicts

When conflict appears in consortium we have foreseen the following measures:

- If there is a conflict between two or more partners, the project coordinator will act as an intermediary in order to find solution and find the decision.
- If there is a conflict between the project coordinator and one or more partners, an independent person will be engaged to make the resolution of the project. Of course, this mediator will be obliged not to disclose the project information to third parties outside the project.

B.2.1.7 Legal aspects

In the framework of the project the project partners will mutually exchange some of IPs needed to implement project results. IPs that will be publicly available over project web-site will be freely available for non-commercial use. The exchange of other IPs will be the subject of non-disclosure agreements (NDA) and the consortium agreement.

B.2.2 Beneficiaries

B.2.2.1 IHP GmbH - Innovations for High Performance Microelectronics/ Institut fuer Innovative Mikroelektronik (Germany)

The IHP has a team of 204 R&D professionals with core competence in micro-electronics: process technology, circuit design, and systems. As a member institute of the Gottfried Wilhelm Leibniz Society, the core funding comes from the German Federal Government and the State Government of Brandenburg.

The institute aims to establish the area of East-Brandenburg as a high-tech region and to create jobs through innovation. Therefore IHP uses its R&D to enhance the competitiveness of German and European businesses and works closely with the Federal and State Governments to attract international companies to the region.

The institute is focussed on developing innovative solutions for wireless communication, particularly in the 5-80 GHz range. Its expertise ranges from system prototyping and circuit design to the implementation and optimisation of protocol stacks and the development of system-enabling CMOS-compatible technology modules. The IHP is focused on wireless communication with an emphasis on integrated solutions, building on European strengths to enhance leadership in rapidly growing areas. Within the Systems Department asynchronous circuit techniques are considered an enabling and supporting technology for 'Systems on Chip' solutions. In particular the EMC properties and the potential to save energy make asynchronous and GALS circuits promising candidates for implementing functions of the physical layer.

Currently, the IHP has joint R&D projects with over 30 companies. In December 1999 the institute has moved into a new building and has now one of the most modern infrastructures in Europe. This includes a clean-room with 0.25um and recent 0.13um high-speed BiCMOS technology.

Internally, IHP is establishing a culture that rewards excellence and risk-taking. This includes the use of rigorous benchmarking, portfolio analysis, and accomplishment reviews to measure the IHP results against the best. Most importantly, the IHP nurtures cross-disciplinary customer-focused teamwork. This customer driven activity culture is motivated by the fact that IHP's scientific peers judge its excellence, but its value is determined by the customers.

B.2.2.1.1 Short Resume of Key Persons to be Involved

- **Miloš KRSTIĆ** received the Dr-Ing. degree in electronics from Brandenburg University of Technology, Cottbus, Germany in 2006. Since 2001 he has been with IHP Microelectronics, Frankfurt (Oder), Germany, as a Research Associate in the Wireless Communication Systems Department. For the last few years, his work was mainly focused on low power digital design for wireless applications and globally-asynchronous locally-synchronous (GALS) methodologies for digital systems integration. His work was followed with more than 35 publications and 4 patent applications mainly in the area of GALS design and its application to the wireless communication area.
- **Eckhard GRASS** received the Dr.-Ing. degree in electronics from the Humboldt University Berlin, Germany, in 1992. He was a Visiting Research Fellow at Loughborough University, U.K., from 1993 to 1995, and a Senior Lecturer in Microelectronics at the University of Westminster, London, U.K., from 1995 to 1999. Since 1999, he has been with IHP GmbH, Frankfurt (Oder), Germany, leading a number of projects on the implementation of wireless broadband communication systems in the 5 GHz and 60 GHz bands. Since 2004, Dr. Grass is within the IHP, leader of a project on the development and implementation of a 60 GHz high data rate communication system. In this context asynchronous design techniques are being investigated and their potential advantages within the baseband processing are currently evaluated. E. Grass has registered four patents and published a number of papers - mainly in the areas of circuits for Wireless Communications and asynchronous circuit design.
- **Marcus EHRIG** received his diploma in information science from the Humboldt-University of Berlin in 2006. Since 2006 he has worked at the IHP Frankfurt (Oder), Germany. His research interests include design and FPGA/VLSI implementation of high performance algorithms for wireless broadband communication.

B.2.2.2 The University of Manchester (UK)

The Advanced Processor Technologies (APT) group in the School of Computer Science has made notable contributions to the development of asynchronous microprocessors, synthesis tools for asynchronous systems, chip multiprocessor architectures for the efficient support of Java virtual machines, and asynchronous signal processing systems. Funding has been secured both from the UK EPSRC and from various EU initiatives. Highlights of our work so far include:

- Amulet1 – developed within the OMI-MAP project (Esprit 5386) – was the first asynchronous implementation of a full commercial microprocessor architecture. This achievement was recognised with a 1995 BCS Award, and in the same year the Computing IT Gold Award for technology transfer (awarded jointly with ARM Limited).
- Amulet2e – developed within the OMI-DE/ARM project (Esprit 6909) – is an asynchronous embedded controller with performance and power-efficiency comparable with comparable clocked ARM processors exhibiting unique electromagnetic compatibility (EMC) properties and a true zero power idle mode.
- Amulet3 – developed within the OMI-DE2 and OMI-ATOM projects (ESPRIT 20452 & 23031) is a flexible high-performance asynchronous embedded subsystem for telecommunications. It was co-developed with Hagenuk GmbH.
- SPA – developed within the G3Card project (IST-199-13515) – was intended to evaluate the suitability of asynchronous processors to enhance the security of the device through its intrinsic resistance to power analysis and EMI attacks. The ARM compatible asynchronous processor was successfully synthesised entirely by the Balsa asynchronous synthesis system developed within the group.
- ASPIDA - produced an asynchronous open-source DLX processor – (IST-2002-37796). The demonstrator chip included a DI-encoded network-on-chip (CHAIN) which worked on first silicon
- Other EU funded projects in which the APT group has played a major part are: OMI-HORN (ESPRIT 7249), ExACT (ESPRIT 6143), PREST (ESPRIT 25242), ACiD1, 2, 3 (IST-1999-29119).
- Balsa is the leading open source high-level asynchronous system synthesis tool and has successfully been used for the DMA controller in the Amulet3 project and also synthesised the entire SPA microprocessor.

The group has regularly received substantial funding from the UK research body, EPSRC. The depth of its research expertise has been recognised by the award of a Platform grant followed by a prestigious 5 year Portfolio Partnership grant.

B.2.2.2.1 Short Resume of Key Persons to be Involved

- **Dr. Doug Edwards**, Senior Lecturer in the School of Computer Science, heads the work on Balsa, the leading publicly available system for the synthesis of large-scale asynchronous circuits. Dr. Edwards is one of a team of academics that was awarded a EPSRC Portfolio Partnership award (GR/S61270/01). Dr. Edwards is an author of over 50 papers and has been a co-investigator in 10 EPSRC funded projects. The review of the EPSRC funded work on Balsa rated the research “Internationally Leading” He headed the Manchester work on the ACiD, ExACT, and ASPIDA EU-funded research projects. Previous research interests have included Silicon Zinc Sulphide heterojunctions, high speed local area networks, hardware accelerators for CAD, formal verification of hardware. Current research interests include synthesis systems for asynchronous circuits, GALS and networks–on-chip for reconfigurable gate arrays.
- **Lilian Janin** is a Research Associate in the School of Computer Science at the University of Manchester, where he received his Ph.D. degree in 2004. His research interests are in simulation and visualization of large asynchronous systems. He has been working since 2000 on the asynchronous Balsa framework, and more specifically on the asynchronous simulator and visualization system. For the last few years, his work was mainly focused on a co-simulation debugging environment for heterogeneous synchronous-asynchronous circuits.

B.2.2.3 Ecole Polytechnique Fédérale de Lausanne (Switzerland)

Swiss Federal Institute of Technology Lausanne (EPFL) is one of the two federally-funded technical universities in Switzerland concentrating on research and teaching in several fields such as basic sciences, engineering sciences and techniques, computer and communication sciences, life sciences, architecture, civil and environmental engineering. EPFL offers undergraduate programs at bachelor and master level, and graduate programs at PhD level. Two research laboratories of the EPFL will be collaborating in this project:

The Microelectronics Systems Laboratory (LSM) operates as a part of the Institute of Microelectronics and Microsystems, concentrating its activities on design styles and methodologies for highly complex integrated systems, based on very deep sub-micron and nano-scale technologies. Recent research activities focus on the design and implementation of high-performance digital and mixed-signal VLSI circuits, language-based modelling and validation of System-on-Chip (SoC) components, intelligent (neural and neuro-fuzzy) system architectures, integrated photonic circuits for high-speed data links, design of highly error-tolerant systems with built-in redundancy and fault immunity for nano-scale microelectronic devices, circuit and system level power management techniques for complex SoCs, and design of high-speed data links for system-level interconnects.

The Integrated Systems Laboratory (Laboratoire des Systèmes Intégrés - LSI) studies design technologies for circuits and systems. One focus point is design technologies for silicon-based integrated systems and beyond. This area includes the modelling of hardware with dedicated languages, the compilation of hardware models into circuits, the relation between hardware and software design and its concurrent co-design, the system-level optimization from multiple standpoints (e.g., performance, energy consumption, yield). A second specialization is the design of reliable, safe and secure integrated systems. Research is centred on the combination of new device-level error-prone technologies within systems that must deliver a high level of dependability to the user. These new techniques have to be compatible with existing constraints for system integration, such as low energy consumption, which were not present in the design of large fault-tolerant systems of the past.

B.2.2.3.1 Short Resume of Key Persons to be Involved

- **Giovanni De Micheli** is Professor and Director of the Integrated Systems Centre at EPF Lausanne, Switzerland, and President of the Scientific Committee of CSEM, Neuchatel, Switzerland. Previously, he was Professor of Electrical Engineering at Stanford University. He holds a Nuclear Engineer degree (Politecnico di Milano, 1979), a M.S. and a Ph.D. degree in Electrical Engineering and Computer Science (University of California at Berkeley, 1980 and 1983). His research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis, hw/sw co-design and low-power design, as well as systems on heterogeneous platforms including electrical, optical, micromechanical and biological components. He is author of one book and co-author and/or co-editor of six other books and of over 300 technical articles. He is, or has been, member of the technical advisory board of several companies, including Magma Design Automation, Coware, Aplus Design Technologies, Ambit Design Systems and STMicroelectronics. He is a Fellow of ACM and IEEE.
- **Yusuf Leblebici** received the B.S. and M.S. degrees in electrical engineering from Istanbul Technical University in 1984 and 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990. Beginning in January 2002, Dr. Leblebici became a full (chair) professor at the Swiss Federal Institute of Technology in Lausanne (EPFL), and director of the newly established Microelectronic Systems Laboratory. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modelling and simulation of semiconductor devices, and VLSI reliability analysis. Dr. Leblebici is the co-author of two textbooks, as well as numerous scientific articles published in international journals and conferences.
- **Frank K. Gürkaynak** obtained his B.Sc. and M.Sc. degrees from Electrical and Electronical Engineering Department of the Istanbul Technical University in 1994 and 1997 respectively. He joined the Integrated Systems Laboratory (IIS) of ETH Zurich in 2000 and completed his Ph.D. thesis on GALS System design in 2006. He is currently with the Integrated Systems Laboratory (LSI) and Microelectronic Systems Laboratory (LSM) of the EPFL. His research interests include design of VLSI systems, full-custom design, globally-asynchronous locally-synchronous systems, cryptography, and Lab-on-Chip systems.

B.2.2.4 Alma Mater Studiorum - Università di Bologna (Italy)

The University of Bologna, created in 1088, is one of the largest in Italy (with more than 100,000 enrolled students). It is one of most active Italian universities in research and technology transfer. At European level, the University was partner in more than 150 EU projects in FP5 and FP6.

The UNIBO research group participating in the project belongs to the Department of Electronics, Computer Science and Systems (DEIS). DEIS is a research-led institute employing about 70 professors, 40 research associates, 90 doctorate students, 40 graduated research assistants, and several visiting researchers. The Department expertise spans the whole range of electronics, communications, computer science and biomedical engineering. The DEIS research group that will be involved in the project is the Multi-Processor System-on-Chip Group (Micrel Lab www-micrel.deis.unibo.it). The research activity of the group deals with the complexity of nanoscale Multi-Processor Systems-on-Chip (MPSoC) design, ranging from architecture-level issues up to parallel software design issues. The communication bottleneck has always been at the core of most research activities, dealing with power, performance and reliability implications of interconnect-dominated highly integrated MPSoCs.

The main achievements of the group have been in the domain of accurate modelling and simulation of MPSoC HW-SW platforms (resulting in the MPSIM virtual platform), in the development and analysis of Network-on-Chip communication architectures and in their crossbenchmarking with state-of-the-art system interconnect fabrics. In particular, the NoC-related activities of the group have led to the development of a mature fully synchronous Network-on-Chip architecture named “xpipes”. This was one of the first NoC solutions relying on a complete synthesis flow, from high-level specification all the way to layout generation.

The group has led several research projects (EU IST-ARTIST, IST-ARTIST2, ESPRIT-TTN Hipcom, National PRIN 2005, regional projects LAICA and SUMMIT) and industrial cooperation (with STMicroelectronics, Hewlett-Packard, Freescale Semiconductors) in the following project-related domains: design space exploration support, low-power and resource-aware embedded system design, communication architecture exploration in MPSoCs.

B.2.2.4.1 Short Resume of Key Persons to be Involved

- **Luca Benini** is a Full Professor at the University of Bologna. He also holds a visiting faculty position at the Ecole Polytecnique Federale de Lausanne (EPFL). He received a Ph.D. degree in electrical engineering from Stanford University in 1997. Dr. Benini's research interests range from multi-processor systems-on-chip/networks on chip to energy-efficient sensor networks. From there his research interests have spread into the fields of biochips and bioinformatics.
  He has published more than 300 papers in peer-reviewed international journals and conferences, three books (the most recent one on Networks on Chips), several book chapters and two patents. He has been program chair and vice-chair of Design Automation and Test in Europe Conference. He has been a Member of the 2003 MEDEA+ EDA roadmap committee 2003. He is a member of the IST Embedded System Technology Platform Initiative (ARTEMIS): working group on Design Methodologies, a Member of the Strategic Management Board of the ARTIST2 Network of Excellence on Embedded Systems and a Member of the Advisory group on Computing Systems of the IST Embedded Systems Unit.
  He is Associate Editor of the IEEE Transactions on Computer-Aided Design of Circuits and Systems and of the ACM Journal on Emerging Technologies in Computing Systems. He is a Fellow of the IEEE.
- **Davide Bertozzi** is Research Associate in the MPSoC research group led by Prof. Benini at University of Bologna. He is also Assistant Professor at University of Ferrara (Italy). He received his PhD in Electrical Engineering from University of Bologna in 2003.
  His research interests concern system level design issues for Multi-Processor Systems-on-Chip, with emphasis on the communication sub-system and on its interaction with the memory and I/O sub-systems. Most of his research efforts have been devoted to Network-on-Chip design, and he has been technical leader of the xpipes project.
  Dr Bertozzi has been visiting researcher at academic institutions (Stanford Universities) as well as semiconductor industries (NEC Research America, Philips Research Labs, STMicroelectronics, Samsung Electronics). He is a member of the technical program committee of several technical conferences and has recently published two chapters in the most recent book on Networks on Chips, and he will be program co-chair for the Int. Symposium on Networks-on-Chips 2008.

B.2.2.5 Silistix UK Limited (UK)

Silistix is a venture funded spinout from the APT group at the University of Manchester. The company was initially funded in Dec 2003 by a syndicate of UK investors, led by Intel Capital. Silistix now has almost 20 staff, with R&D located in Manchester, and Sales/Support primarily in San Jose, USA.

Silistix is the leader in commercial exploitation of GALS techniques with its CHAINworks toolsuite that allows commercial use of self-timed Network-on-Chip technology to interconnect IP-blocks that speak standard protocols, and using existing synchronous design flows.

B.2.2.5.1 Short Resume of Key Persons to be Involved

- **John Bainbridge** is the CTO of Silistix. He holds an MEng in Electronic Engineering and his British Computer Society Distinguished Dissertation Award winning PhD was received in 2000 from the University of Manchester, UK.

  John has worked on interconnect techniques for the past 10 years, which have been demonstrated on a number of working fabricated prototype chips and published in books, conferences and journals. He formed Silistix Ltd in 2003 to exploit the CHAIN self-timed networking technology that he developed as a postdoctoral Research Fellow.

  Dr Bainbridge is a member of several conference technical program committees, including the Async series and NoCs, both directly related to this project.

B.2.2.6 Infineon Technologies AG (Germany)

Infineon Technologies AG, Munich, Germany, offers semiconductor and system solutions addressing three central challenges to modern society including energy efficiency, mobility and security. In fiscal year 2006 (ending September), the company achieved sales of Euro 7.9 billion (including Qimonda sales of Euro 3.8 billion) with approximately 42,000 employees worldwide (including approximately 12,000 Qimonda employees). With a global presence, Infineon operates through its subsidiaries in the US from San Jose, CA, in the Asia-Pacific region from Singapore, and in Japan from Tokyo. Infineon is listed on the Frankfurt Stock Exchange and on the New York Stock Exchange (ticker symbol: IFX).

B.2.2.6.1 Short Resume of Key Persons to be Involved

- **Christoph Heer** is Senior Director at Infineon Technologies, responsible for the global development of standard components for large scale integrated digital circuits. Responsibilities include the definition of the technical roadmaps for future advanced CMOS technologies like 45nm, 32nm and below as well as the development of a productive design environment for the actual manufacturing technologies from 180nm down to 65nm. He is responsible for a global organisation with teams in Singapore, San Jose (California), Sophia Antipolis (France), Bangalore (India) and Munich (Germany). He received a Diploma degree in solid state electronics from Aachen University of Technology in 1990 and a Ph.D. degree in electrical engineering from Ulm University in 1995. Dr. Heer's research interests range from hardware architectures for dedicated signal and multimedia processing to circuit design for sub-100nm CMOS technologies. He has published more than 50 papers in peer-reviewed international journals and conferences and contributed to two books.

  Dr. Heer has been member of the technical program committee and organizing committee of several technical conferences, including the Design Automation Conference (DAC), Design and Test Europe (DATE) and the IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC).

  He has been teaching on asynchronous circuits at various universities in Germany, Spain and Australia. His lecture on “Asynchronous Design Methods” has been part of EPF Lausanne’s summer courses since ten years.

B.2.3 CONSORTIUM AS A WHOLE

The project consortium consists of very experienced partners in the areas related to the project. Therefore, the project tasks are clearly distributed to the partner with dominant expertise in a particular research field. Consequently, the tasks in each work packages are distributed such that there is a dedicated responsibility of every project partner for reaching the respective milestone and accomplishing the planned activities within WPs.

IHP, the University of Manchester, and Silistix have been active in the asynchronous and GALS community already for several years. IHP has much experience in synchronous and asynchronous chip design, fabrication, testing and GALS system implementations. Consequently, besides project management, IHP will cover the evaluation and optimization of GALS interfaces, explore EMI reduction with GALS, contribute to the GALS library and finally be dominantly involved in system implementation. Additionally, since IHP strategically develops high-end wireless communication systems it will not be difficult to provide the consortium with a suitable telecommunication IP ready to be GALSified.

The University of Manchester, on the other hand, has designed the Balsa that is the leading open source high-level asynchronous system synthesis tool. Hence, in the framework of this project they will be mainly involved in providing the CAD tools for the support of GALS design flow.

Silistix spans both territories relevant to this project: Asynchronous design and Network-on-Chip, and will in this project concentrate on challenges of GALS based on pausible clocking, and adding improved clocked/self-timed boundary support to their tools. That will strengthen the position of the company in distributing their product CHAINworks, a suite of software tools for the design and synthesis of customized on-chip interconnect using self-timed circuits.

In addition, we have in the consortium experienced partners in NoC research (EPFL and University of Bologna) that will strengthen our expertise in this very important research direction. The EPFL team is reinforced with the team member (Dr. Frank Gurkaynak) who originated from ETHZ, pioneers of GALS research in Europe. Therefore, they will here additionally focus on research in the area of low power GALS design. University of Bologna will, on the other hand, cover the nanoscale technology aspects with introduction of the GALS methodology and provide a research and exploration platform for GALS-based NoC design (xpipes). There is a strong collaboration between UNIBO and the Integrated Systems Laboratory (LSI) of EPFL on the NoC issue as members of both groups have developed the xpipes concept in collaboration over the past 10 years. In addition the Microelectronic Systems Laboratory (LSM) of the EPFL has significant experience in designing, fabricating and testing high performance digital and mixed signal integrated circuits. In this project we will use the experience of LSI and UNIBO for the front-end design aspects (specification, modelling, RTL design) and the design experience of the LSM for back-end aspects (verification, synthesis, place and route, testing) of the IC design.

Finally, the industrial partner Infineon Technologies will provide the consortium with industrial requirements for GALS interfaces and with support for an advanced 45 nm CMOS process. GALS methodology appears to be the right answer for many challenges present in design process for nanoscale technologies. However, until now there were no practical research activities covering GALS in conjunction with such advanced process technology. Therefore, the access to this leading edge 45 nm CMOS manufacturing technology is a key success factor for this project. Infineon's broad experience in different related subjects will improve the quality and impact of the project results.

The GALAXY consortium is balanced such that the complementary interests of the project partners are integrated in a homogenous partnership. In this project we will have IHP concentrated on architectural issues and chip design, INFINEON on technology support, UNIBO on GALS NoCs, UNIMAN on design flow support, EPFL on low-power issues with GALS, and STX on pausible issues. However, the wider expertise of partners will allow an effective exchange and distribution of the project deliverables and results between the tasks and work packages. The work plan of this project considers synchronized activities of several partners working on same tasks and in same work package. In addition, the extensive dependencies between the tasks and work packages will reinforce collaboration between the partners and generate the synergy in the project.

The project tasks are clearly distributed to the partner with dominant expertise in respective field. Therefore, we see this project consortium as complementary oriented regarding the partners' focus on different project tasks. However, we have foreseen an important level of synergy between the tasks and work packages in order to have a coherent project development.

The distribution of the effort amongst the partners shows that the expected output of all partners in the project should be very significant for reaching the project results. In this consortium there is no partner with just a marginal contribution to the fulfilment of project goals.

Another important point is the industrial exploitation of the project results. Our consortium is well balanced with three academic partners (UNIMAN, UNIBO, EPFL), one research institute (IHP), one SME (Silistix) and one large scale industry partner (INFINEON). The industrial exploitation of the project results is insured, on one hand, by Silistix, as young and growing company, providing CAD services and interfaces for SoC design. On the other hand, Infineon Technologies will, as leader in semiconductor business, guarantee commercial utilization of the research results achieved throughout this project.

In general, all project partners were working or even leading previous EC funded research projects. Additionally, some members of consortium have already good experience in working together on different subjects. For example, IHP and the University of Manchester were in the ASPIDA project consortium, that implemented an asynchronous DLX processor, funded under EU framework programme FP6. Also EPFL and University of Bologna have strong collaboration in the research in NoC area. The University of Manchester, IHP and Infineon Technologies were part of Working Group on Asynchronous Circuit Design (ACiD-WG) under Framework Programme FP5 Microelectronics, FP4 Technologies for Components and Subsystems and FP3 Basic Research. All those common activities resulted in very valuable outputs and created strong informal connections between the partners. Therefore, we are very confident that in the context of the GALAXY project this consortium can create excellent synergy and deliver very important results.

The GALAXY project consortium consists of six partners as already mentioned. They are from three different EU members (UK, Germany, Italy) and from one associated county (Switzerland). With such workload distribution we will be able to strengthen the European competitiveness on a wider level in the respective research areas. In the framework of this project we do not plan the involvement of any subcontractor or any legal entity outside the EU member states and associated countries.

B.2.3.1 Sub-contracting

Subcontracting costs include costs related to the production of Certificates of Financial Statements (CFS), as required by FP7 rules, for partners IHP, STX, EPFL, and UNIBO. The subcontracting costs related to CFS are foreseen with 14400 € in total.

B.2.4 RESOURCES TO BE COMMITTED

The members of consortium will commit many additional resources in order to reach the project goals and improve the excellence of the project. In the following sections, a retrospective of the complementary resources will be given:

- **IHP –** In the framework of the GALAXY project IHP will make available to the project the chip fabrication facilities supporting 0.25 um and 0.13 um CMOS process. IHP will provide communication IP cores (baseband processing for 60 GHz PHY) for the design example of GALS design flow. Additionally, for the personnel working in the project we will enable the use of CAD tools, design flow for chip design and PCB design in order to perform the tasks defined by the project. In order to verify the project results we will use our test facilities (Verigy 93000 tester) for packaged and on-wafer tests and measurements. In addition, depending on the project needs, we will utilize the other equipment such as logic analyzers, oscilloscopes, Advantest CertiMAX test system, Verisity Axis emulator, various measurement equipment, etc.
- **UNIMAN –** will use commercial CAD tools that are already licensed to the APT group and make available demonstrator boards with large Xilinx FPGA devices for prototyping. A 44 core, Opteron based, high performance computing cluster is available for simulation. The group is involved in a number of related projects that will provide undoubted synergy and a critical mass of expertise, for example: Asynchronous Datapath and System Synthesis (extending the Balsa system), Energy-Efficient NoCs for Reconfigurable Computing Platforms (joint with Bristol University, UK) and "Meeting the Design Challenges of Nano-CMOS Electronics". The latter activity is part of a collaborative £3M EPSRC funded project investigating the impact of uncorrelated variability in deep sub micron semiconductor processes.
- **EPFL –** Within the GALAXY project, EPFL will use its extensive background in IC design, verification and testing. This will be supported by a state of the art computer infrastructure which has all major EDA software installed. EPFL has significant experience in testing fabricated ICs and has an adequately equipped laboratory for this purpose. We believe that the GALAXY project will greatly benefit from the design experience of EPFL members in GALS based systems, low-power design, network on chips and verification.
- **UNIBO –** University of Bologna will complement the EC contribution by making his NoC architecture available as a research and exploration platform to achieve the project's goals. Moreover, the network building blocks will be available in the context of a virtual platform which allows for IP core integration and attachment to the network, for automatic statistics collection, for functional traffic injection, for memory architecture exploration and, more in general, for design space exploration. This will save months if not years of work and provide an ideal modelling and simulation environment right at the beginning of the project. Moreover, the xpipes NoC architecture allows the project to start investigating GALS implementations right away and even to compare them with a mature synchronous implementation.
- **STX –** Silistix already allow access to their tools and technology to UNIMAN and this relationship will continue through this project, allowing self-timed NoC IP blocks and protocol converters to be used as units for trialling the design-tools created by UNIMAN.
- **INFINEON –** For the members of GALAXY project consortium INFINEON will provide a standard ASIC development kit for their advanced 45nm CMOS manufacturing platform. The opportunity for test chips and silicon verification of the developed components and systems will be available for the consortium.

It is planned that GALAXY project utilizes the following personnel and indirect resources per beneficiary:

- **IHP (73 person months, requested EC contribution ~ 635 T€) –** Planned personnel and indirect cost will be used for management and RTD activities. IHP as administrative and technical coordinator of the project has to utilize reasonable staff needed for management tasks (15 person months). Additionally, IHP has to cover important RTD tasks such as GALS interface specification (WP2; 12 person months), additional cell generation for 130 nm CMOS process (WP3; 4 person months), support for GALS design & test flow (WP5; 7 person months), exploration of EMI reduction with GALS methods (WP7; 14 person months), fabrication & testing of synchronous and GALS complex chip in 45 nm CMOS process (WP8; 20 person months), and finally dissemination (WP9; 1 person months).

- **UNIMAN (74.7 person months, requested EC contribution ~ 570 T€) –** Planned personnel and indirect cost will be used for RTD activities and to the very small extent (1.1 person months) for management activities. Most of its efforts UNIMAN will concentrate on software tools development (WP3, WP4, WP5, WP8; 62 person months) needed to establish GALS design flow. Those deliverables are of highest importance for this project. Additionally, they will work on asynchronous IP packaging (WP2; 3 person months), GALS libraries (WP3; 5.6 person months) and dissemination and exploitation (WP9; 3 person months).
- **EPFL (42.7 person months, requested EC contribution ~ 410 T€) –** In the GALAXY project EPFL will be intensively involved in exploring low-power properties of GALS methods (WP7; 12 person months), and GALS application to NoC (WP3, WP6, WP5, WP8; 16.7 person months; this is a common work of UNIBO and EPFL). Additionally, they will support chip fabrications (WP7, WP8; 5 person months), in support for the GALS interfaces design & test flow (WP2, WP5; 7 person months), and in dissemination (WP9; 2 person months).
- **UNIBO (44 person months, requested EC contribution ~ 385 T€) –** Planned personnel and indirect cost will be used for RTD activities and to the very small extent (1 person month) for management activities. UNIBO will mostly cover GALS application to NoC (WP3, WP6, WP5, WP8, together with EPFL; 35 person months), process variation tolerance in GALS circuits (WP7; 6 person months), and dissemination (WP9; 2 person months).
- **STX (37.5 person months, requested EC contribution ~ 510 T€) –** Planned personnel and indirect cost will be used for RTD activities and to the very small extent (0,5 person months) for management activities. STX will be engaged for the work on calibration and jitter control circuits for pausible clocking (WP3; 15 person months) and design of clocked CHAINworks components and NoC interfaces development (WP6; 8 person months) and investigation of techniques to mitigate process-variation in self-timed NoC transport layer (WP7; 6 person months). Additionally they will support IP packaging (WP2; 2 person months), and design & test flow tutorials (WP5; 3 person months). They have also significant role in exploitation of project deliverables and dissemination (WP9; 2 person months) and in generating requirements for asynchronous cell generation (WP9; 1 person month).
- **INFINEON (40.7 person months, requested EC contribution ~ 395 T€) –** The main contribution of INFINEON will be the support for their advanced 45 nm CMOS process (WP6, WP7, WP8; 13.7 person months) and generation of additional standard cells for this process (WP3; 12 person months). The later task will especially require increased personnel utilization since it is planned to generate extended set of the asynchronous cells with different driving capabilities followed with specification of the cell characterization. Additionally they will heavily involved in providing industrial requirements for interface specifications (WP2; 6 person months), tools (WP4; 3 person months), design & test flow (WP5; 3 person months). Finally, they are the key partner in dissemination and commercial exploitation (WP9; 3 person months).

Subcontracting costs are planned only for financing the external audits for the Certificate on Financial Statements (CFS) required from EC.

In order to fulfil the milestones and deliver the project results defined in section B.1.3 we have requested additional funding for the chip fabrications foreseen in WP8 and WP7. In WP7 we have planned to fabricate a relatively simple test chip in a 0.13 um CMOS process in order to pre-evaluate the effectiveness of our EMI and power reduction methods and to fabricate various test structures. The estimated cost of this fabrication is around 10 k€ and additional small spending is needed for chip packaging. Additionally, we have planned parallel implementation of two evaluation chips (one GALS and one equivalent synchronous design) and various test structures in a 45 nm CMOS process. The estimated cost of those fabrications is 85 k€. Additionally, to properly test those chips, we need to order a probe card with the cost around 3 k€ and to reserve some budget for chip packaging. All project partners will request also some funding needed to attend the project meetings and to disseminate project results by attending the conferences. The chip fabrication is of key importance for verification of the results of the project. The GALS methodology appears to be the right choice for nanoscale technology, but until now there have not been any practical experiments in a process more advanced then 130 nm. Therefore the funding of those chip fabrications is of high importance for the success of the project. In the following text there is a summary of the other direct costs needed to fulfil the project goals. More details can be found in GPFs.

IHP other direct cost table	**total**	**43.573,97€**
Test chip fabrication (0.13 um CMOS)		10.000€
Probe card for testing the chips, Chip packaging		5.500€
Project meetings, other mng. cost, conferences, summerschool speakers cost		28.073,97€
UNIMAN other direct cost table	**total**	**37.842€**
Project meetings, other management cost and conferences		27.842€
Workstations + filestore		10.000€
EPFL other direct cost table	**total**	**40.500€**
Project meetings, conferences and partner visits for collaboration		23.500€
FPGA board/ PCB for adapting the test chips to the FPGA		17.000€
UNIBO other direct cost table	**total**	**38.000€**
Project meetings and conferences		23.000€
Equipment (computation power enhancement for the simulation)		15.000€
STX other direct cost table	**total**	**23.000€**
Project meetings and conferences		23.000€
INFINEON other direct cost table	**total**	**85.000€**
GALS, Sync, various test structures chip fabrications (45 nm CMOS)		85.000€

The overall cost of the project (provided in GPF) together with staff effort (shown in section B.1.3) and complementary costs provided from partners are integrated in coherent way and used for fulfilling the variety of tasks including management, dissemination, simulation, modelling, software design, hardware design, chip fabrication, testing and measurement. The overall financial plan includes the optimum of the cost needed to fulfilling the planned tasks. The additional cost contribution request from the EC relates only to financing of the fabrication of the needed chips, activities for dissemination (attendance to conferences, workshops, etc.), and support for management tasks (travel funds for partners attending project meetings).

In order to estimate our staff efforts needed to fulfil the project tasks we were guided with the great experience that partners have in similar size EU and national projects. UNIMAN and IHP were together partners in EU project ASPIDA dealing with asynchronous system design and funded in framework FP6. IHP has additionally very broad experience in chip designs and fabrication and estimation of time needed for implementations of such activities. EPFL and UNIBO are also active in the several projects with NoC topics. Finally, for this process the technology support will be provided from Infineon. They are able to precisely identify the efforts needed for their contribution to the project since they have to co-finance all tasks together with EC on 50-50% basis. To conclude, the staff effort requested in this project represents a fair match to the complexity of the project tasks.

For the estimation of the other direct cost of the project we were using the numbers extracted from the real quotations. For example, the estimation of the chip fabrication cost is based on the prices provided from Europractice web-site (http://www.europractice-ic.com/prices.php) for the academic and research institutions. The costs for the probe card and chip packaging are determined from previous quotations of the similar products. The travel costs are estimated as fair represent of average continental flight price, standard hotel room costs and possible conference fee (this cost is not calculated for project meeting travels).

Finally, the project plan has been devised such that no double funding is requested and that responsibilities of all partners in work packages are clearly distributed. The planned efforts from different project partners are used in a complementary way. Therefore, the results of some activities produced from one partner are the basis for other partners' work in further activities. For example, the IHP work in the system design work package (WP8) relies on UNIMAN results in WP4 and WP5, but also it integrates the results achieved from EPFL and UNIBO in WP6 and WP7, and uses technology support from INFINEON. In this way we will effectively reuse the resources of the project, improve coherence of activities and improve the synergy among the partners.

B3. POTENTIAL IMPACT

B.3.1 STRATEGIC IMPACT

B.3.1.1 Impact expected from GALAXY project

In the framework of this project, it is expected that we meet all requirements defined by the call 3.3. This project should result in a reliable and user friendly design flow for GALS-based complex digital systems. Then we will be able to effectively GALSify complex digital designs and reduce the system integration problems and additionally improve different design parameters (EMI, security, power, etc.). With this approach we will be able to cope with modular heterogeneous systems using simple asynchronous interfaces. The realization of such an ambitious goal will result in improved design-to-market time, fewer design iterations and finally in a lower cost of the system design process.

The GALS design flow is currently not integrated and GALS circuits are not frequently utilized in industry. Enabling designers to freely use the GALS methodology, offering optimized interfaces for particular applications, and evaluating the advantages of a GALS technique will enormously increase the chances that GALS becomes the leading interface technique. The industrial support that we have within the project will guarantee utilization of the project results and improve competitiveness of European companies in design and integration of embedded digital systems. The effective application of GALS methodology will result in reduced design costs.

This project covers several innovative issues summarized in following text:

- The main point is the implementation of the automated and integrated GALS design flow that is completely missing at present.
- We plan optimization of GALS interfaces and especially improvements in pausible clocking calibration mechanisms.
- Additionally, in the context of the project, we will explore the EMI and power reduction possible with GALS circuits. Until now, these subjects have been covered just marginally or only at the theoretical level.
- We will also explore the transition from conservative synchronous implementations of NoCs to GALS compliant NoCs.
- GALS design has not previously been explored for deep submicron technologies. The main results of the effectiveness of GALS are based up to now on almost obsolete 0.25 um processes although some new results were achieved in 0.13 um CMOS process implementations. The system design in a 45 nm CMOS process will give completely new value to the achieved results.
- Process improvements introduces additional and, up to now, unsolved challenges such as variability and reliability. These issues and how a GALS methodology can solve such challenges will be covered in this project. The elaborated concepts will be proven in practice.

To conclude, the number of innovative points in this project is high and this will make certain that the project results make a large impact.

In order to achieve this expected impact, we have foreseen the following steps:

- To maintain the excellence of the project results we will have careful project planning, monitoring and control of the challenging issues.
- To follow and anticipate the major factors that can affect the impact of the project results, numbered in subsection B.3.1.4. The management of the project will be flexible enough to handle the emerging external factors affecting the impact of the project results and consequently adapt the emphasis to the respective project activities.
- In order to increase the impact of the project, we will motivate all activities leading to increased dissemination and commercial and non-commercial utilization of project results.

The GALAXY project has also ambition to further confirm leadership of Europe in a GALS system-on-chip design and CAD support. This leadership is already established with previous realization of complex asynchronous and GALS demonstrators (AMULET chips, GALS chips from ETHZ (CH), IHP, and LETI (FR)) and tools developed by UNIMAN, TIMA (FR), Universitat Politècnica de Catalunya (ES), and Handshake Solutions (NL). In the project consortium we have a company Silistix (UK) with a strategy to develop and distribute the software tools for the design and synthesis of customized on-chip interconnect using self-timed (clock-less) circuits. With the success of this project, Silistix will be able to further improve its position in a world market of CAD providers for embedded system design tools. As a leading player in the semiconductor market, Infineon Technologies will further utilize and promote the results of the project. The involvement of a large industrial partner will guarantee the success of the project and the impact to the embedded system design methodology and practice. However, the competitive level of USA companies and universities in this field is also very strong. Therefore, with the results of this project the European institutions and companies will be able to remain in very completive position in the area of complex system design. Additionally, we will enhance the synergy between the leading European research institutions in this area.

B.3.1.2 Necessity for European level project

There are several reasons why this topic cannot be successfully covered by any national research program:

National based projects cannot cover the GALS topic with enough capacity. Research activities in Europe in this field are widespread. This project consortium assembles the European leaders in the targeted subject: EPFL and UNIBO are leaders in NoC research, IHP is in a very good position regarding GALS research and its application to wireless communication, UNIMAN is one of the founders of the asynchronous research in Europe and the leading partner in CAD tool development for asynchronous circuit design. From the industry side in consortium we have STX as an established company in the GALS NoC field, and semiconductor industry leader, Infineon Technologies. This project also has the potential to improve the synergy between the leading European research institutions in this subject. Therefore, the national based project on GALS, as it was proven in the past, can give only very limited results.

Europe is together with USA in the lead in asynchronous and GALS research and this position has to be further confirmed. The importance of GALS subject is beyond the level of national interest and there are strong research activities across the world. Therefore, Europe can be the leader only if we unite our strengths and capacities in a common project framework.

B.3.1.3 Other research activities tackling the GALS paradigm

In the previous years there have been several projects directly or indirectly dealing with GALS as a subject. They were mainly funded on a national level and the results were also limited.

- **"VLSI Structures for Globally Asynchronous Locally Synchronous Systems"** was a joint project between the Universities of Manchester and Cambridge, funded by EPSRC. The objective was, inter alia, to investigate novel circuits and design techniques for a GALS approach to deep sub-micron design. Cambridge devised a novel clock distribution scheme using asynchronous circuits, Manchester investigated ternary logic asynchronous networks-on-chip.
- **ESPRESSO**, Synchronous programming for the trusted component-based engineering of embedded systems and mission-critical systems, Consortium: CNRS, INSA of Rennes, University of Rennes, France (http://www.inria.fr/rapportsactivite/RA2005/espresso/uid76.html), (2003 - 2005). This project marginally covered GALS topic focusing on synthesis of GALS architectures. However, the results of the project and impact of this project were relatively low in the area of GALS.
- **Modelling and Analysis of Globally Asynchronous Locally Synchronous (GALS) Systems** (2005) (http://www2.informatik.hu-berlin.de/top/forschung/archiv/gals/index.php), funded by the German Research Council (DFG), Consortium included Humboldt-Universität zu Berlin and IHP Frankfurt (Oder) Germany. This project was funded for relatively short time and the main activities were performed at Humboldt-Universität zu Berlin. Mainly this work included formal verification and modelling of GALS wrappers. However, the impact of this project was relatively limited.

- **Design and implementation of communication systems using the GALS approach**, project implemented at Linköpings University, Sweden (2004 - 2005?) - (http://www.tde.isy.liu.se/projects/GALS/). This project resulted in several interesting publication in GALS area. However, we have no further information about this project.
- **Asynchronous Array of Simple Processors (AsAP) project**, Project realized at University of Davis, USA, (http://www.ece.ucdavis.edu/vcl/asap/). This project was supported by Intel Corporation, UC MICRO, the National Science Foundation under Grant No. 0430090, and a UCD Faculty Research Grant. (-2006?). The goal of this project was development of GALS array of simple processors. As a result they have fabricated ASIC chip that assembles a mesh 6 X 6 of such processors. As a demonstration this structure was used for implementing structure able to perform transmitter functionality compliant to IEEE 802.11a standard.
- **GALS project ETHZ,** The Integrated Systems Laboratory (IIS) of the Swiss Federal Institute of Technology has worked on GALS system design from 1998 until 2006. The work has resulted in the implementation of several working GALS chips, most notably Marilyn (the first working GALS demonstrator), Shir-Khan (a GALS interconnect testbed with 26 interconnected processors) and Acacia (a GALS based cryptographic engine). As part of the project, advanced pausible clock generators were developed and practical implementation issues such as design flow and testing have been addressed. Detailed information can be found under the www site of the project (http://gals.ethz.ch)
- **NEVA-FAUST project,** Project currently running at LETI, ACE, Bull, Certess, LETI / CEA, LIACS / Univ. of Leiden, Philips, Silicomp, STMicroelectronics, TIMA / INPG and VERIMAG / UJF (2005-2008). The project goal is to build multi-processor platform based on NoC paradigm including support for asynchronous (and GALS) communication between the components. Target is computing power around one giga operations per second per chip

B.3.1.4 Factors affecting impact of the GALAXY project

There are several factors that may affect the impact of GALAXY project. One major threat to the impact of the GALAXY project is based on the future of NoC concept. NoC at the moment represents a clear application target for GALS systems and methodology. With the major success of the NoC paradigm and its great commercial utilization, we can estimate a major impact of the results of this project. On the other hand, if the NoC concept is applied in the future just marginally or seldom, the GALS concept has to look for an independent future as the interconnect mechanism. However, even in this case, it is quite probable that GALS will be a strong system integration option, but probably the implementation target has to be adapted and changed. In addition, increasing industrial interest in NoCs (e.g., NXP, STMicroelectronics, Intel and Silistix, Arteris, Teklatech among the SMEs) and the proliferation of international events (conferences, journal special issues, tutorial sessions, invited paper sessions) focusing on NoCs make it reasonable to envisage the success of the NoC paradigm.

The targeted impact of the GALS design flow developed in the framework of this project looks currently very likely to happen. However, there is a slight possibility that some of the major CAD providers for synchronous design tools will also cover in their future releases some aspects of GALS design flows. If this happens, this can to some extent diminish the impact of the results of our project, as our tools will not be required as much as they are now. However, having in mind the current trend, this is relatively unlikely to come soon. The support for a GALS design flow appearing in commercial releases will be an option only after GALS is established as a relevant and frequently used design technique in commercial products. Since currently this is not the case we expect that the coverage of a GALS design flow in commercial tool sets will come with significant delay in comparison to the results of this project. Also, if commercial CAD vendors happen to extend their tools towards GALS, the open-source aspect of our framework will always make it attractive to a large audience unable or unwilling to invest in commercial CAD tools.

The only commercial CAD provider for the asynchronous design flow is currently Handshake Solutions (spin-off from Philips). They are currently very much oriented toward pure asynchronous design flow and not entirely targeting mixed asynchronous-synchronous design environment. It is possible that the impact of our design flow is affected by some commercial tool provided from HS covers the GALS topic during project implementation. However, there are no indications for this in the moment.

We have already described in the Section B.1 why GALS is not already leading interface technology. In the framework of this project, we have concentrated on demonstrating the

competitiveness of GALS methods in comparison with standard synchronous solutions for system integration in nanoscale process environments. The additional issues that we will address are the superior EMI characteristics and low-power potentials of GALS methods. If we do not achieve satisfactory results in this respect, the impact of the project will be certainly be lower. However, the initial theoretical explorations of those issues, as described in Section B.1, show great potential of the GALS interfaces. Therefore, we anticipate that the practical results of the project will confirm our results.

Finally, we can estimate as a potential danger to the impact of this project, an enormous success of some parallel approach that is currently conducted in other institutions (for example, the NEVA-FAUST approach, or some USA-funded project). This may mean that the results of our project are not exploited well enough and some other approach takes the market. The GALAXY project consortium, on the other hand, assembles leading research institution in the field, the University of Manchester (design flow), IHP (GALS design), EPFL (NoC and GALS), University of Bologna (NoC), Silistix (GALS NoC commercial products), Infineon Technologies (leading semiconductor industry). This project consortium guarantees competitive results of the project and enables the successful impact of the project.

In order to anticipate the factors affecting the impact and generate the adequate actions to minimize the risks we will have frequent project management meetings. Therefore, we will be able to take the decisions leading to increased impact of the project results. Additionally, we will support any way of dissemination of the project results such as submission of papers to conferences and journals, attending the forums, taking part in trade exhibitions, etc.

B.3.2 DISSEMINATION AND/OR EXPLOITATION OF PROJECT RESULTS, AND MANAGEMENT OF INTELLECTUAL PROPERTY

B.3.2.1 Popularization of GALS methodology

One of the most important goals of this project is to popularize GALS methodology and techniques. GALS techniques have not been utilized much outside the asynchronous community until now. One of the major reasons for this is that asynchronous design as such was difficult for inexperienced designers due to the assumed (or real) immaturity of the CAD tools. In the framework of this project we will try to break those prejudices and to organize events and create tutorials that will make asynchronous and GALS design closer to the designers.

We will therefore take part in the summer schools and workshops to present the GALS design flow and advantages of GALS techniques for the complex system integrations to the students and engineers. The project partners will be invited to those events to present their results and visions of the GALS future. Also we will try to invite eminent scientists working in this area to contribute to the success of such events.

One of the summer schools that we target for distributing knowledge about GALS methodology is annual summer school of microelectronics held in Frankfurt (Oder), Germany (http://www.kme-ffo.de). This event is additionally important because it is targeted at talented PhD students from eastern European countries. The asynchronous community currently is very strong in the so-called "old Europe", the main centres being in UK, France, Italy, Spain, Switzerland, Germany and the Netherlands. However, the asynchronous community in the eastern countries was up to now weak or nonexistent. With our efforts targeted to this summer school we expect to reach two very important goals. One is to generally popularize GALS idea, and the other, not less important, to build a solid base for GALS and asynchronous research in the new European countries.

Additionally, we will generate appropriate tutorials and technical documentation on how to use the design flow proposed within project. That information will be freely available over the project web-site for download. The information provided this way will be clearly presented and should be easy for understanding even for inexperienced designers. Members of the project will offer also technical support to the institutions and individuals facing some problems while using proposed GALS CAD tools. We will additionally try to generate design scripts (for example for synthesis and layout) that should enable easy adaptation of standard CAD tools to the GALS design process

One of the important tasks within the project is to establish library of GALS IPs. This library will allow easy integration of the GALS components into the standard synchronous environment. The library elements will be on the level of hard macros and transistor-level components (standard cells, handshake components, ready-made GALS interfaces, etc.), netlists (verilog) and scalable behavioural source code (Balsa, verilog, VHDL). For technology dependent part of the offered IP library we will use IHP CMOS process. This process is available for European universities and research institutions over Europractice with discounted prices. Therefore, we will enable further exploitation of the project results to the other institutions as well.

Our project page will not be only used for representing project results and enabling users to use project results. We see also this page as an open forum for the user to exchange their IPs, tools, design experiences and elaborate possible problems with using GALS design. It is expected that the possibilities that we will freely offer over the web-page, including support for design flow, IPs and tools, will attract large design community and individuals. Consequently, we expect that our design and tool library will be significantly extended from the user's side.

In order to increase the impact of the project we have foreseen the following measures for general press publicity:

- We will promote the results of our project in the media. We will try to publish the news sourced from our project in the related popular technology press (such as EE Times).
- One important aspect of our public relation will be the publications in the local media of the project participants. In this way we will not only promote the results of the project, but also promote the values of European Union and importance of scientific support coming from EU. In particular IHP, UNIMAN and STX will have ambitious plan for communication with the local media from Manchester and Frankfurt (Oder). Financing coming from EU have special

importance for those two cities. In the framework of the GALAXY project Manchester will have two beneficiaries. Similarly, for Frankfurt (Oder) is the investment in new technological development an important chance to cope with high unemployment rate.

- We will try to popularize our online GALS IP library (results from WP3) by putting advertisements and links in the relevant internet forums (The Asynchronous Logic Home Page, OpenCores, etc.) and in general web-sites and press. The major goal is to popularize the application of software, source code and tutorials given in our GALS IP library.

We expect the above mentioned actions and measures will strongly popularize GALS design flow and methods. Therefore, as a result of the project we expect that our tools and components will be widely used in the European research institutions and academies. Also we expect that our open core approach will attract many interested researchers and that their effort will further extend the results of the project.

B.3.2.2 Publication of achieved results

It is expected that this project will result in large number of published papers. We will strongly support submitting of the papers to the eminent conferences in Europe and in the world. There are several reasons behind this strategic decision. One is naturally to present the results of the project. The other is to influence the research community and popularize GALS methods and tools in general. An additional, but no less important, target will be submitting the comprehensive project results to the important journals and transactions. Members of the project consortium have already good reputation regarding the number and the quality of publications and therefore it is plausible to expect that this project will result in a large number of high quality papers.

B.3.2.3 GALS applied in NoC environment

High clock speeds and the increasing performance variability of new technologies are making strict global synchrony prohibitively difficult to implement in large chips. Increasingly complex clock distribution techniques used to minimize clock skew (e.g., distributed active skew control) do not seem to be the answer, since they are taking an increasing portion of total power consumption. Ultimately, failure to live up to the challenges of implementing a clocking signal properly may render an entire chip dysfunctional, e.g. due to hold time violations. However, getting a 50M gate chip to run synchronously is a difficult and time consuming undertaking, if at all possible. Today it can be reasonably envisioned that an effective solution to this problem for the near future is to secure timing integrity locally while maintaining a globally synchronous system perspective. Globally Asynchronous, Locally Synchronous (GALS) methodology allows clusters of IPs to be grouped into “islands of synchronicity”, and to run asynchronously between the clusters. The GALS approach is a practical way to improve the back-end time spent achieving timing convergence, while keeping design style and flow unchanged.

Networks on chips potentially suffer from the same clocking concerns of sequential logic, since they are global interconnect fabrics which are distributed across the entire chip, and since the majority of them is implemented in a synchronous design style. GALS methodologies can therefore relieve clocking concerns for network building blocks, and pave the way for the success of NoCs as reference industry-viable solutions for system-level interconnection in nanoscale MPSoCs. This is in fact the ambitious goal of this project, which includes activities aiming at removing major barriers to make this scenario come true. Firstly, design technology advances will allow for automated generation of GALS NoCs, relieving design productivity concerns. Secondly, architecture and circuit level solutions for process variation tolerance and communication reliability will relieve concerns on applicability of GALS interconnect solutions to nanoscale technologies.

More interestingly, such critical advances and findings of the project for the NoC community will be derived through an academic exploration virtual platform, thus paving the way for a facilitated dissemination of the results and a future potential broader sharing of them with academic and industrial entities. Therefore, the dissemination objectives of the project are inherent in the choice of xpipes as the reference fully synchronous NoC architecture to GALSify. In addition, the crossbenchmarking activity comparing a fully synchronous NoC and a GALS architecture implementing some of the most promising techniques explored throughout the project will allow the real case for GALS technology in the NoC domain to be made.

Recently, new international events have been scheduled, specifically targeting on-chip networks. In particular, the International Symposium on Networks-on-Chip (first time in May 2007) brings together academic and industrial researchers and developers addressing issues of NoC-based systems at all

levels, from the physical on-chip link level through the network level, and ranging up to system architecture and application software. We intend to take the maximum advantage of this event for presenting project findings and developed tools and techniques, given its unprecedented potential for networking with the entire NoC community. In addition, all major conferences and journals are increasingly devoting time and space to NoC-related topics (e.g., NoC tutorial at DATE 2007, TVLSI special section on NoCs, Special Issue on NoCs on Hindawi VLSI Design Journal); we intend to contribute to them through the outcomes of this project.

B.3.2.4 Plan for the exploitation of the project results

During the project span it is planned to generate many deliverables of different nature. In principle, we can classify the expected foreground in four different categories. For each of these categories, we have prepared an appropriate exploitation plan.

The major project deliverables are CAD software tools (generated in WP4 and WP5) intended for establishing the interoperability framework. As it is specified in section B.1.3.4, this software will be offered freely over our GALS web forum. However, this plan doesn't prevent the commercial exploitation of these CAD tools. In fact, with the expected growing interest from software users (partially caused from license-free software use), the commercial exploitation can be achieved by providing a technical support, by offering additional tool features on non-free basis, etc. As described in B.3.2.5.2 below, the University of Manchester, School of Computer Science has an excellent record in exploiting its research, either by software licensing or by the formation of "spin-off" companies. We expect that the results of this project (software for GALS design flow, deliverables D10, D31, and D19) would form the basis for such exploitation.

The second category of exploitable deliverables are the developed GALS circuits, algorithms, and IP (deliverables from WP2, WP6, WP7, and partly WP3). Those deliverables will partly be publicly available and included in our GALS library. From this, we expect increased popularity of the suggested methods and architectures. One part of the generated deliverables will be also kept confidential (SystemC model of NoCs, GALS network interfaces for NoC IP) and expected to be exploited directly by licensing and using patent rights on methods. In principle, project partners can jointly commercially utilize developed IPs over some partner company or by creating start-up(s). Additionally, open-source IPs can be exploited indirectly by providing technical support and offering additional chargeable features. We expect that this combined strategy will be very effective on establishing a good business model and enabling commercial exploitation of the project results.

In the context of the project, we planned to build a base of design tutorials, synthesis and layout scripts needed for a successful GALS design process. Those deliverables will be part of our GALS library. However, our adopted know-how will be the outstanding basis for the third way of exploitation of the project results in the direction of service. It is expected that after the end of the project the accumulated expertise among the project partners will be on a level that enables further commercial exploitation by providing design services for external customers. For example, such services may include support in the design process for GALS and GALS NoC chips from an algorithmic level, over synthesis, up to layout and testing of fabricated chips. The proposed exploitation plan may be realized over a partner company or by creating a start-up.

Fourth direction of exploitation will work directly over the industrial partners in the project. In the project consortium we have two industrial partners: Silistix (SME) and Infineon Technologies (Industry). All of their deliverables will be directly used in their products and in design process. For example, Silistix will work on deliverables (D25 Ability to have clocked/async boundaries within the switching fabric of the CHAIN network and D28 Pausible clock DLL with self-calibration, jitter, frequency and drift control) that will be directly used in their products. Also Infineon will use a deliverable (D4 Extension of standard cell library for 130 nm CMOS (IHP) and 45 nm CMOS (INFINEON) processes) in their design process. In addition, our industrial project partners are very much interested in the success of the GALAXY project. Therefore, the good impact of the project results may result in additional possibilities for commercial exploitation over our industry partners. In particular, the foreground from category one, two and three generated from academia can be also exploited by the project industry partners under conditions defined in Consortium Agreement. Generally, our industry project partners will have priority in exploiting the foreground of the project generated by academia.

We strongly believe the proposed exploitation plan facilitates successful commercial utilization of the results. The exploitation of the project results from the project partners is further described in section B.3.2.5. As stated before, some project results will be publicly available over our project web

site and in the dissemination process. Therefore, we can additionally expect that the results of the project will be widely used in commercial applications from different companies outside the project consortium.

B.3.2.5 Exploitation of results by project partners

B.3.2.5.1 IHP

IHP strategy is for a long time focused on wireless applications. We have many research activities in direction of communication system development in 5 GHz and 60 GHz frequency range. While designing such complex mixed signal systems we were facing many problems in the area of system integration and chip interconnects. Development of such systems requires support for reliable and fast system integration. Additional features that we require are EMI reduction in order to support System on Chip (SoC) implementation and power reduction for our handheld and mobile systems. Therefore, IHP has very big interest in GALS in order to cope with such challenges. In our future design flow it is planned to use GALS as a design integration vehicle and to have maximal use of other GALS features.

This project will give us the opportunity to cope with the state-of-the-art and future design issues related to 45 nm CMOS process that is currently unavailable to academic research institutions. The additional expertise that we will be to establish in this way will be very usable to further improve our results.

IHP is currently very good positioned in the community regarding GALS research. We already have published large number of highly referred publications in this field. Also we have fabricated and successfully tested, in 2004, one of the most complex GALS demonstrators up to now. This previous work was followed with the two published patents. Consequently, now with this project we expect to establish ourselves as a leading institution in the area of GALS research. It is planned that this project will be the basis for at least one PhD some Master theses.

B.3.2.5.2 University of Manchester

The results generated by this project will be exploited in two ways: academically and commercially. The university is a research led institution and the results of its research are included in both its undergraduate and taught Master's programmes. We are currently revising our course portfolio and will be offering, jointly with the School of Electrical and Electronic Engineering, a degree in "Computer Systems Engineering" which will heavily feature embedded systems engineering. We also offer taught M.S.c modules in "Low Power Systems Engineering" and "System Level Design". Both of these modules incorporate materials, relevant to industry, directly arising from previous research projects.

The University has a well established exploitation unit. Spin-out companies founded from the School of Computer Science as a result of previous research activities include:

- Transitive Corporation: a provider of solutions that allow the transportability of software applications across multiple OS and processor pairs. Transitive's technology allows Apple to run legacy Power PC applications on its newer Intel platforms.
- Silistix: utilizes breakthrough synthesis technology to generate self-timed on-chip interconnect networks
- imorphics: shape modelling technology of digital images for clinical trials.
- Genemation: facial image generation software
- Cognisience: hardware support for neural networks
- Kestra: optical inspection technology, recently sold to CyberOptics Corporation for approx. £7 million.
- Cerebra: semantic metadata management technology across the web.

B.3.2.5.3 Ecole Polytechnique Fédérale de Lausanne

Members of the Integrated Systems Laboratory (LSI) of EPFL have a long history of working on Network-on-a-Chip solutions and have made significant contributions to this field. There are many parallels between the NoC approach and the GALS approach to system design. For example both

methodologies favour a clear separation between functionality and communication. The LSI is interested in investigating how the NoC approach can be supported by the GALS methodology and how these solutions compare to more traditional synchronous approaches in terms of power, throughput and circuit area.

The Microelectronic Systems Laboratory (LSM) has a slightly different focus. LSM specializes in the design of high-performance digital and mixed-signal VLSI circuits. As such, methods to improve performance, reduce power and/or energy consumption as well as architectures for reliable operation have been active areas of research. The LSM is especially interested in the low-power aspects of GALS design.

B.3.2.5.4 Università di Bologna

University of Bologna is a leading institution in NoC research worldwide, and aims at migrating its mature fully synchronous xpipes NoC architecture to the GALS domain, dealing with the exploration and optimization tasks posed by this task. The current xpipes prototype is a milestone in the development of NoC architectures, but the increasing concerns on effective clock distribution in nanoscale MPSoCs are urging a new milestone. With this project, University of Bologna aims at strengthening its position in the research community by coming up with an optimized GALS-based NoC platform overcoming clocking, but also relieving power and reliability concerns. The main objective is for xpipes to become a solid research and exploration platform, i.e., a reference infrastructure around which a number of European as well as international research cooperations can be established to bring NoC architectures to industrial maturity. In this context, GALS technology is a fundamental driver for this roadmap, which needs to be thoroughly explored and consolidated. Moreover, since NoCs target nanoscale technologies, architectural solutions cannot be devised independently of physical considerations any more. As a consequence, devising architectural-level techniques and testing methodologies accounting for process variability is key in establishing xpipes as leading research platform for nanoscale NoCs.

Finally, University of Bologna will exploit the projects results to raise the level of education by giving Master and PhD students the opportunity of working on cutting-edge research in a European collaborative effort. In addition the research results will be used in teaching of undergraduate and graduate students, thus promoting awareness of leading edge technology with those students.

B.3.2.5.5 Silistix

Silistix already has a toolflow for commercial deployment of GALS based NoC, but the primary exploitation opportunity they bring to this project stems from this fact in that there are many areas where their solution will benefit by extension with knowledge gained and techniques developed through this consortium.

Much of the work in this project can be directly used with the Silistix NoC technology, and the exploration of the impact of GALS techniques on a clocked NoC framework will further enhance Silistix understanding of what their competitors could feasibly implemented in the medium term.

Furthermore, the positive reinforcement of the maturity and robustness of GALS techniques, demonstrated through the tools developed, and testchips fabricated in this project will help lower the barriers to market adoption of Silistix tools.

B.3.2.5.6 Infineon Technologies

Infineon Technologies is supporting GALS activities already for years. In particular, they were supporting previously GALS research, driven from ETHZ Switzerland. Infineon strongly believes in the future of GALS methodology, especially in the context of nanoscale technologies. Up to now problems with reliable GALS design flows and the competitiveness of conservative synchronous solutions prevented the major breakthrough of GALS techniques. However, Infineon expects that solutions offered within the GALAXY project will dramatically increase the acceptance of GALS methodology especially for complex deep sub-micron system.

In this context Infineon wants to utilize results of the project, evaluate effectiveness of GALS techniques and possibly apply GALS methodology in future products. Additionally, Infineon will in the framework of the project integrate extension of the standard cell libraries with asynchronous cells (C-element, mutex, etc.) and GALS hard macro interfaces into a standard design kit for high-end 45 nm CMOS process. This will give a strong support for the further exploitations of GALS and asynchronous interfaces in future commercial designs originated from Infineon.

B.3.2.6 Management of intellectual property

In a consortium agreement the partners will define specifically the rules and procedures for non-disclosure of the restricted know-how and dissemination of the other project results. The consortium agreement will be based on models provided from ICT and DESCA. Commercial utilization of the project results or the parts of the project results will be defined in a consortium contract.

One of the basic premises of the project is that many of the project results (IP cores, CAD tools, etc.) will be publicly available on the project web-site and as open cores. However, every partner in the consortium will be able to select the level of availability of its own project results (as provided in table 1.3.3.2 that integrates the list of deliverables).

In principle we can define two approaches driven from different partners. Industry partners STX and INFINEON will mainly keep their deliverables confidential in order to secure commercial exploitation of the project results. The only exception from this will be the specification of characterization for INFINEON 45 nm process, which will be public. IHP holds two patent applications on GALS interconnects, one dealing with own developed request-driven GALS technique and the other with methods for EMI reduction with GALS interconnect. The circuits and methods covered by those two patents may be utilized in the framework of this project and made available for non-commercial application. Nevertheless, a commercial exploitation of those proprietary patents is subject to licensing. On the other hand, software tools developed from UNIMAN will be under GPL (General Public License); SystemC synthesizable models of GALS-compatible Network-on-Chip from UNIBO will be open source and provided in our IP library. An abbreviated guide to the status of results generated in the project is given below:

Publicly Available

Output from Partner	Partner
GALS interface definitions and standards	IHP, STX, EPFL, INFINEON
GALS interface library	UNIMAN
Co-simulation Tools	UNIMAN
IP packaging format	UNIMAN
Specification of characterization for the additional asynchronous standard cells for INFINEON 45 nm CMOS process	INFINEON
SystemC synthesisable models of GALS compatible building blocks (switches, links, network interfaces) corresponding to a GALS NOC library.	UNIBO
Reports detailing proven architectural techniques to increase communication reliability and process-variation tolerance of NoCs	UNIBO
Tools for automatic specification and instantiation of GLAS NoC building blocks	UNIBO
Design and Test Tutorial	EPFL, IHP, STX, INFINEON, UNIMAN
Various reports about evaluation of GALS methods from different partners	IHP, EPFL

Restricted Availability

Output from Partner	Partner
Pausible clock-generator with calibration control and test-chip analysis circuits are confidential	STX
Clocked CHAIN NoC transport layer components are confidential	STX
Commercial utilisation of all methods, specifications and source code regarding GALS interfaces are subject to licensing terms	IHP

Extension of the 130nm standard CMOS cell library subject to standard Europractice terms	IHP
Communication IP is confidential	IHP
SystemC-based virtual platform for MPSoC exploration. This includes modelling and simulation environment, statistics collection system, memory hierarchy, a subset of models of computation, interconnect and storage core will be confidential	UNIBO
45nm libraries: confidential	INFINEON

The intellectual property that is brought to the project by the partners (communication IPs from IHP for example system design, technology information and parameters from INFINEON) will not be disclosed outside the project consortium. The subject of the dissemination will be only the knowledge, IPs and innovations sourced from the GALAXY project activities. The exceptions to this rule may relate to the tools needed for GALS design (for example Balsa) and GALS interface IPs that are already freely available.

The cost of the possible patent application will be covered from partners. Project coordinator will be informed about the possible patent applications and about their status. Consequently, the project coordinator will regularly inform EC about the status of patent applications generated from the project results. The patent status summary will be also a part of dissemination work package report.

B.3.2.7 Contribution to the standards

The contribution to the standards will be focused in two directions. First goal is to influence standardization of the GALS NoC interfaces. A typical NoC system partitions the system into several independent resources that communicate over the network. At the hardware level, data communication is accomplished by dedicated network switches. The resources are connected to these switches by the way of network interfaces. Even if the underlying network architecture remains the same, such a system has many parameters (type of the network interface, width of data communication lines, buffering strategies, etc.) that can be adjusted. A GALS implementation offers even more choices, especially in determining the clock domains between different resources. The goal of this project is to define new standards for GALS based NoC interfaces. Wherever possible, these standards will be made compatible with existing standards such as OCP. The standardization effort aims at design reuse of network building blocks across different platforms, at the optimization of die area by configuring into the interfaces only those features that are needed by the NoC at hand, and at simplifying system verification and testing by providing a firm boundary around each network building block that can be observed, controlled and validated.

Our newly developed GALS design flow will be based on an open format for mixed synchronous-asynchronous IPs in order to consolidate asynchronous IPs dissemination and re-use. This format will most probably complete the existing IP-XACT synchronous IP packaging format proposed by the SPIRIT consortium, which is currently lacking support for asynchronous-specific structures. After specification of our new format, the preferred route will be to propose our ideas to the IP-XACT standard. In case of incompatibility, our specifications could still be used to create a new standard for describing asynchronous IPs, as none has been proposed so far by the international community.

It is planned that this IP format will be able to describe hardware/software entities at multiple levels of abstraction in multiple languages (SystemC, C, Verilog, VHDL, Balsa, gate-level netlist etc.), with both synchronous and asynchronous interfaces. The IP format will contain enough information to transparently convert signals between varying levels of abstraction enabling: a transparent co-simulation of IPs at different levels of abstraction, the visualisation of signals at levels of abstraction independently of the simulated level of abstraction, and exploitation of transaction level structures during hardware-software co-design and visualisation.

ABBREVIATIONS

AHB	- Advanced High-performance Bus
AMBA	- Advanced Microcontroller Bus Architecture
ASIC	- Application Specific Integrated Circuit
ATE	- Automatic test equipment
AXI	- Advanced eXtensible Interface
BiCMOS	- Integration of bipolar junction transistors and CMOS technology into a single device
BIST	- Built-in self-test
CAD	- Computer Aided Design
CC	- Coordinating Committee
CHAIN	- CHip-Area INterconnect, product of STX
CLB	- Configurable Logic Block
CMOS	- Complementary metal–oxide–semiconductor
DFS	- Dynamic frequency scaling
DfT	- Design for testability
DMA	- Direct Memory Access
DPA	- Differential Power Analysis
DVS	- Dynamic voltage scaling
EDA	- Electronic design automation
EMC	- Electromagnetic compatibility
EMI	- Electro-Magnetic Interference
FF	- Flip-flop
FFT	- Fast Fourier Transform
FIFO	- First-in first-out
FPGA	- Field programmable gate array
GALS	- Globally Asynchronous, Locally Synchronous
GPL	- General Public License
GUI	- Graphical User Interface
HDL	- Hardware Description Language
HLA	- High Level Architecture
hw-sw	- Hardware-software
IC	- Integrated Circuit
IDE	- Integrated Development Environment
IFFT	- Inverse Fast Fourier Transform
I/O	- Input/output
IP	- Intellectual Property
LS	- Locally synchronous
MC-CDMA	- Multi-carrier code division multiple access

MPSoC	- Multiprocessor Systems on Chip
Mutex	- Mutual exclusion element
NDA	- Non-Disclosure Agreement
NIC	- Network interfaces
NoC	- Networks on Chip
OCP	- Open Core Protocol
OFDM	- Orthogonal Frequency Division Multiplex
OSCI	- Online Services Computer Interface
PVT	- Process, Voltage, Temperature
R&D	- Research & development
RTL	- Register transfer level
SME	- Small and Medium Enterprise
SoC	- System on Chip
SPIRIT Consortium	- A global organization focused on establishing multi-faceted IP/tool integration standards that drive sustainable growth in electronic design
TC	- Technical Committee
VC	- Virtual channel
VHDL	- VHSIC Hardware Description Language
VLSI	- Very-large-scale integration
WLAN	- Wireless LAN
WP	- Work package