Newcastle University

An Adiabatic Power-Supply Controller for Asynchronous Logic Circuits

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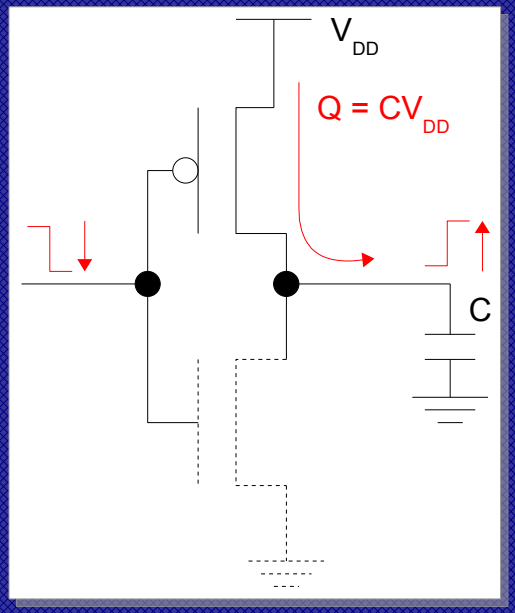
Summary

- Adiabatic logic background.
- Asynchronous adiabatic implementation.
- Simulations / Evaluation.
- Conclusions.

Standard CMOS Energetics

1. Charging



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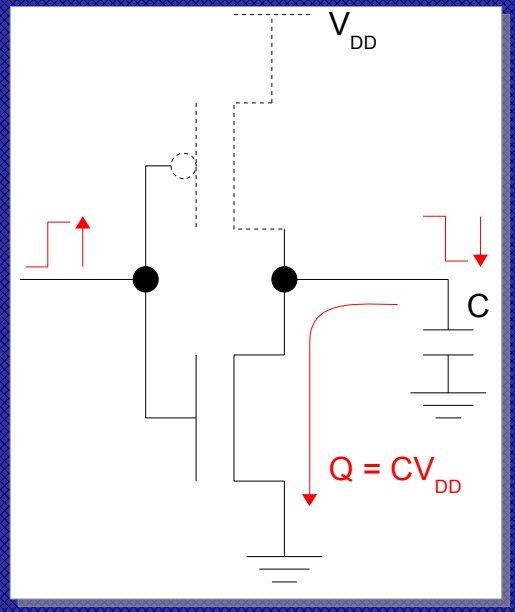
2. Discharging



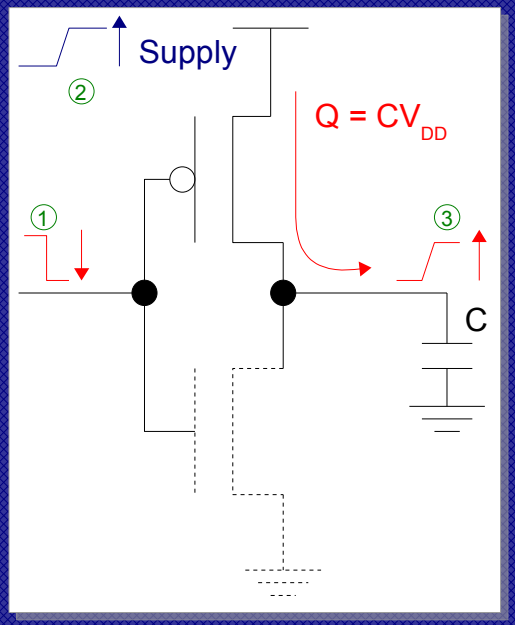
$$\Rightarrow E_d = QV_{DD} = CV_{DD}^2$$

The only ways to reduce energy consumption are:

1. Reduce supply voltage $\mathbf{V_{DD}}$.
2. Reduce load capacitance **C**.

Adiabatic Logic

1. Charging



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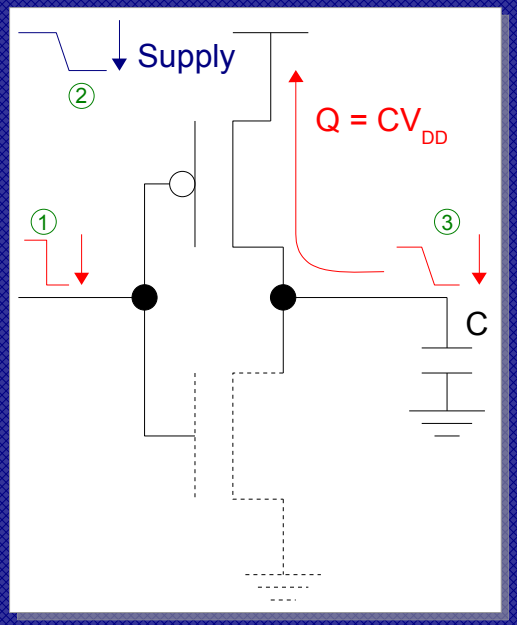
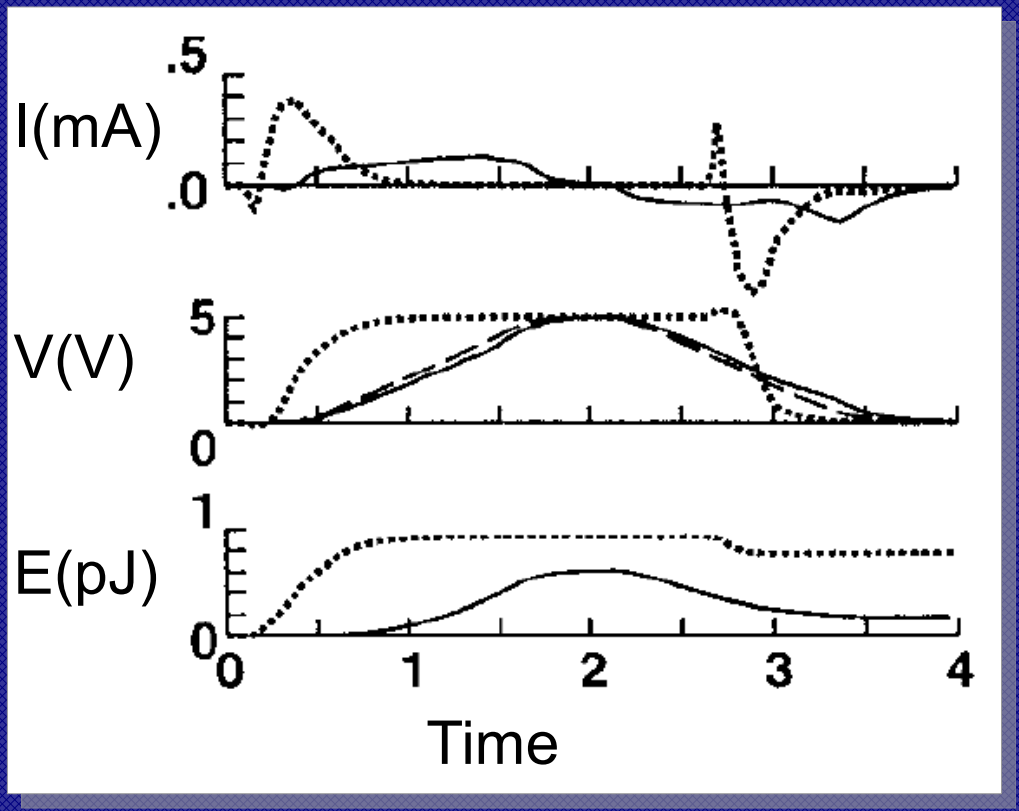
2. Discharging



=> **E_d = very small**

1. Charge Q is recovered back to the power supply.
2. Charging current becomes uniform and small over ramp time T → energy dissipation is minimized.

Adiabatic Logic

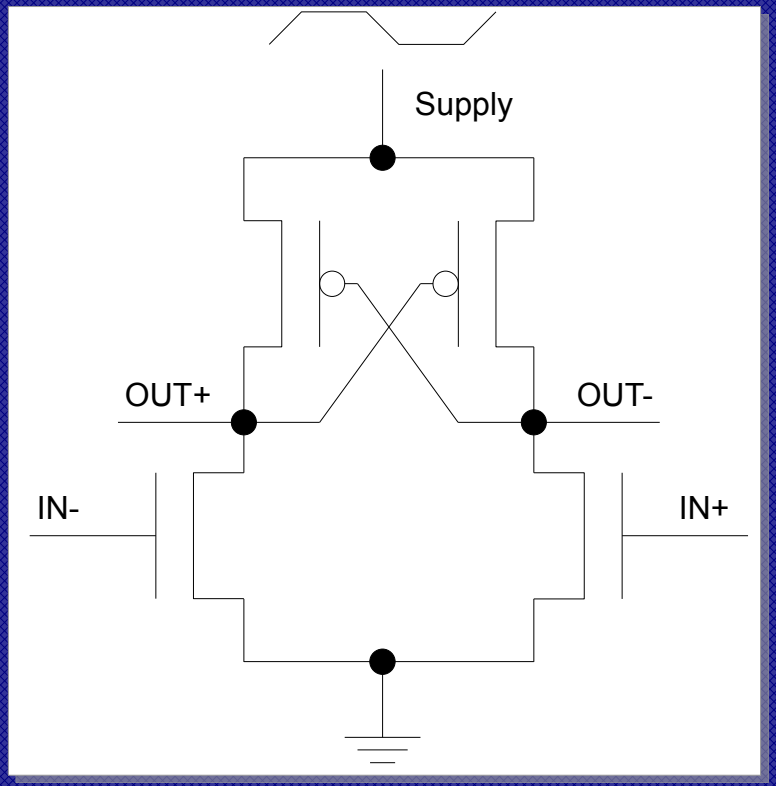


Voltage/Current/Energy measurements.

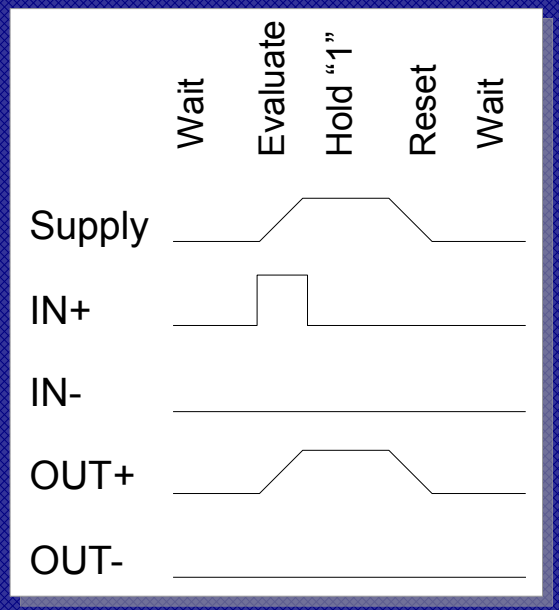
Dotted line: Conventional Inverter.
Solid line: Adiabatic Inverter.

J S Denker, “A Review of Adiabatic Computing”, 1994, IEEE Symposium on Low Power Electronics, pp.94-97.

Adiabatic Logic



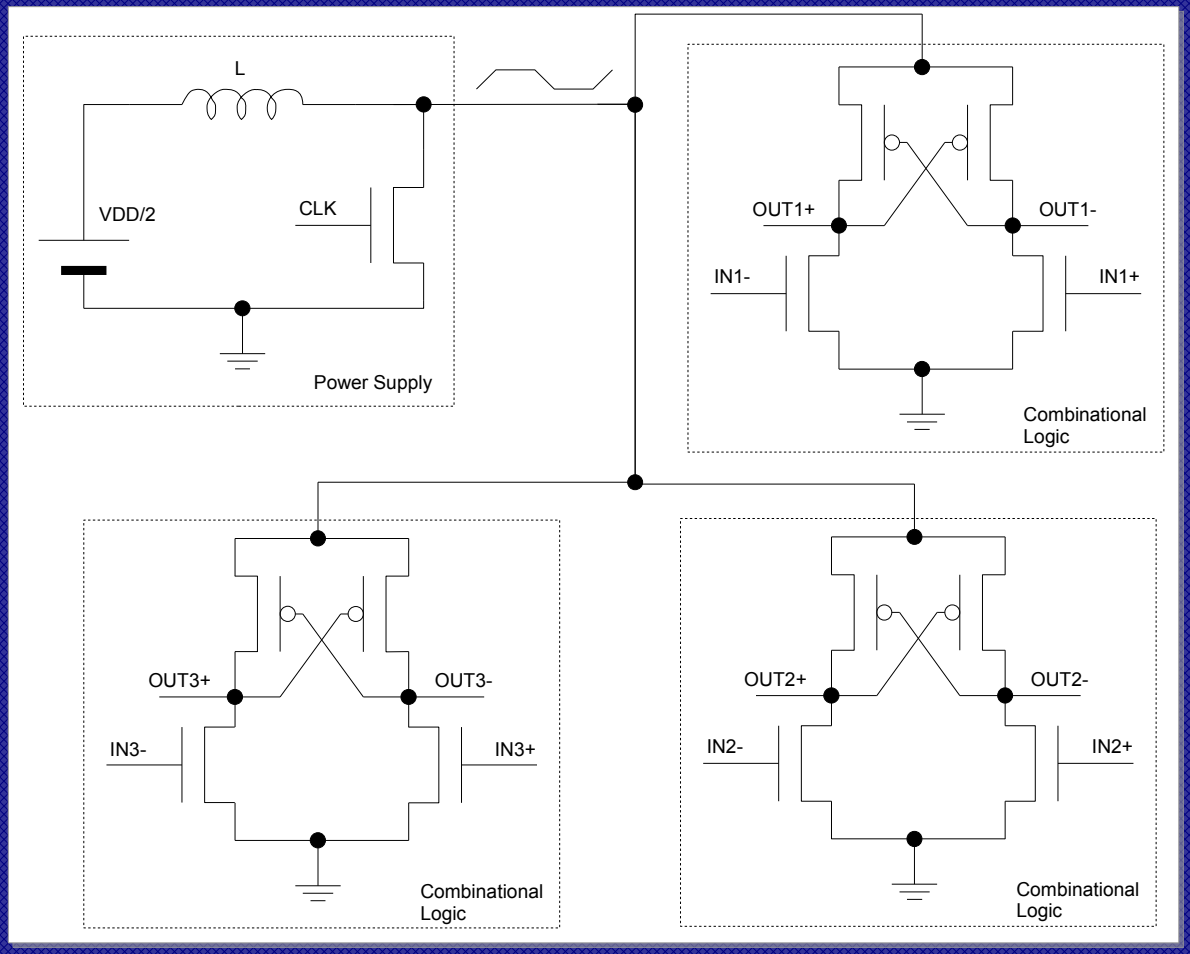
Basic 2N-2P Adiabatic Circuit.



2N-2P Timing Diagram.

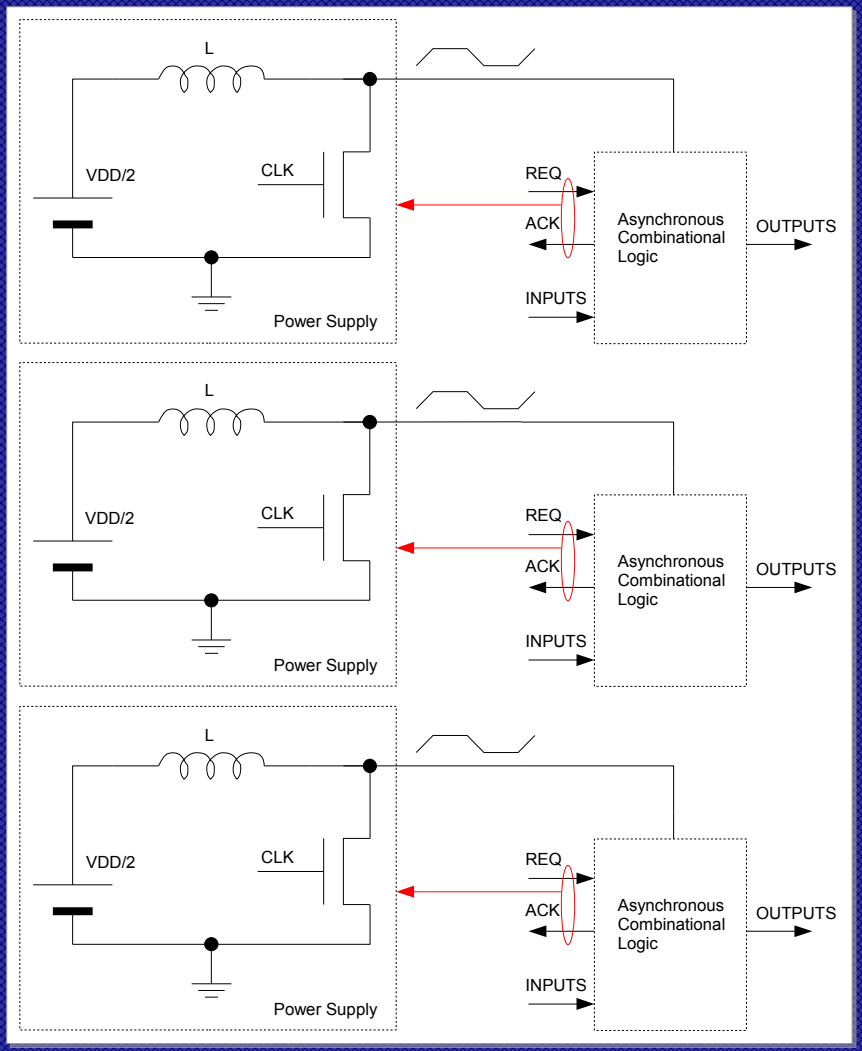
Kramer A., Denker J.S. et al, "2nd order adiabatic computation with 2N-2P and 2N-2N2P logic circuits", Proc.1995 Int. Symp. Low power design, pp. 191-196.

Synchronous Adiabatic Logic



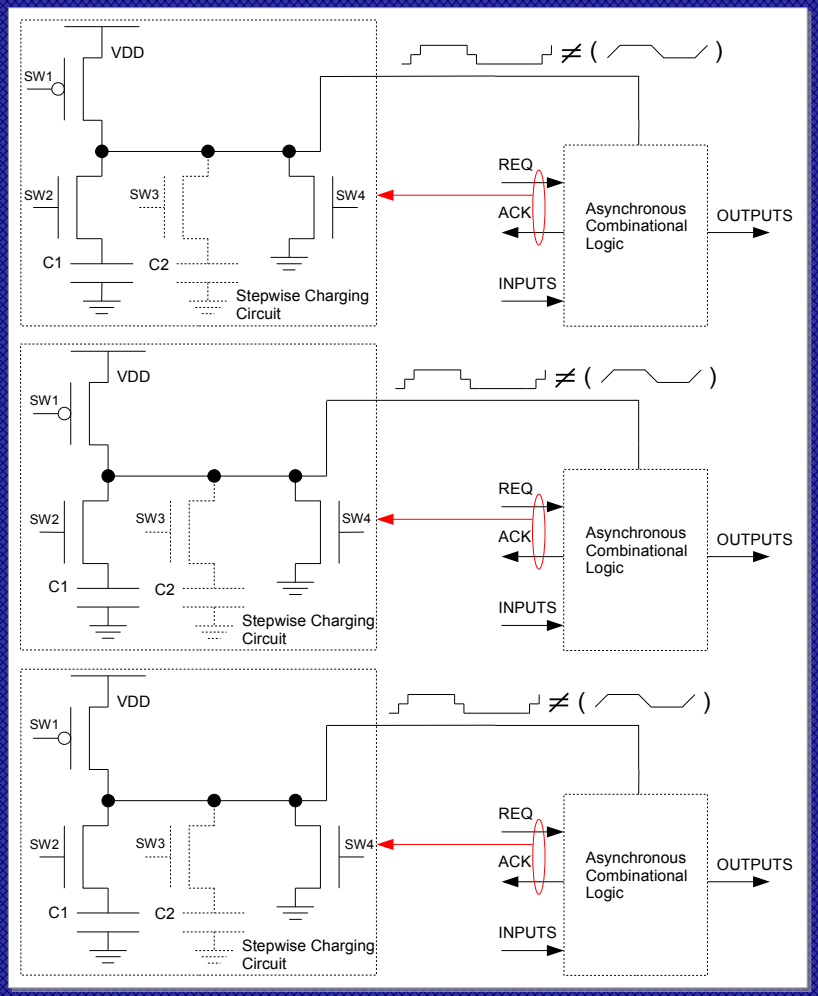
- One fixed frequency - one global power supply.
- Might require multiple phases of the power supply.

Asynchronous Adiabatic Logic



- Multiple frequencies – many power supplies.
- Space consuming design approach.

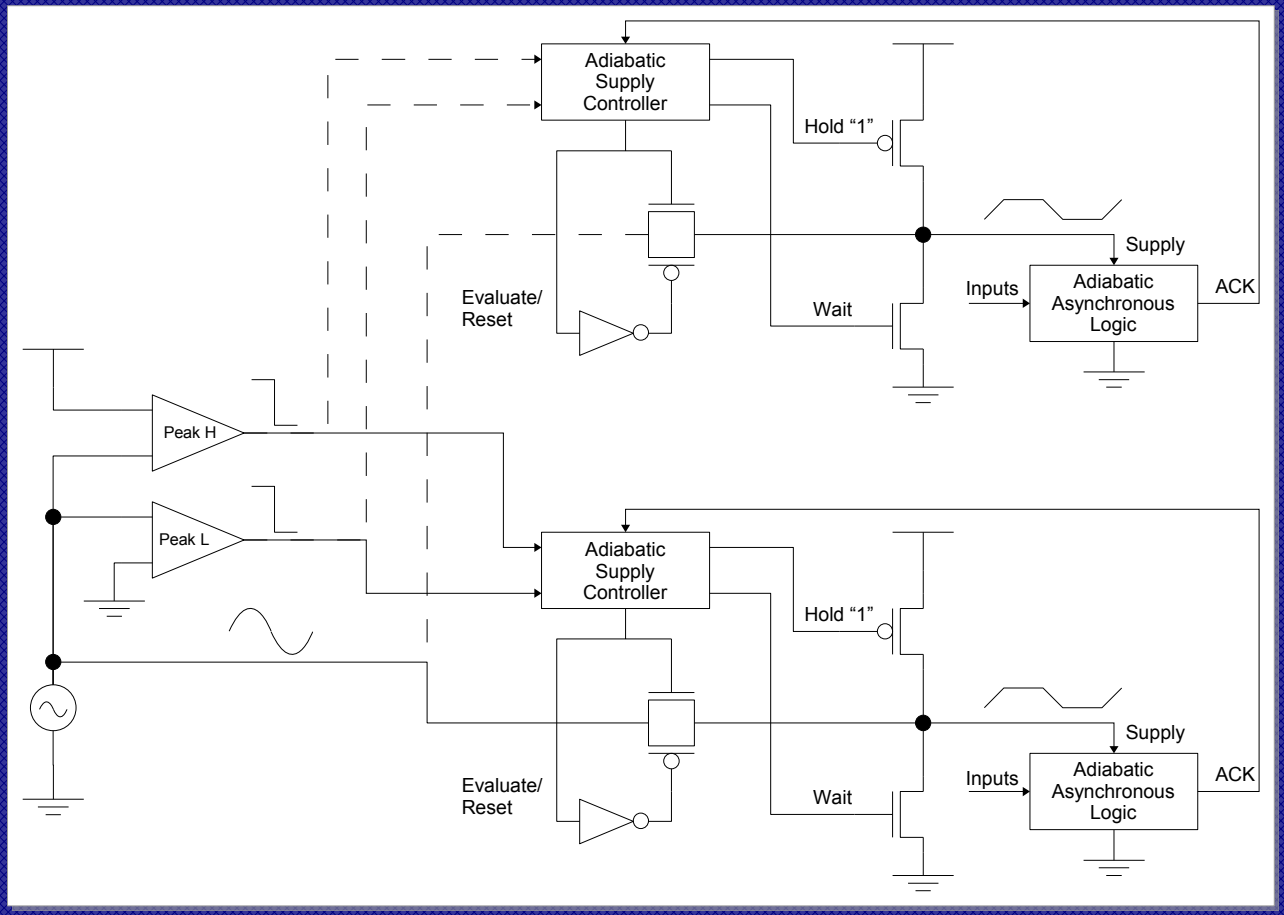
Asynchronous Adiabatic Logic



- Using a stepwise charging circuit, inductors are eliminated.
- Charging/discharging is no longer ramp-like.
- Capacitors still occupy large area on chip.

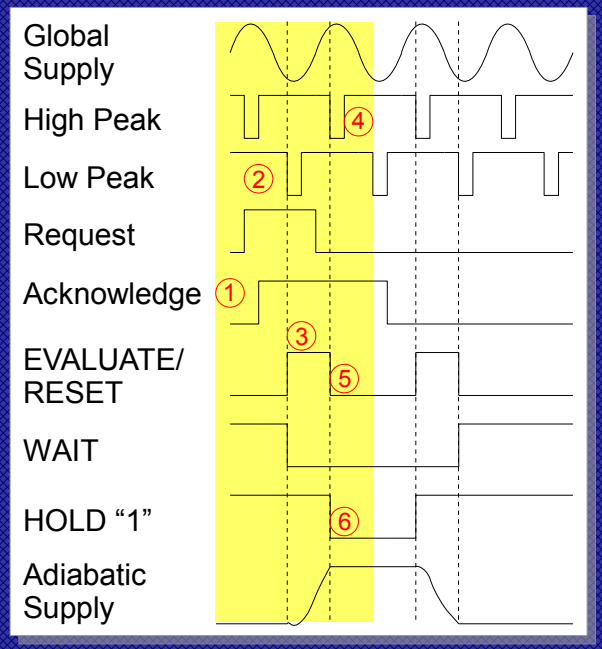
Willingham D.J. and Kale I., "Asynchronous, quasi-Adiabatic (Asynchrobatic) logic for low-power very wide data width applications", Circuits and Systems, 2004, Proceedings of the 2004 International Symposium on Volume 2, 23-26 May 2004 pp. II - 257-60 Vol.2.

Proposed Circuit



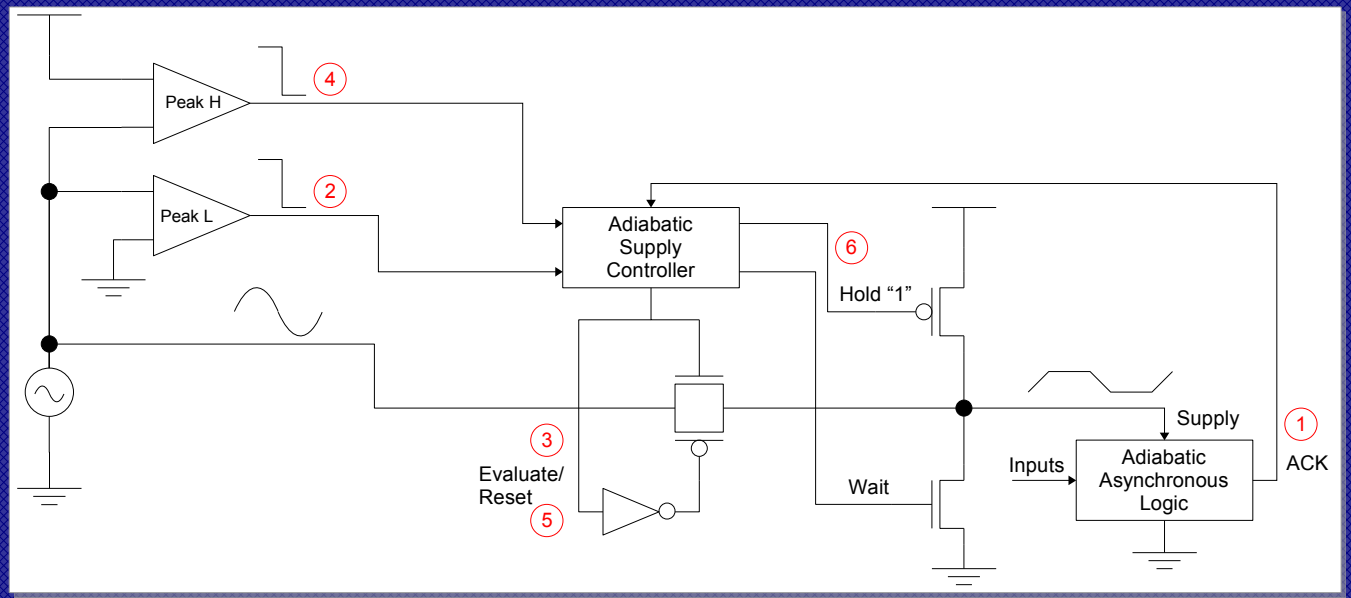
- Only one inductor-based supply.
- Ramp-like power supply generated by individual adiabatic supply controllers.

Adiabatic Supply Controller

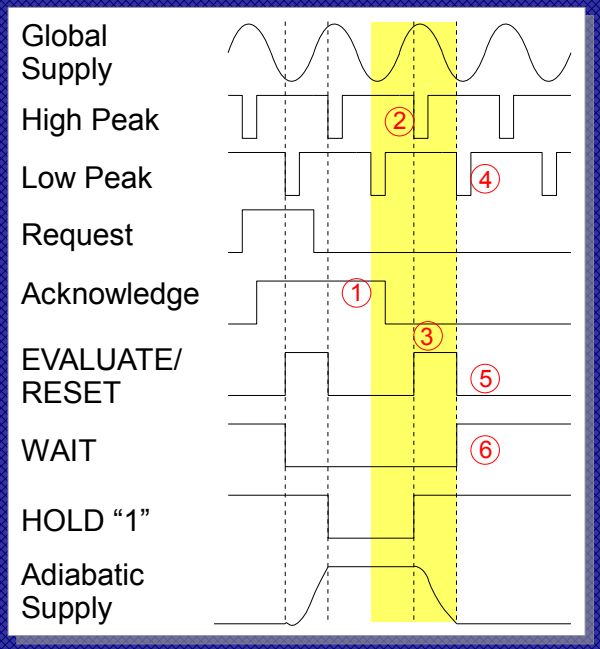


Adiabatic supply controller timing diagram.

Circuit topology.



Adiabatic Supply Controller



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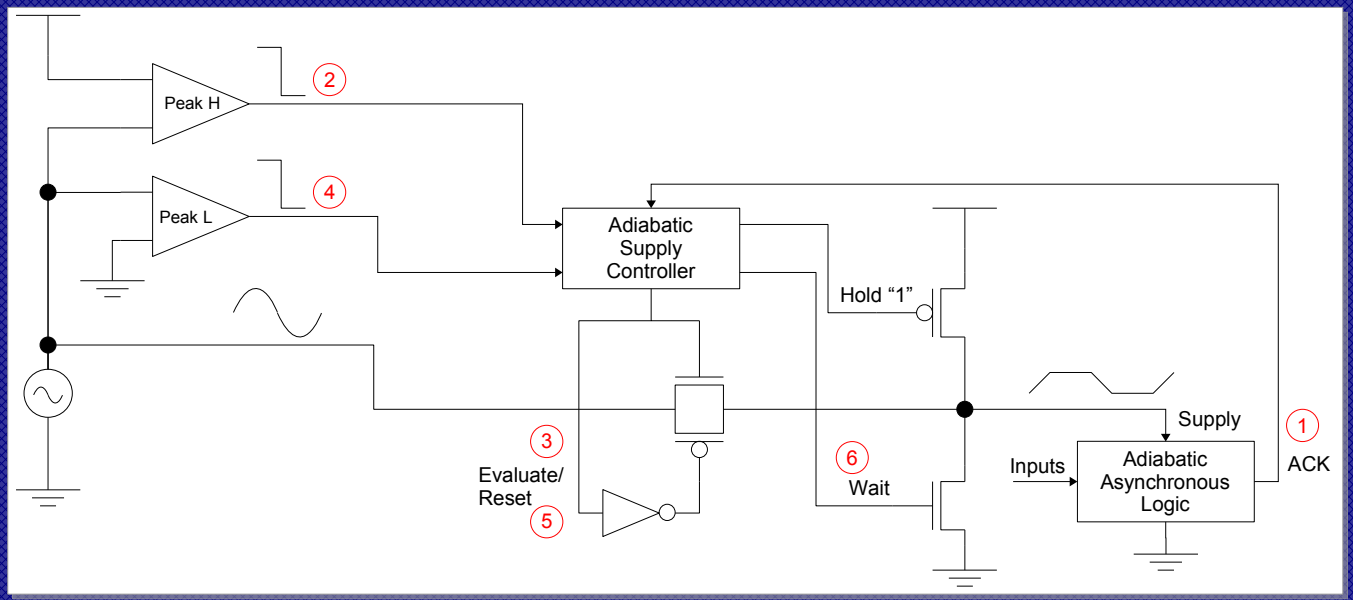
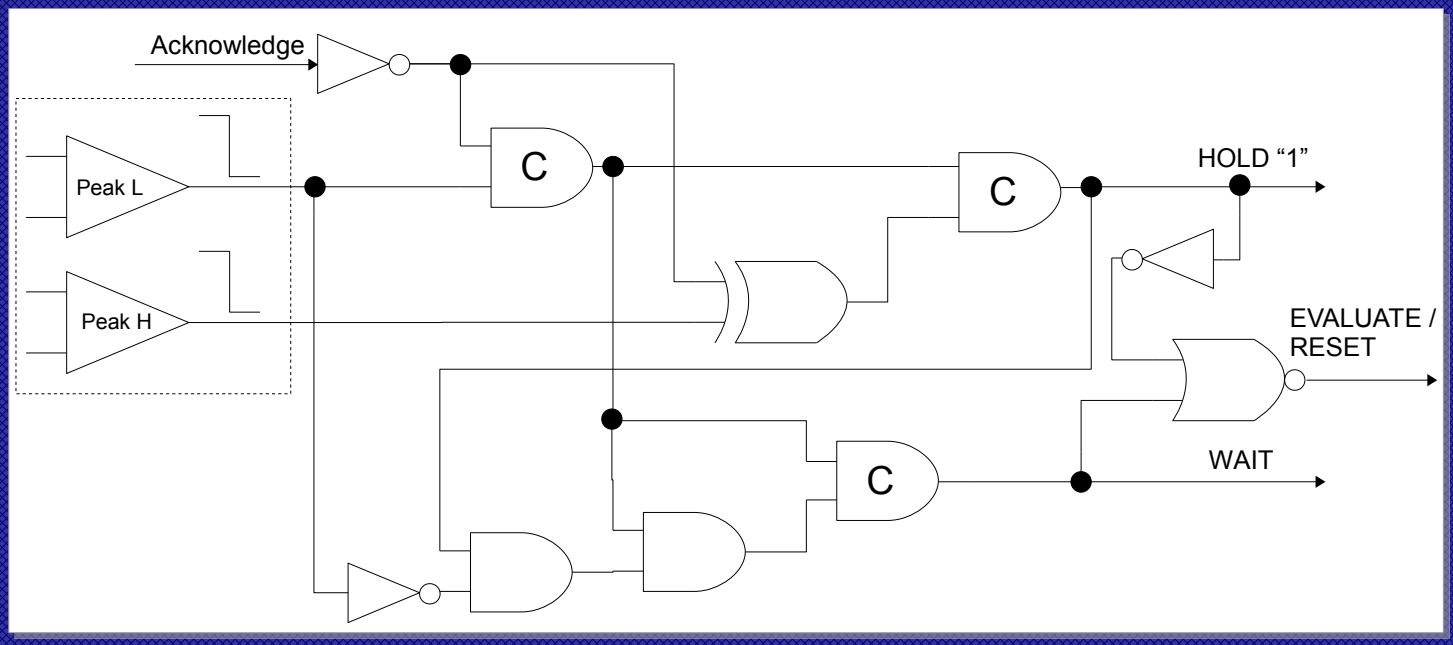
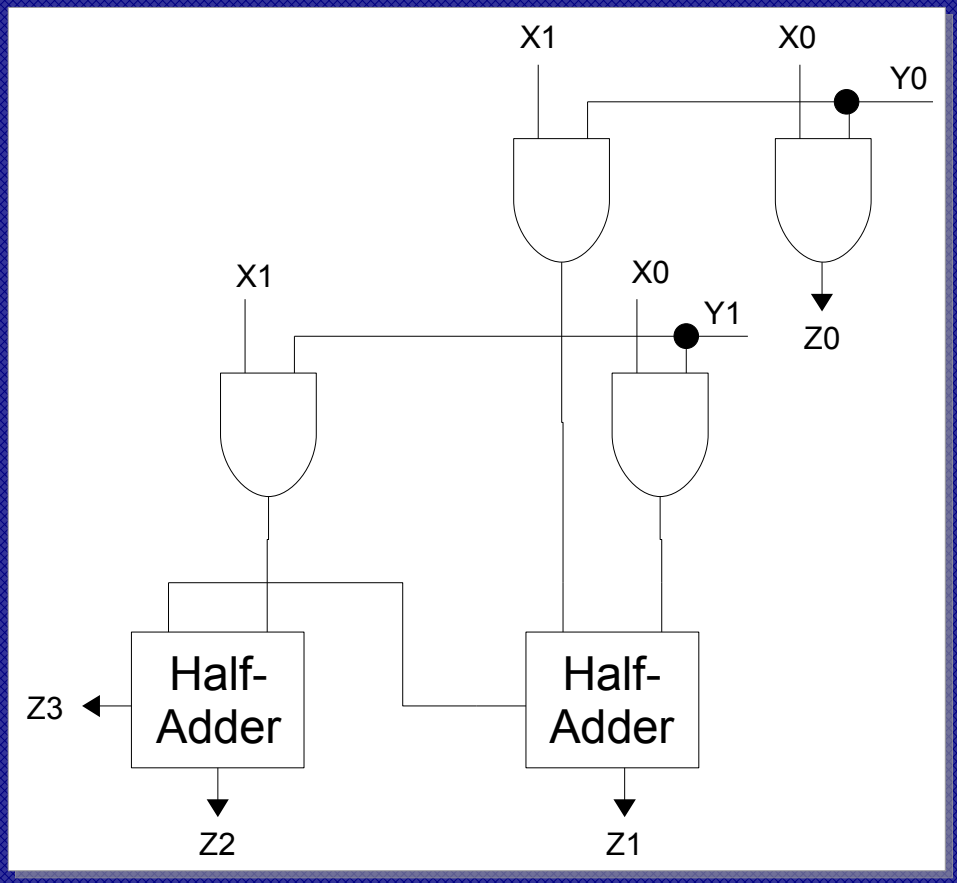


Adiabatic Supply Controller



Adiabatic supply controller logic.

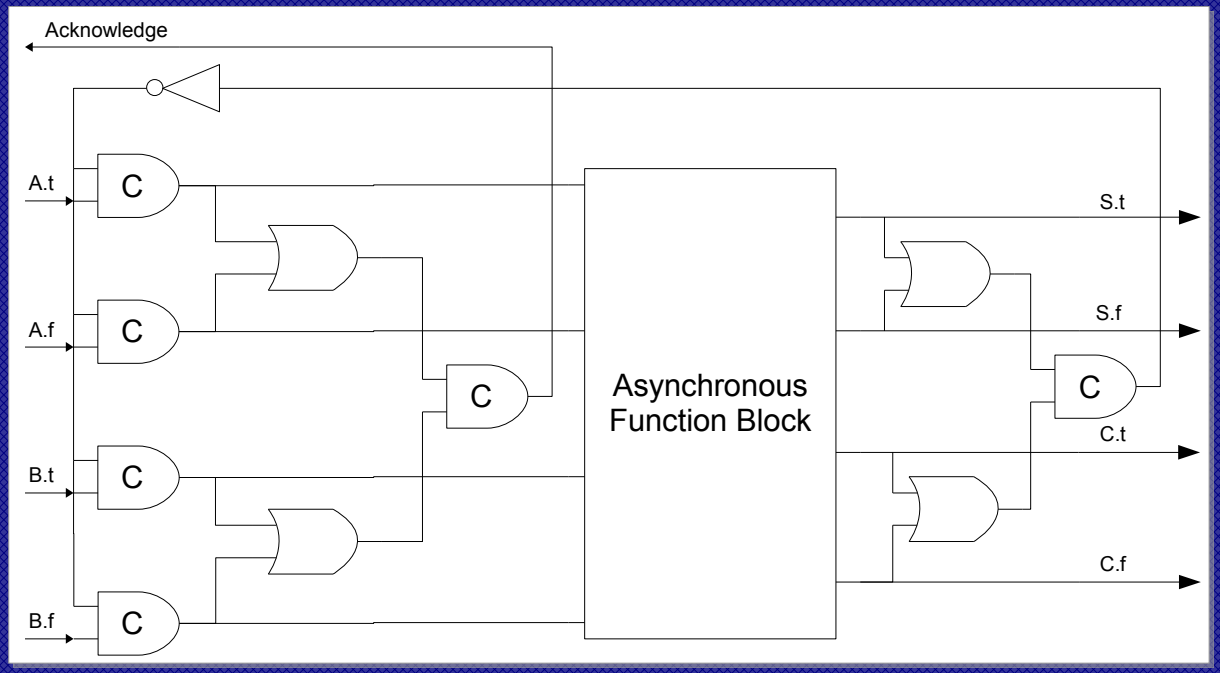
Evaluation



2-bit Multiplier.

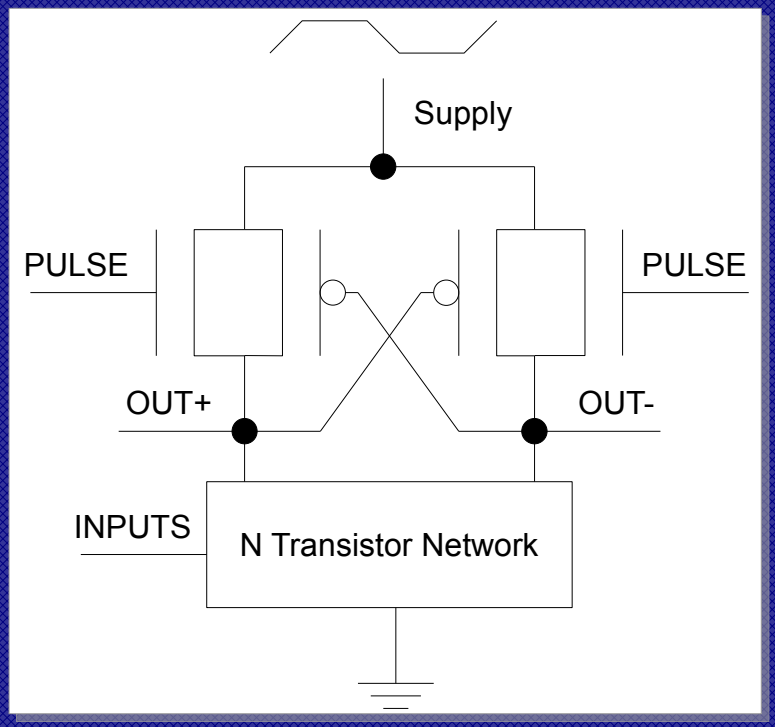
- Performance is evaluated by comparing 2,4,5 -bit asynchronous multipliers implemented in both conventional and adiabatic logic.

Evaluation



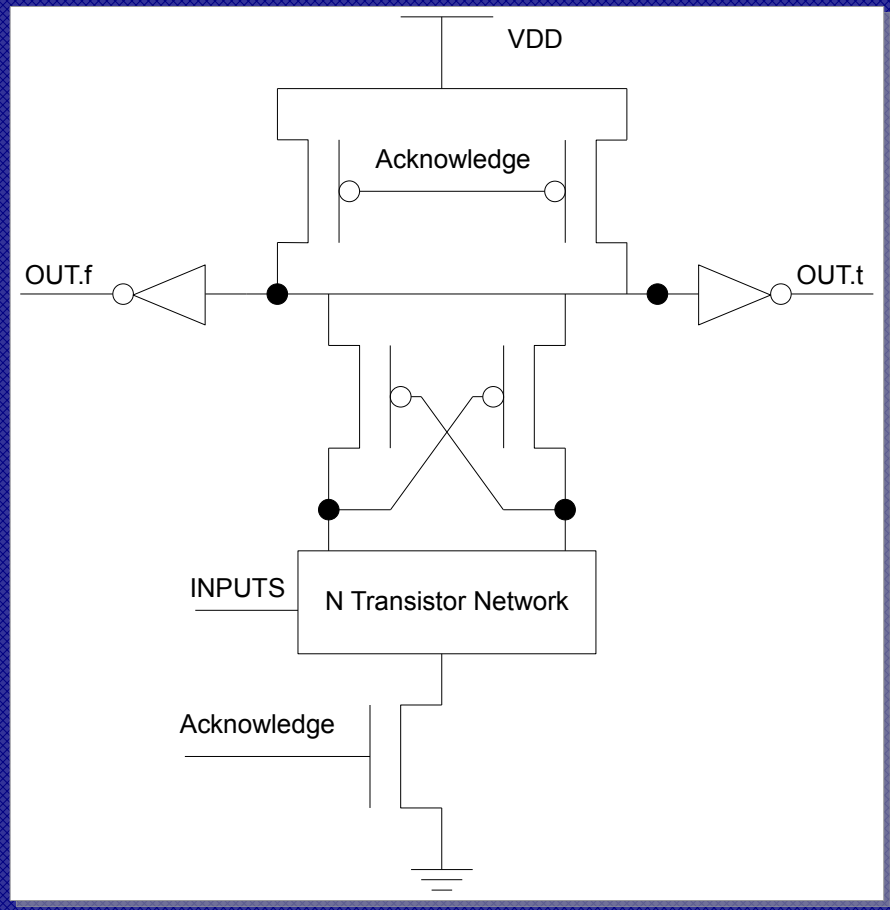
- The dual-rail pipeline handles asynchronous handshaking.
- Is the same for both conventional asynchronous and adiabatic asynchronous logic.

Evaluation



Modified 2N-2P Circuit.

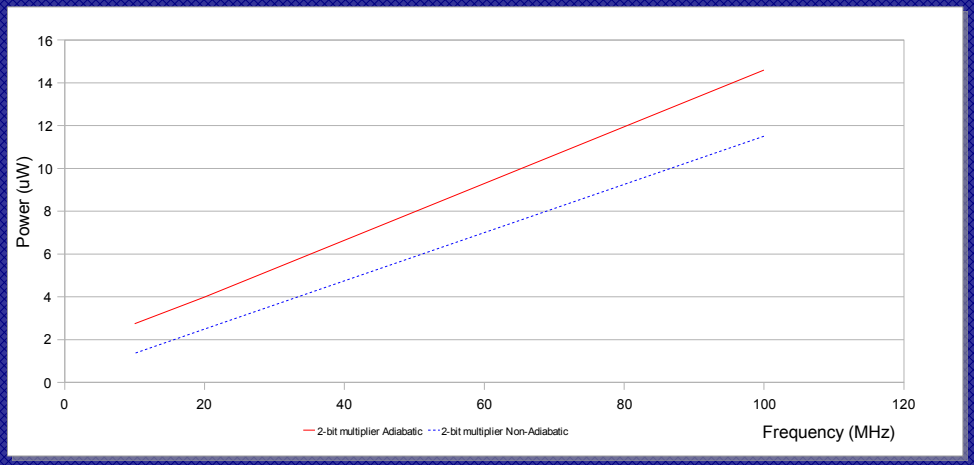
Yeh C.C., Lou J.H. and Kuo J.B., “1.5 V CMOS full-swing energy efficient logic (EEL) circuit suitablefor low-voltage and low-power VLSI applications”, Electronics Letters Volume 33, Issue 16, 31 Jul 1997 pp. 1375 - 1376.



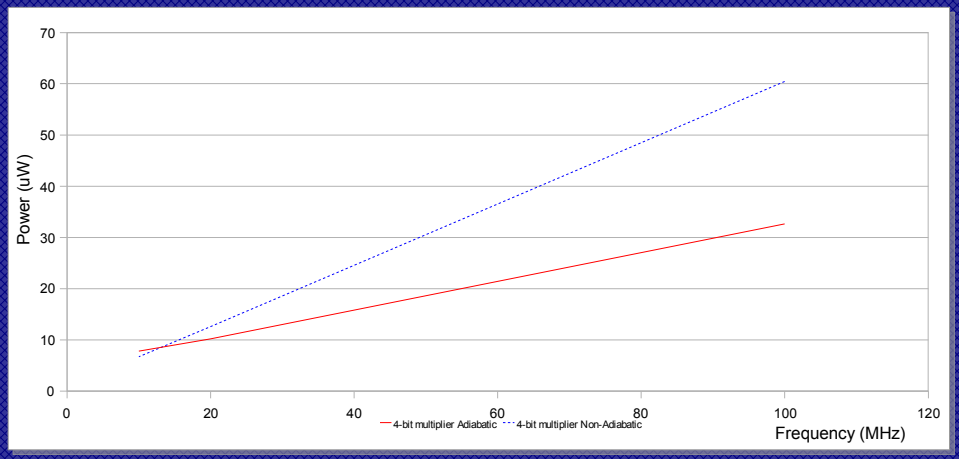
Precharged Differential CMOS Logic.

J Sparso and S Furber, ”Principles of asynchronous circuit design - A systems perspective”, Kluwer Academic Publishers, 2001.

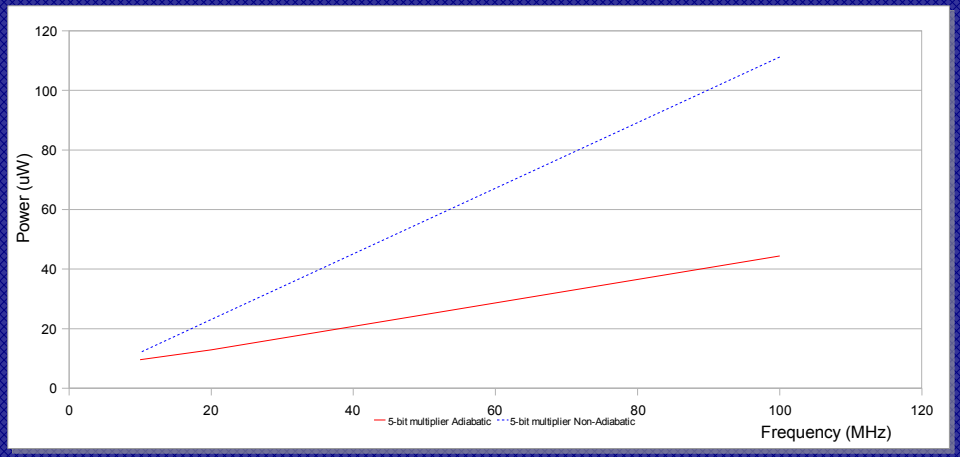
Simulation Results



2-bit Multiplier.

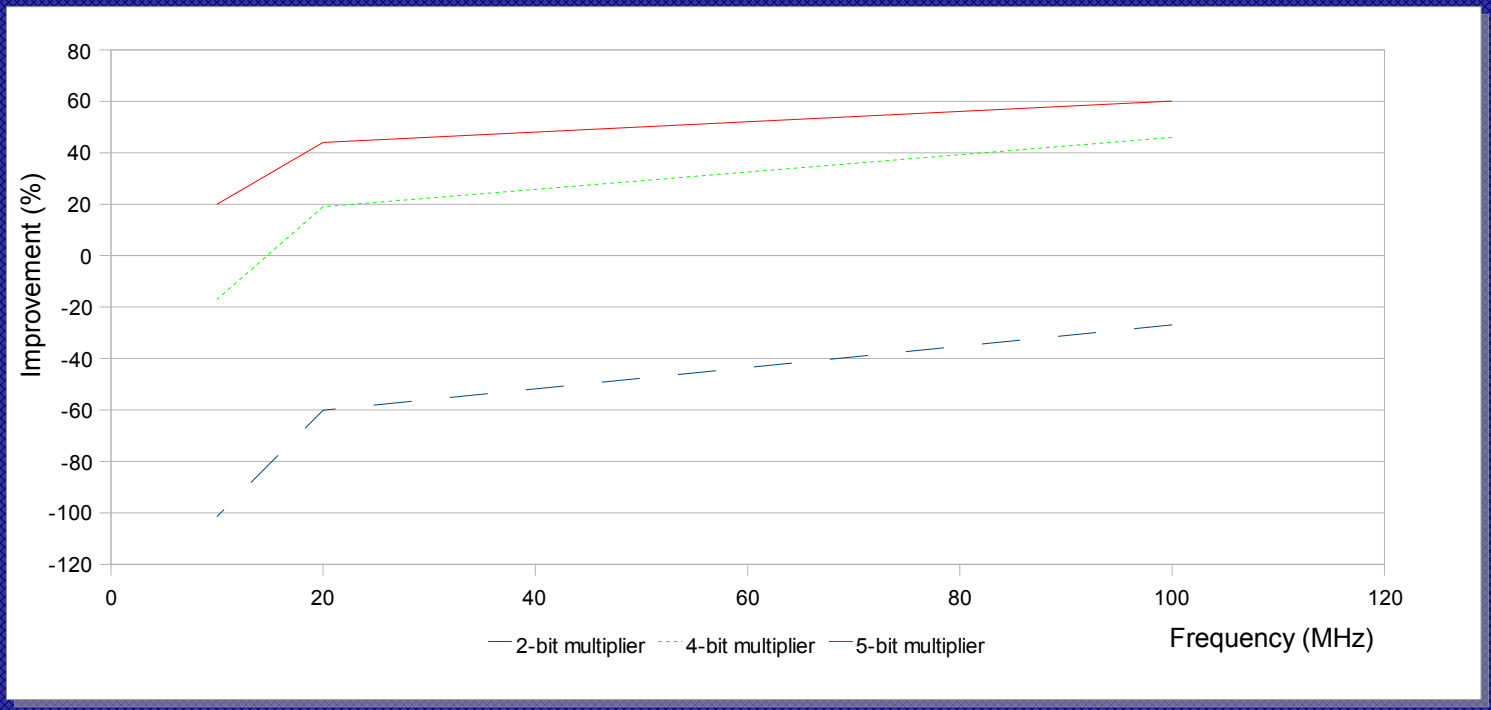


4-bit Multiplier.



5-bit Multiplier.

Simulation Results

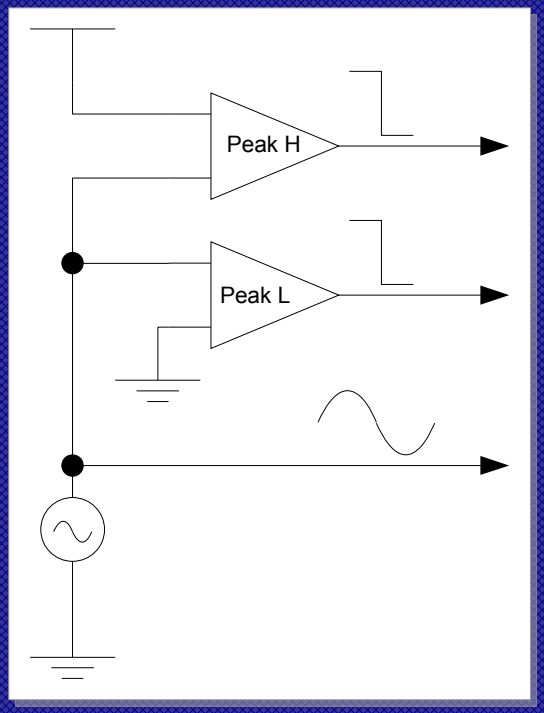


2,4,5-bit Adiabatic Multipliers power improvement over conventional circuit.

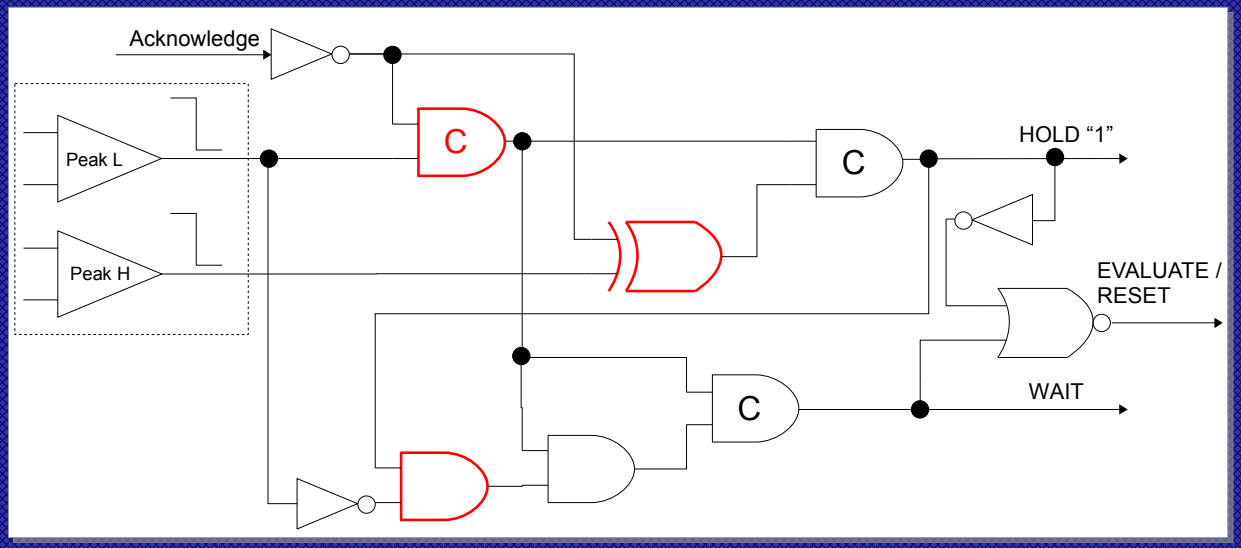
Circuit Weaknesses

- The operating frequency of the asynchronous logic blocks is limited by the sine-wave supply frequency (can introduce to the handshaking, an additional delay of 3 times the sine-wave period).
- The adiabatic supply controller induces a power consumption overhead. This makes the circuit inefficient for simple logic implementations.

Future



Peak detectors/sine-wave generator are ideal.



Metastability.

Conclusions

- A new approach for the design of asynchronous adiabatic logic was presented.
- Only one inductor-based power supply is required.
- The power improvement over conventional CMOS asynchronous is demonstrated to be more than 60% (can be further improved with more complex computational loads).
- This design approach could benefit applications that require low-to-medium speed performance and implement medium-to-high complexity logic functions → energy-harvester supplied computational logic.