EDSAC

Main Memory:

Batteries of 16 mercury-filled supersonic delay tubes. Each tube 63.8" long, with delay of 1.1 millisec, ∴ holding 16 numbers, i.e. 576 pulses.

Numbers:

Ten digit = 35 binary pulses (including Sign Digit)
or five " = 18 " " (" " ")

e.g. D_0 = blank
D_1–D_{34} = ten-digit number.
D_{35} = Sign digit (1 = +ve, 0 = -ve).

Minor Cycle:

Space occupied by one 10-digit no. =

Order:

As number, but ½ M/c in length — i.e. 18 pulses plus blank space.

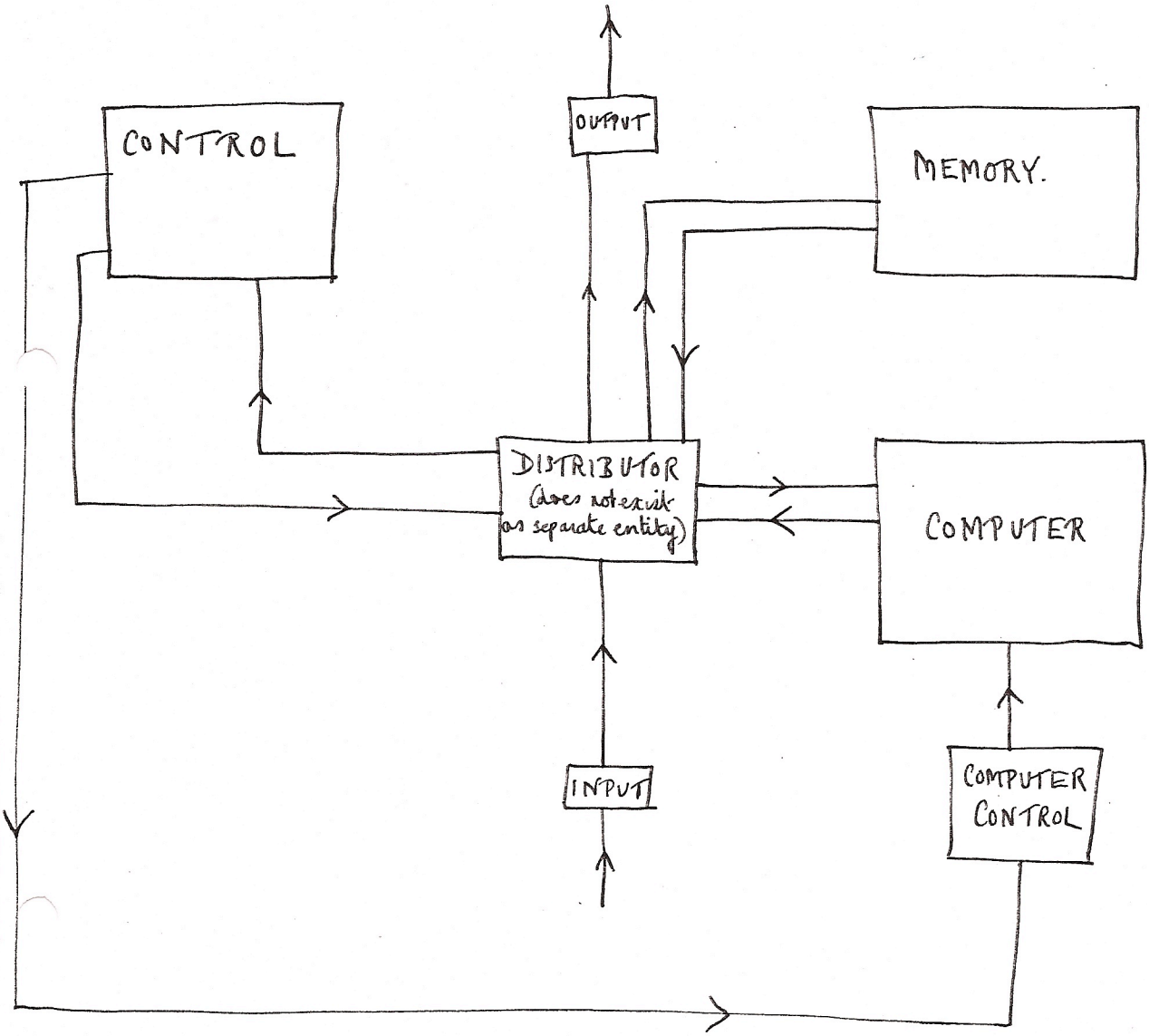
D_0 = Blank.
D_1 = Whether to operate on 1st or 2nd half of M/c
D_2–D_5 = M/C number.
D_6–D_{10} = Tank number.
D_{11}, D_{12} = Spare.
D_{13}–D_{16} = Type of order.
D_{17} = Whether +5 or -10-digit number.

Change 1 O_{17} & O_1 interchanged

Change 2

O_1 becomes 5 or 10 digit
O_2–O_{11} become position digits
O_{12} Spare
O_{13}–O_{17} = type of order

Brief Schematic.



24/1/48

Discussion — (Wilkes – Bennet – Mutch)

Decided:-

1. Retain delay (may be ½ or 1 M/c) between R_1 & reinstalation of Coincidence Unit to prevent possibility of coincidence at (N+1)/18. In the case of a 5 digit number being passed from Computer to Memory via Delay Tank such coincidence would give trouble, as O.F.U. is not set up until (N+1)/16 – i.e. Coder will not allow relevant number into Delay Tank until beginning of next ½ M/C – i.e. (N+1)18. Thus, not until ~~(N+2)~~ will number get thro' Delay Tank, that is ½ M/c after Coincidence Gate.

2. Include in M.C.U. F/F, Gate & 2μsec delay to deal with C.T.O. F/F is set by D_{35} (from computer – indicating ~~sign~~ sign is –ve & ∴ transfer is to take place) & pulses delayed by ½ M/c gate which transfers contents of Delay Tank to Order Tank. At end of ~~get~~ D_{18} resets F/F & sends out R_2 pulse.

2μsec.

26/1/48 (Renwick, Bennet, SHM — later agreed MVW.)

1. 2nd Stir. pulse (delayed as above) coincides with D_{18} (not D_0) to ~~prevent pass. of coincidence before F.U.'s set up.~~ ~~N.B. F.U.'s only set up first half of M/c.~~ provide Stir. Pulse to Computer after F.U.'s set up.
   N.B. F.U.'s only set up during first half of M/C.
2. ~~Stir. pulse from M.C.U. used~~ fed to Computer as well as to Coinc. Unit.
3. For C.T.O., Coinc. Unit to inhibited by preventing stir. pulse reaching it [CTO –ve output closes gate normally open]. This system is more convenient than the suggested method of inhibiting the R_2 pulse in the Coinc. Unit as it avoids the problem of resetting the Coinc. Unit.
4. "Transfer Unit" reinstated (½ M/c Delay tank to effect transfers involving delay from Memory to Computer or vice versa). Necessary because when transferring from Comp. to Memory Coinc. Gate must not come until number has begun to emerge from the delay. But to get Coinc. Gate, Delay Tank ~~must~~ must contain the Order. Thus if Delay Tank was used to effect transfer the Order would be wiped out by the incoming number. Hence necessity to use separate Transfer Tank.
   N.B. This tank does not have to circulate — thus reduces gating complications.

→ later decided gate normally closed & only opened by relevant operations ~~(i.e. not by CTO)~~ (i.e. not by CTO)

Main Control Unit.

This unit has to provide:-

(a) A Stimulating Pulse to the Computer and elsewhere as required, including the Coincidence Unit in ~~the case of operations~~ Stage 1 of the Main Control Sequence and also in Stage 2 in the case of transfers to or from the Memory [N.B it is not applied to the Coincidence Unit in the case of a Conditional Transfer Order, or "CTO"];

(b) Gating waveform to gates G_1 in Stage 1;

(c) " " " " G_2 in Stage 2;

(d) " " " gate G in Stage 2 in the case of a CTO in which a Sign Pulse is received from the Computer indicating that the condition for transfer has been satisfied and that it is therefore desired to connect the Delay Tank to the Order Tank;

(e) A single pulse to add "1" to the Order Tank at the end of each Stage 1.

(f) Pulse R_2 to Computer and to Flashing Units.

Operation is as follows:-

Stage 1

(a) ~~In Stage 1~~ the Start Pulse (or End Pulse) is applied to Flip-flop F_1 via Adder a_1. F_1 is ~~then~~ set & is reset by the following D_{18} pulse providing a Stimulating Pulse ~~to the Computer etc, and also to the Coincidence Unit in the case of those operations (eg. transfers to or from the Memory other than CTO) in which Coincidence is required, the path to the Coincidence Unit being controlled by gates which are opened by gating waveforms from the Order.~~ to the Coincidence Unit via Gate G_3 which is opened by the +ve output of F_2 (see (b) below). The Stimulating Pulse, whenever it occurs, is also fed to the Computer where it may or may not be used in Stage 1.

(b) The Start or End Pulse sets F_2 which provides the gating waveform to set gates G_1 (see Block Diagram of Main Control Sequence). This also opens G_4 allowing the Stimulating Pulse to pass to the Coincidence Unit (see (a) above). F_2 is reset by the R_1 pulse which is separated out from the R_2 pulse by G_4 which is only open ~~during~~ during Stage 1.

(c) The R_1 pulse from G_4 is delayed ~~for~~ 2μs and applied to G_2 together with D_1 & D_{19} so that a "1" is sent to the Order Tank at the end of each Stage 1. The R_1 pulse itself is not used directly to provide the "1" as it may not be of sufficiently good shape.

N.B. The Order Tank must have "end round carry" inhibited so that the first half of the first m/c of the first tank of the Memory may be made use of.

Stage 2.

(a) The R_1 pulse from G_4 is applied, via adder a_1, to set F_1 again so that ½ or (M/C later D_{18} resets F_1 providing another Stimulating Pulse to the Computer etc. In the case of those operations (e.g. transfers to or from the Memory) in which Coincidence is desired, this pulse also passes to the Coincidence Unit via G_2 or G_3 which are controlled by the relevant outputs of the Coder.

N.B. D_{18} has to be used to control the Stimulating Pulse and NOT D_0 in order that the Reading Units (which only set up during the first half of a Minor Cycle) are set up before the Stimulating Pulse passes to the Computer.

(b) The gating waveform for G_2 is supplied by F_3, which is set by the R_1 pulse from G_4. At the end of Stage 2 F_3 is reset by the R_2 pulse which is applied via adder a_3 and gate G_5. Without G_5 R_1 would tend to both set & reset F_3. ~~From G_5, R_2 is also taken out to the Computer where it is used to stop the computation if such is required & does nothing at all at other times.~~

N.B. (i) In the case of a "transfer to Memory" operation the MCU has to provide the End Pulse. R_2 is used for this, being routed to the "End Pulse" input via G_6 which is opened by the +ve "transfer to Memory" output from the Coder.

(d) The ½ M/C CTO gate is provided by F_4. This is set whenever a pulse A_0 is received from the Computer, A_0 in this case being the Sign Pulse, A_{35}, delayed by 1 μsec. in the Computer. ~~From~~ F_4 is reset ½ M/C later by D_{18}, which is allowed through G_8. In this case no End Pulse is received from the Computer, & no R_2 Pulse is received from the Coincidence Unit, which has not been stimulated. The MCU has therefore to provide both these pulses. D_{18} from gate G_8 is used being commoned with the other End Pulse lines & being added to the other R_2 pulses by adder a_3.

N.B. Commoning the End Pulses will suffice, no adder being necessary as End Pulses do not affect the operation of either G_6 ~~or F_4~~ G_8 or F_4, and F_3 is protected by

Main Control Sequence

A. Two parts:-

(1) To extract correct order from Memory & hold "operative part" until required;

(2) to extract number specified in order from Memory & transfer to computer together with "operative part" of order.

B. Control system consists mainly of:-

Main Control Unit:- emits various gating & controlling pulses

Coincidence Unit:- selects correct minor cycle, letting pulses through from memory by emitting 'coincidence gate'.
N.B. a counter counting half-minor cycles is associated with this unit in order that it shall know when any relevant minor cycle has been reached.

Tank No. Flashing Unit:- selects the correct tube of the main memory. This unit (known by N.P.L. as a "Staticiser") consists of five flip-flops. An order contains information re tank number in pulses D_6 --- D_{10}. (these are sufficient, on the Binary system, to designate any of the 32 tubes). Each of these pulses actuates one of the flip flops, which ignore all irrelevant pulses as they are each gated with pulses from the Digit pulse generator which coincide in time with the respective D_6-D_{10} pulses. (known as 'D' or Digit Pulses.)

The outputs from the flip-flops are fed to two Decoders, one controlling the Input Gate & one the Output Gate of the main memory. Each decoder has 32 outputs, the correct one being actuated by the configuration of pulses obtained from the flip flops. N.B. in order to work out whether the Input or Output decoder is concerned in any particular case, a further pulse (say D_{13}) has to be fed in from the Order Register

Together with the Coincidence Gate this forms an Order Transfer System so that any order fed to the switching device is routed to the correct minor cycle of the correct tube of the memory.

Order Flashing Unit: Similar to Tank No. F/U. Four flip-flops set up by pulses D_{13}–D_{16} of order. Associated with Decoder with 16 outputs, each specifying a different type of order. These outputs are fed to the Computer Control via the Order Coder.

N.B. One pulse (say O_{13}), designating Input from or output from Memory has also to be fed via the Tank No. 4 F/U. Decoding system.

Order Tank: ½ M/C tank containing ~~details of~~ the number of the place in the Memory which contains the next order to be executed.

N.B. (i) Tank probably contains all 18 pulses, but all except 1–10 are ignored
(ii) A "carry" operates continually ~~the~~, and at the end of each operation a "1" is fed in from the N.C.U. thus specifying the next order unless a Controlled Transfer Order is introduced
(iii) Initially the Order Tank contains nothing, thus specifying the first place (called actually "place 0") in the first tank of the Memory.

Delay Tank: ½ M/C tank which:-

(a) holds order, when received from Memory, until required
~~(b) Delays any 5 digit number occurring in first half of M/C by half a minor cycle.~~

Transfer Unit: ½ M/C ~~tank~~ which does not circulate.

This unit is in the path from Computer to Memory or vice versa & is used to delay a 5 digit number occurring in the first half of a Minor Cycle. In other cases it is by-passed.

N.B. (i) When "0" pulses are "staticised" in Flashing Units they are known as "F" pulses (actually these are D.C levels, not 1μs pulses)

~~(ii) D pulses should really only refer to actual regular pulses obtained direct from the Digit Pulse Generator (a sort of basic pulse generator following the Clock Pulse Generator).~~

(ii) There must be two more Flashing Units to deal with pulses O_1 & O_{17}. O_1 becomes F_1 & controls a gate switching the Transfer Unit into the Memory — Computer Path. F_{17} is fed to the Coincidence Unit to control the length of the Coincidence Gate.

Gate G_5 which is closed as F_3 is ~~already~~ reset.

(f) Pulse R_2 from G_5 is fed in all cases to all Flashing Units, except the Order Flashing Units, and to the Computer. In the Computer it sets off a computation if such is required, but is not used at other times.

Note 1 — Reason for G_2 + G_3

In operations (e.g. CTO) where Coincidence is not required it could be prevented by inhibiting the emission of the Coincidence Gate by applying a suppression pulse to the stimulated Coincidence Unit. However an end pulse would remove this suppression (by resetting the O.F.U.) but would not reset the Coincidence Unit, so that Coincidence could occur as soon as 1/2 M/C later, ~~at this~~ which point the OFU would not have been set up again.

It is therefore preferable not to stimulate the Coincidence Unit except in cases such as transfer to or from the Memory in which Coincidence is required. In such cases G_2 or G_3 opens and allows the Stimulating Pulse through to the Coincidence Unit

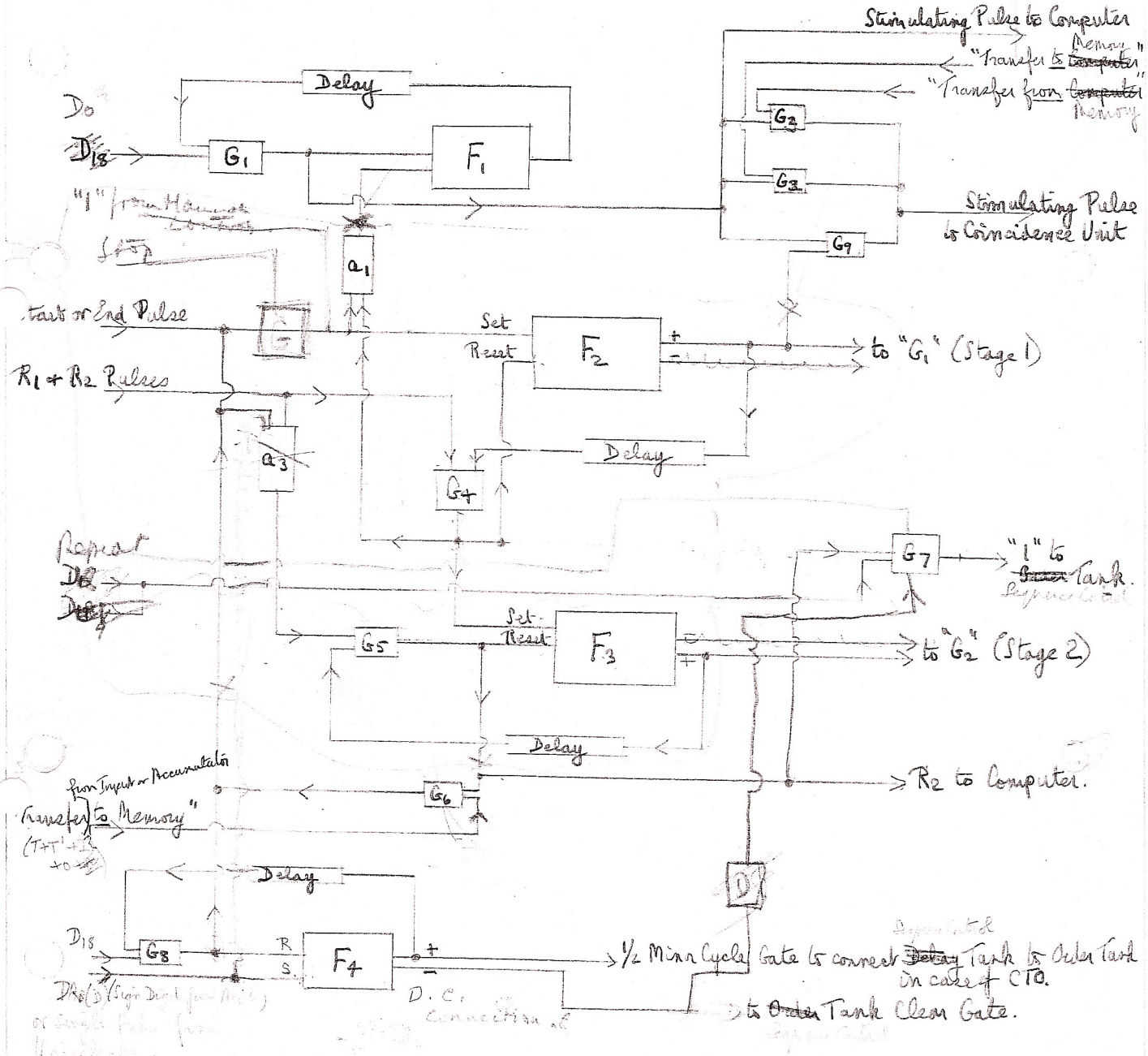
Note 2:—

Adder a_1 is necessary to add R_1 and the Start or End Pulse which must be delayed until the following Do before triggering off the Stimulating Pulse. The lines cannot be commoned as the End Pulse would then be applied to G_7, providing an unwanted "1" to the Order Tank.

Note 3:—

F_3 could be reset by the End Pulse instead of R_2 if:—
(a) R_2 did not have to be provided to the Computer, &
(b) the MCU did not have to provide the End Pulse in cases of transfer from Computer to Memory.

Main Control Unit Block Schematic Diagram.



30·1·48.

Coincidence Unit.

This unit, after stimulation, has to provide a Coincidence Gate either ½ or 1 M/c in length, depending upon whether the number to be dealt with has 5 or 10 digits; followed by an R≡ pulse which occurs 1 M/c after the beginning of the Coincidence Gate.

The operation is as follows:—

Incoming D_0 & D_{18} pulses are added together in a_1, delayed by 2 μs and used to set F_1. This flip-flop, however, is always reset immediately, except when coincidence occurs, as will now be explained.

G_1 is fed with pulses from the Counter Tank, while G_2 receives pulses from the Order Tank in Stage 1 and from the Delay Tank in Stage 2. The unit has to establish "coincidence" when the "position" pulses in these two tanks (i.e. pulses $O_1 - O_5$ or $O_{19} - O_{23}$) are the same. All other pulses in the ½ M/c are ignored by gating G_1 & G_2 with the output of F_2, which is set by each incoming D_0 or D_{18} pulse & reset by each incoming D_6 or D_{24}.

The pulses which get through G_1 are fed directly to G_4 and are also fed to G_3 via a reversing stage. Similarly, those getting through G_2 are fed to G_3 directly & to G_4 via a reversing stage. Thus there will always be an output from either G_3 or G_4 except when the outputs of G_1 & G_2 are identical — i.e. at coincidence. The outputs of G_3 & G_4 are added together in a_2 & used to reset F_1 which is therefore always reset except at coincidence. *

The Stimulating Pulse is used to set F_3 whose output is fed via Delay d_3 to the Triple Gate. Together with the output of F_1 this opens the Triple Gate soon after coincidence so that the next D_0 or D_{18} pulse passes through the Triple Gate. ~~Note that Delay d_3 is necessary so that F_3 is set in time for D_0 to get through the Triple Gate & not at the same instant as F_1 closes the Triple Gate.~~

This pulse is used to reset F_3, so that no further coincidence is possible until the unit has been restimulated. It also sets

F_4 whose positive output to the Coincident Gate. If this Gate begins on a D_{17} pulse it must end at the following D_0. If it begins on a D_0 it must also end on the following D_0 unless a five digit number (or order) is concerned, in which case it will end on D_{18}. The presence of pulse D_{17} indicates a five-figure number. This will set a flashing unit whose negative output, F_{17} is gated with D_{18} to produce a reset pulse for F_4. The alternative D_0 resetting pulse is added to this in a_4 and applied to the Reset line of F_4 via G_6 and Delay d_4 which ensure that F_4 is not set & reset at the same time.

The output of the Triple Gate forms the necessary R pulse by being delayed one minor cycle in d_5 and then gated with D_0 or D_{18} to produce a clean R pulse.

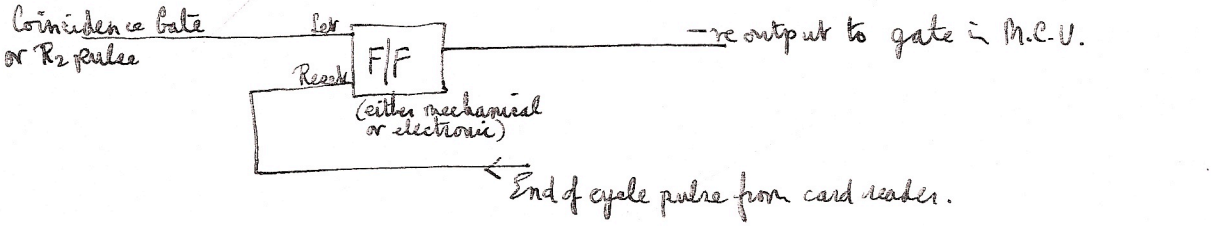
Delay d_1 is necessary to delay the D_0 setting pulse of F_1 because, except during D_1—D_5 there can be no output from G_1 or G_2 and thus F_1 cannot be reset. If this D_0 were not delayed F_1 would set almost immediately and, if the unit were stimulated the same D_0 would get through the Triple Gate and cause a false Coincidence Gate to be emitted.

Effect of "Input" on Main Control Sequence.

(Bennet – 29/1/48).

If an "input" order comes up on Coder before cycle completed execution of input to Memory must be either (a) inhibited or (b) repeated in the same position until the Input relays show the correct configuration.

In (a), Stimulating Pulse must be inhibited by inhibiting the gate which would normally be opened by the Coder. This would require one gate & one C.F. in MCU, but suppressor suppression might be used so that no extra valves were needed in the MCU. In the Input Unit the following would be necessary:-



This method seems neater than (b) as the coincidence gate only comes up when required thus making it unnecessary to inhibit the adding of '1' to the Order Tank, and also preventing a succession of wrong inputs to the same position in the Memory before the right input is available.

In (b), the adding of '1' to the Order Tank must be inhibited as it may be necessary to repeat the same operation several times until the relays are correctly set and the correct input can go to the Memory. In this case R_1 cannot be used to control the addition of '1' as it occurs before the Coder is set up – i.e. before the fact of an Input order is known. The End Pulse must then be used instead of R_1: R_2 could be used, but in many cases it is coincident with the End Pulse.
In this case the addition of '1' must also be inhibited in the case of a CTO (the CTO ½ M/C gate in the MCU may be delayed & used to accomplish this).
The inhibition will involve 2 C.F's & one diode gate in the MCU.

Preliminary Notes on "Input"

1. Teleprinter → tape punched in sequences of 5 holes → Tape Reader → Input Storage Relays → Memory.

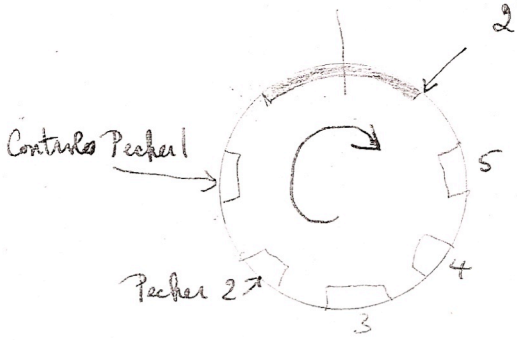
2. Intermediate Memory (= 5 storage relays) necessary as input operations require very much more time than computations inside machine. ∴ machine must be able to perform computations while Input is operating, having always one new input available on relays.

3. To input whole Number, done in steps, 5 digits at a time. These digits are fed to 5 least sig. places in M/c's Memory. Then, while Input is setting up next 5 digits on Relays machine translates first 5 from Memory to Accumulator, shifts to five places to the right & puts back into Memory. Next 5 digits, when available, then go into last five places in Memory. Process is repeated until whole Number has been built up in Memory.

4. Tape Reader has Shaft driving Cam which controls five 'Feelers' which read holes in tape. Each Feeler sets up one of the five Relays if it goes thro' a hole in the tape. The Shaft is controlled by a Clutch which is energised by a solenoid & operates so that once energised it causes the shaft to make one complete rev^n.; the Energising pulse not needing to last until the end of the rev^n.

5. Should two Input gates follow closely (i.e. in less time than that taken by one rev^n of the Shaft) the machine must be stopped as soon as it has dealt with the information fed in by the first one (which comes direct from the Relays which would be already set up), until the shaft has had time to revolve once & set up the relays again. Thus each Input gate must set up a condition so that if another gate occurs "immediately" the usual "1" must be stopped from going into the Signum Tank, i.e. the machine will go on repeating the same cycle until the relays are set up again & their whole output can be fed into the Memory. The "1" can then be added, the Input disconnected from the Memory, and the shaft make a further rotation so that the Relays can be set up against the time when their output is required once more.

6.



7. Brief Input Sequence.

(a) Shaft Initially at Rest: –

Receipt of I. gate causes:–

(i) Path from Input to Memory to be set up;
(ii) on Coincidence, 1st ~~[illegible]~~ Number is fed from Input Relays to Memory;
(iii) Clutch engaged so that shaft makes one rotation;
(iv) condition is established so that if another I gate comes up before end of rotation, the addition of '1' to the ~~[illegible]~~ Tank will be inhibited;
(v) Condition of preparedness for inhibition, to be stopped as soon as shaft comes to rest (i.e. as soon as Input Relays are set).

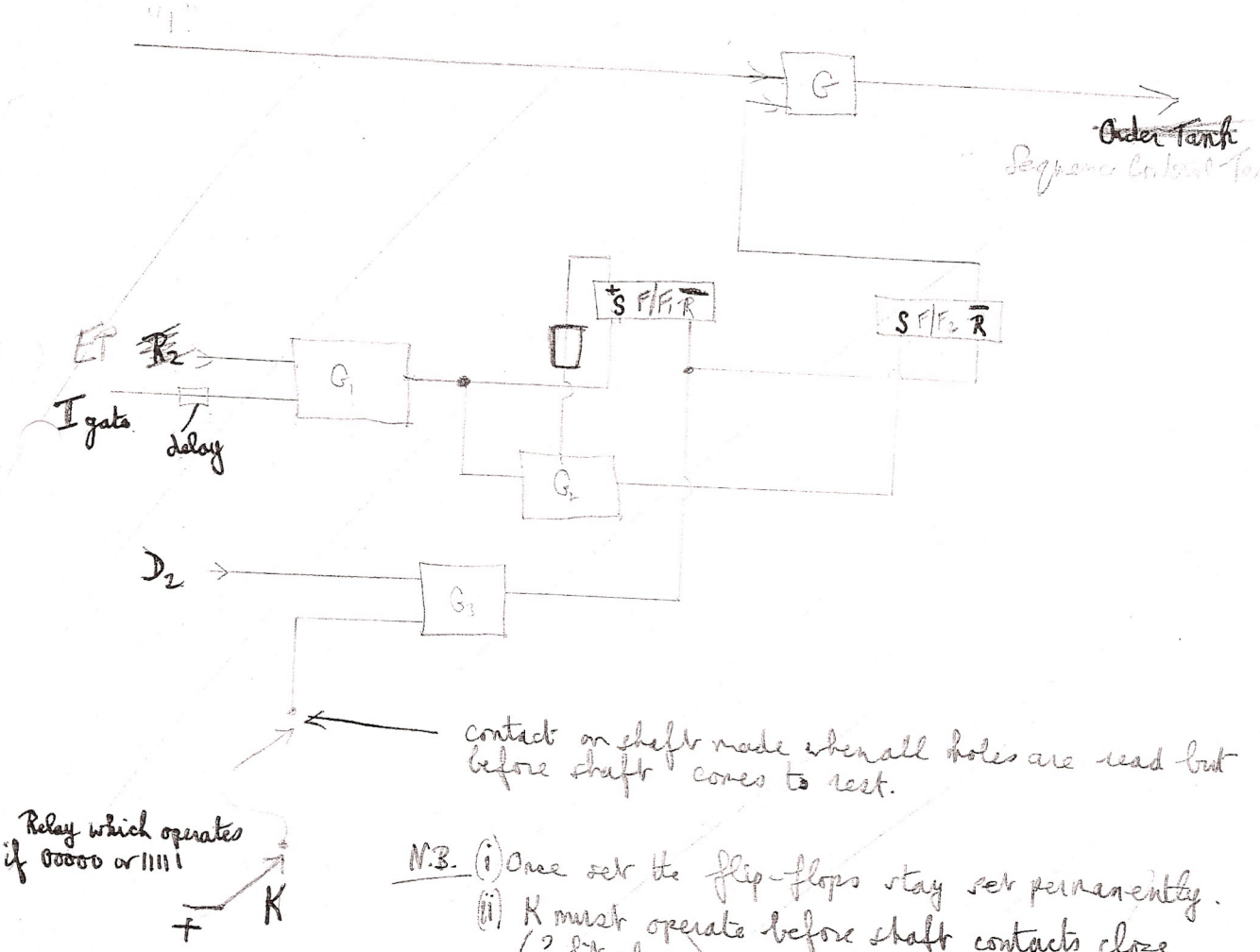
(b) Shaft Initially Rotating: –

Receipt of another I gate causes:–

(i) '1' to be inhibited;
(ii) path to be set up from Input Relays to Memory;
(iii) at each Coincidence, number on Relays to be transferred to Memory;
(iv) shaft to be prevented from stopping (or restarted);
(v) inhibition to be stopped as soon as new number has been transferred, but condition of preparedness for further inhibition, in case of receipt of another I. gate, to continue until shaft has made further rotation & set up relays once more.

'Input' — contd.

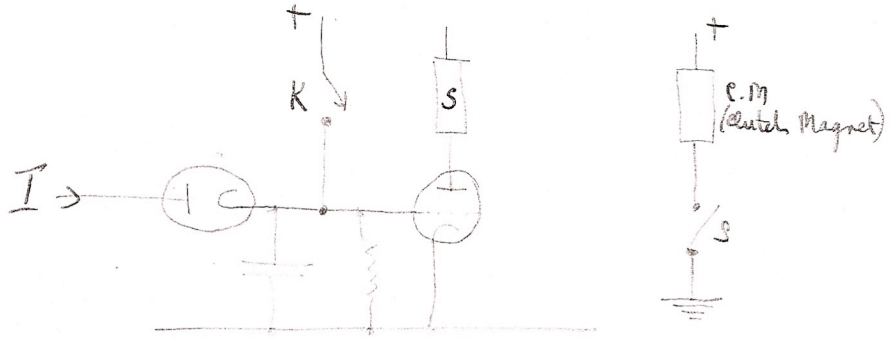
8. Proposed System for Inhibition of 'I' to ~~Order Tank~~ Sequence Control Tank.



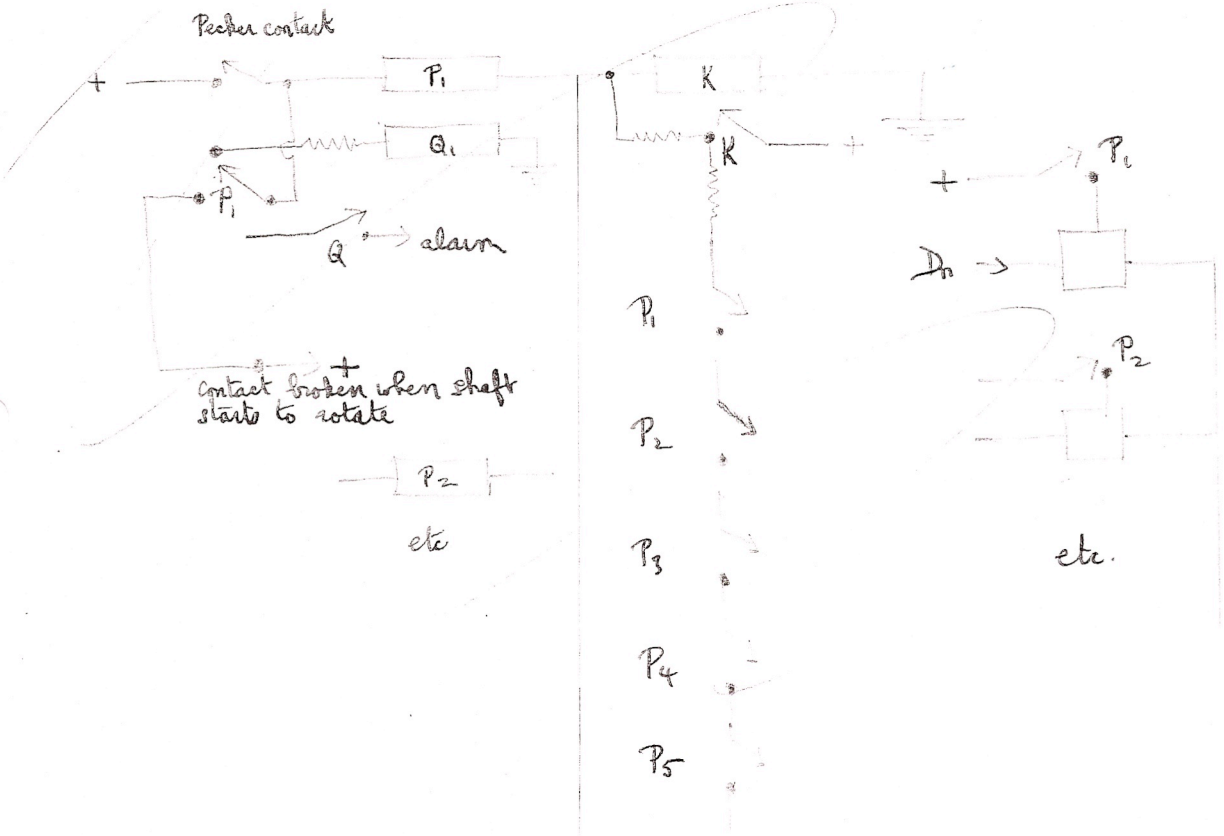
← contact on shaft made when all holes are read but before shaft comes to rest.

N.B. (i) Once set the flip-flops stay set permanently.
(ii) K must operate before shaft contacts close (? for alarm)

1. Tape Feed Control.



10. Input Relays :-



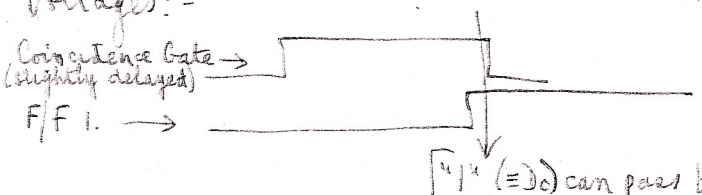
Notes on Inhibition of "1"'s etc for Input and Output.

1. As soon as an Input or Output order ceases a condition must be set up at electronic speed so that a further I or O order, which can occur as soon as 4 M/C's later, causes inhibition. However, this inhibition must be "taken over" at some stage by a relay (altho' due to its slow operating time, a relay cannot be used to initiate it) so that when the shaft reaches the correct position it resets the relay & so ends the inhibition.

2. A relay cannot be used to control the requisite gate directly as, in closing, its time of rise may be very slow. Hence it might result in pulses of doubtful amplitude getting thro' the gate with unfortunate consequences. Relays then can only be used to control the setting & resetting of flip-flops — via gates if necessary — where time of rise is not important as the F/F is either set or reset & cannot have any awkward intermediate stages.

3. For inhibiting "1"'s we can get away with a single F/F which, with suitable delays, can be arranged to open the gate for about 2 μsec. For inhibiting ~~digits~~ input of digits to the Output flashing Units however the gate must be open for a whole minor cycle in the case of the first O order & then closed subsequently. This needs two F/F's — but one can be the same one as is used for inhibiting the "1".

4. N.B. The method of inhibiting the "1" depends on being able to open a gate for just sufficiently long for the first "1" to get through. This is done by the overlapping of two gating voltages:-



["1" (=Do) can pass this gate here]

If the coincidence gate should end ½ M/C before R_2 (which pulse provides the "1") this system obviously will not work. Thus, for the moment:-

Input & Output can only be made to or from a Whole Minor Cycle of the memory.

Possible remedies are:-

(a) research to find a method of delaying a gating voltage (i.e. the case the Coincidence Gate) by slightly more than ½ M/C. This can be done with a short pulse (e.g. 2 μsec) by means of a phantastron, but no means exists of coping with a pulse of order 36 μs. ? ordinary delay line as time of size does not matter very much ??

(b) In Coince. Unit, pulse which sets F/F emitting C.G. is delayed 1 M/C. & then used as R_1 or R_2. If this delay was replaced by another F/F which was set by the pulse which now resets the C.G. F/F, & reset by the following D.18, its reset pulse could be used as R_1 or R_2 which would thus always occur as a D.18. Further the output of the F/F could be used for inhibition in place of the C.G. and, as it always coincides with the Rpulse, whatever the length of the C.G., it would enable Input or Output to be made from any ½ or whole M/C in the memory.

5. In the Input Unit all "1"'s not occurring as the result of an I order are allowed to pass via a gate G_4. This gate is inhibited by a Coder output for I & should also be inhibited for O. Note that G_4 need not be duplicated in the Output Unit although the rest of the inhibition circuitry must be duplicated as I & O coders could follow one another very closely. The extra circuitry & core mat. Inhibition & digits to F/U's is, of course, peculiar to Output. It will probably be built into a separate panel so that the other panel will be interchangeable between Input & Output. For this reason too the Output Unit may well contain a G_4 altho' it will, of course, normally be disconnected.

Overloading of Accumulator due to Left Shift.

(point raised at Colloquium on 29/4/48)

During Input of Orders, digits are fed into L.S. position of 2nd½ M/cy M.S. half of Accn & gradually shifted left into position. When the final shift is made, if 0_{35} happens to be 1, the adjacent position = the accn (i.e. the "second sign digit") will be 0 & thus the alarm bell will ring. The same situation may arise in double length arithmetic when the L.S. half of a 2o digit number is moved into the M.S. half of the accn prior to a T or T' order.

(N.B. it will not arise when an order is put into the accn for an arithmetic operation to be performed upon it because if 0_{35} is a 1, the computer will consider the order as a negative number & automatically add a 1 into the 2nd sign digit position).

This point was discussed at some length on 29/4/48 by W.R., J.M.B., E.N.M. & D--, with B.W. & Dr. Hartree part time.

Possible solutions seem to be as follows:-

1. If it can be agreed that an alarm is not necessary for an L order, devise an alarm system which works on the added 1 so that the bell rings if a carry occurs into the 35th position.
2. If the alarm facility is needed for L orders, introduce an L' order for input purposes which automatically switches out the alarm.

(not a satisfactory scheme)

3. ~~Alternative to 2:-~~

(a) To clear input difficulty put digits into most sig. positions of accn & shift right.

N.B. means must be found of preventing the CCU from adding a 1 to the second sign digit position whenever the most sig. digit of any group of 5 digits is a 1.

(b) To clear double length arithmetic trouble introduce new order, T" which allows number to be taken out of least sig. half of accumulator.

N.B. numbers thus must previously have been shifted one place to the right.

3. Alternative to 2:-

Either:-

(a) Put digits into most sig^{t}. position of Accumulator & shift right :-

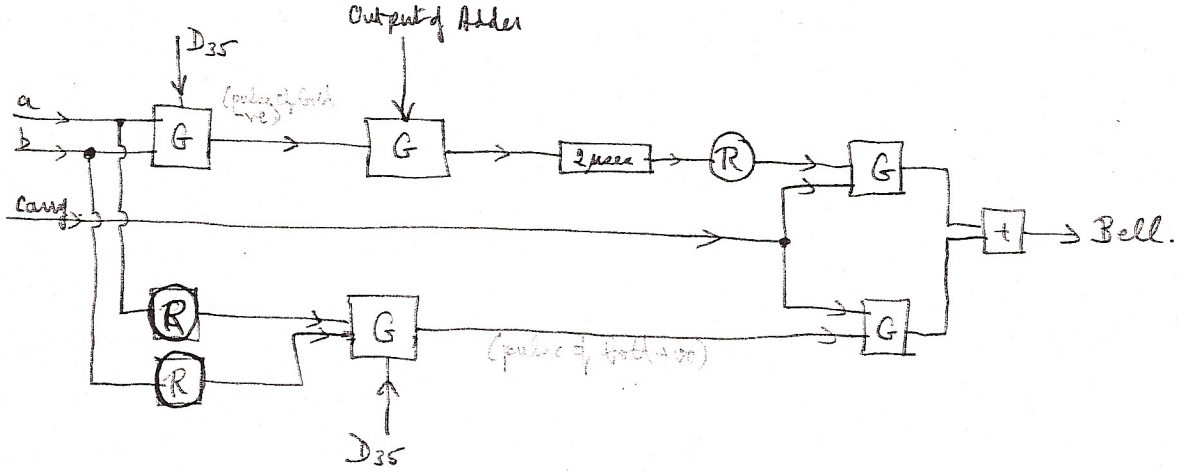
i.e. put digits into these places 4 at a time & shift right. The 35th place must always be 0 to avoid addition of 1 by the CCU. At the end however, when the last of order is put in (either by 5 digits at once or a single 0_{35}) the CCU will add a 1 if 0_{35} is 1, but no further R. shift is necessary & the extra 1 is lost when the order is transferred to the acc^{r}.

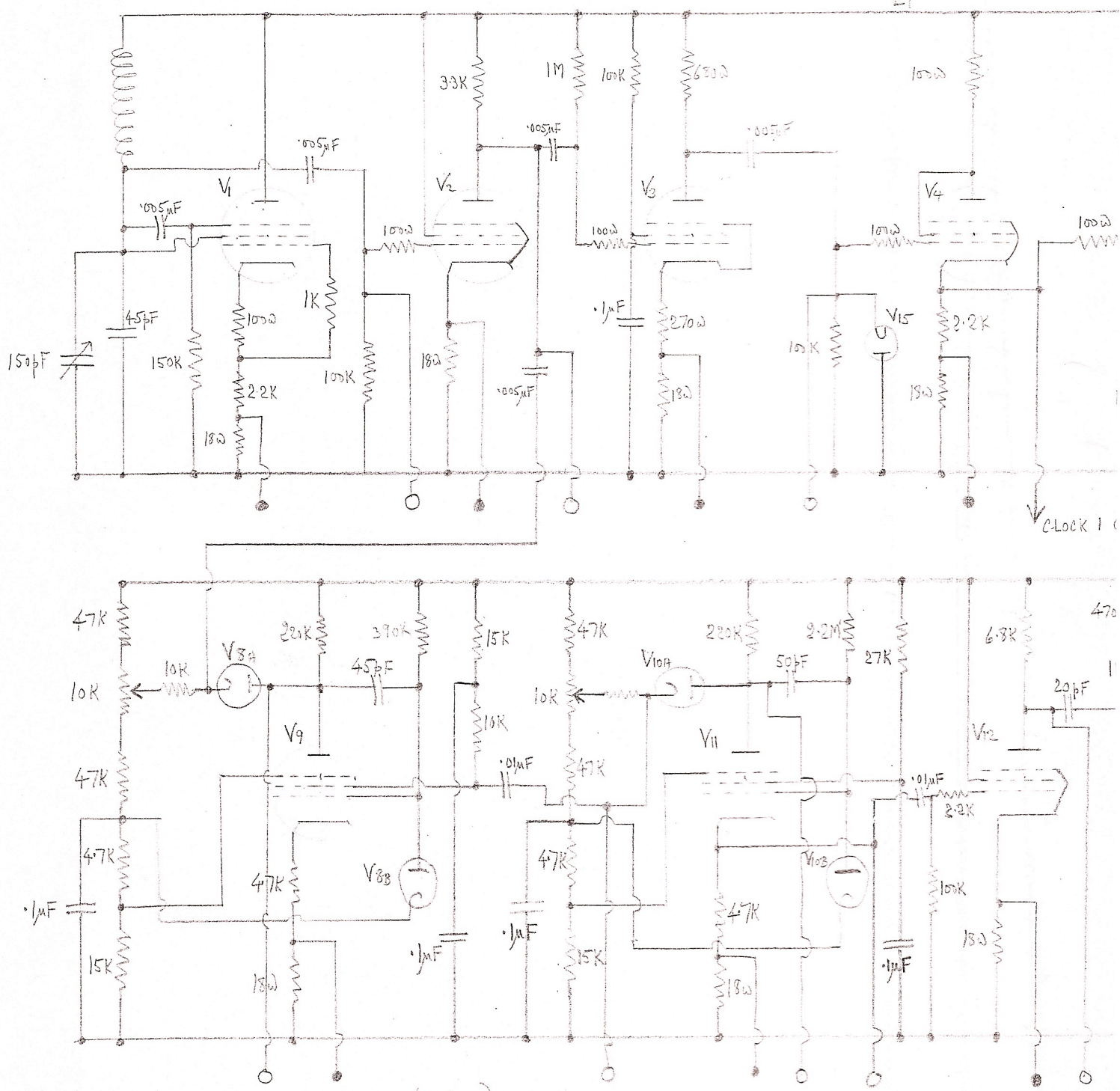
(b) Put digits into least sig^{t} part of most sig^{t} half of acc. & shift right into least sig^{t}. half. Then when whole order has been built up use new order T" which allows no. from least sig^{t} half of accumulator to be transferred to memory. This needs (i) D_1–D_6 wired to input relays; & (ii) a whole minor cycle of training to put the digits into initially.

4. The new T" order is the answer to the double length arithmetic trouble, the T" order being preceded by a shift of one place to the right (this is instead of shifting the number in the least sig^{t} half of the acc^{r} several times to the left & taking it out of the most. sig^{t} half as normally by a T or T' order.

5. Detail for 1.)

If both nos. are +ve or −ve may overload, but if one +ve & one −ve cannot overload (unless one was already too large)
Thus can show if both +ve → overload if carry between 34th & 35th positions
& if both −ve → overload if 1st carry between 35th & 0th positions while 35th digit becomes zero.
Thus some such scheme as following may cope:−



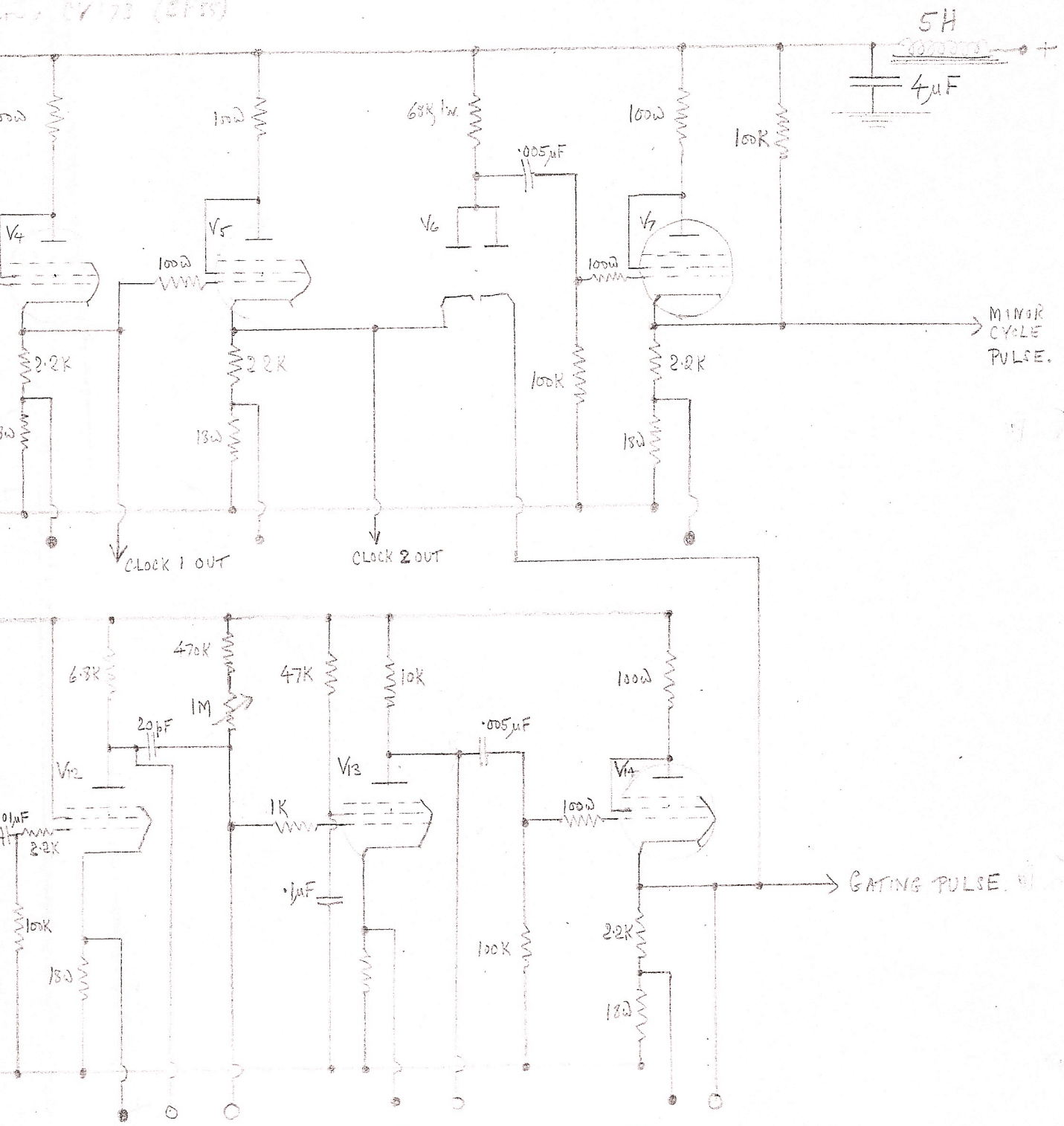


V_1 = EF 50, V_3 = EF 55 (CV173)

$V_2, V_4, V_5, V_7, V_{12}, V_{13}, V_{14}$ = EF 54 (VR136)

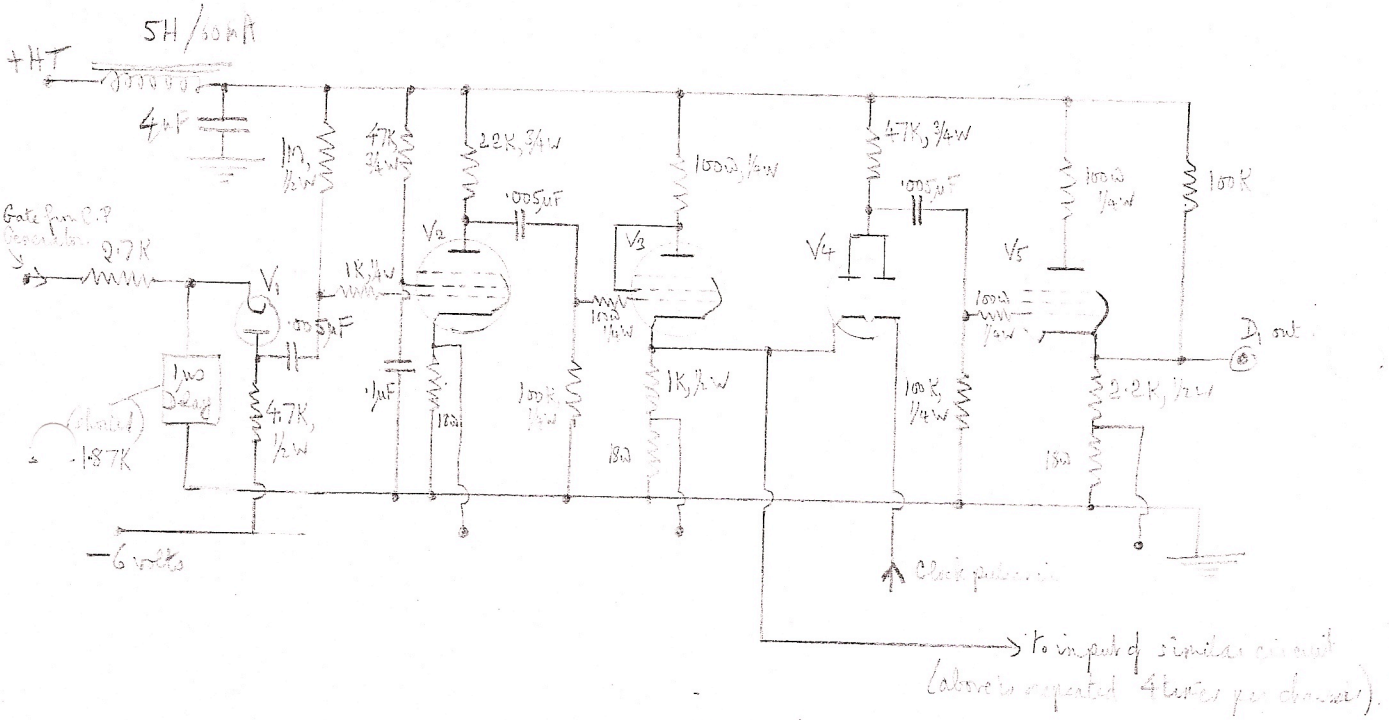
V_9, V_{11} = VR 116 (Mazda VS72)

$V_{15}, V_6, V_8 + V_{10}$ = EB 34 (VR54)



EDSAC — PANEL 2.

CLOCK PULSE GENERATOR.

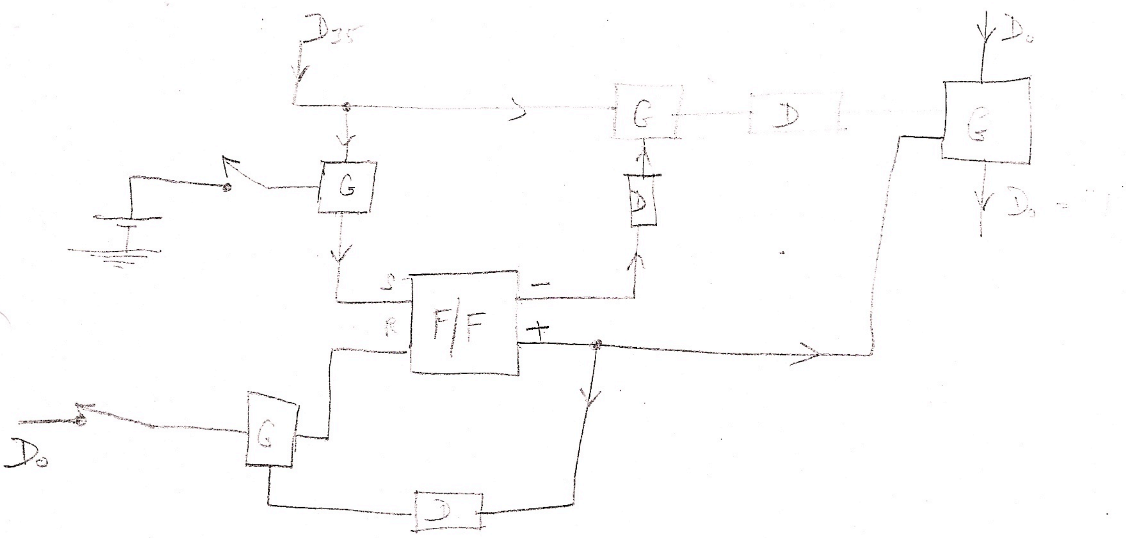


$V_1, V_6, V_{10}, V_{15}, V_{19}, V_{23}, V_{28}$ & V_{32} = E83CC (VR138)

$V_2, V_3, V_4, V_5, V_7, V_8, V_9, V_{11}, V_{12}, V_{13}, V_{14}, V_{16}, V_{17}, V_{18}, V_{20}, V_{21}, V_{22}, V_{24}, V_{25}, V_{26}, V_{27}, V_{29}, V_{30}, V_{31}$ & V_{33} = EF54^V (VR136)

Decoupling condensers = 1 type, 350–400V D.C. Wkg.
All other condensers = paired.

EDSAC, PANEL 3: LIGHT PULSE GENERATOR.



Suggested scheme for for adding single "1" to S.C.T. on push button?

(Bennett 26.2.48.

Decisions 8/3/48.

1. $D_{19} - D_{35}$ on Uniselector for Initial Input.
2. $D_{19} - D_{23}$ on Tape.
3. F.U.'s set up in 2nd half of M/C to avoid provision of large no. of new D.P. G's.

— agreed MVW.