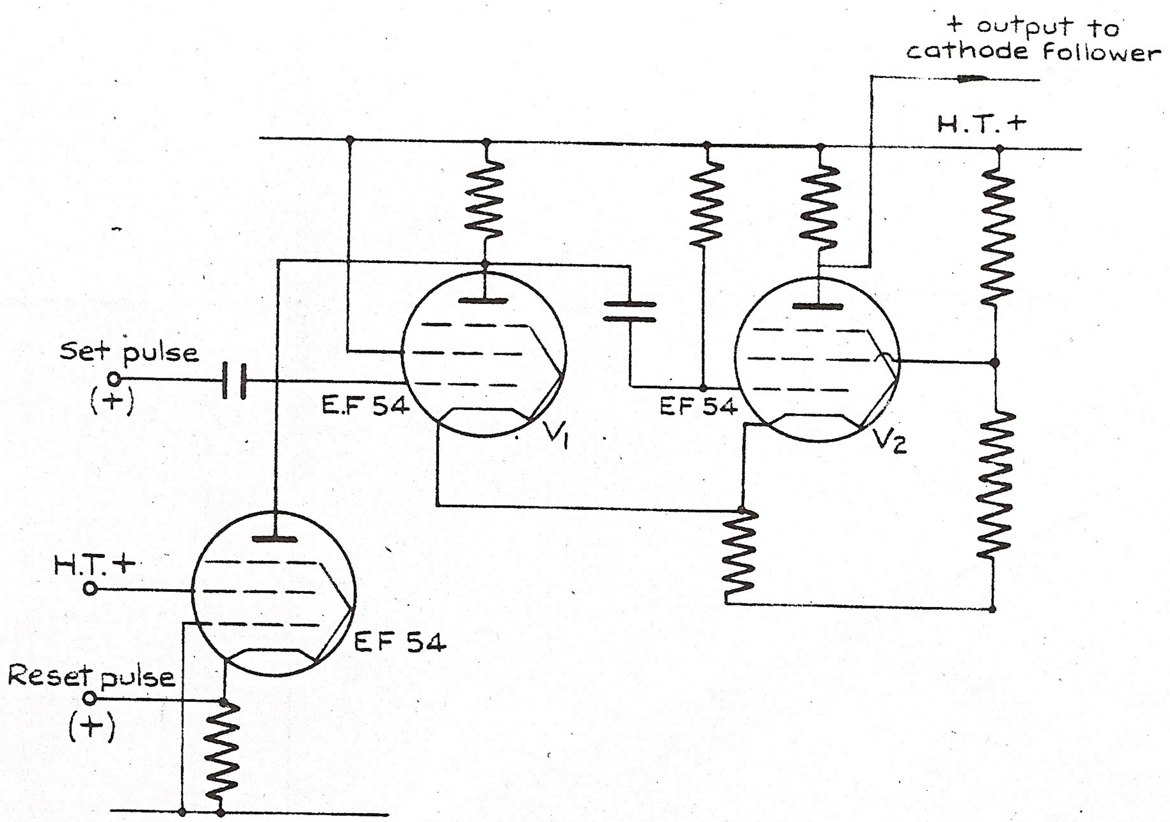


Fig. 5. BASIC CIRCUIT OF FLIP-FLOP

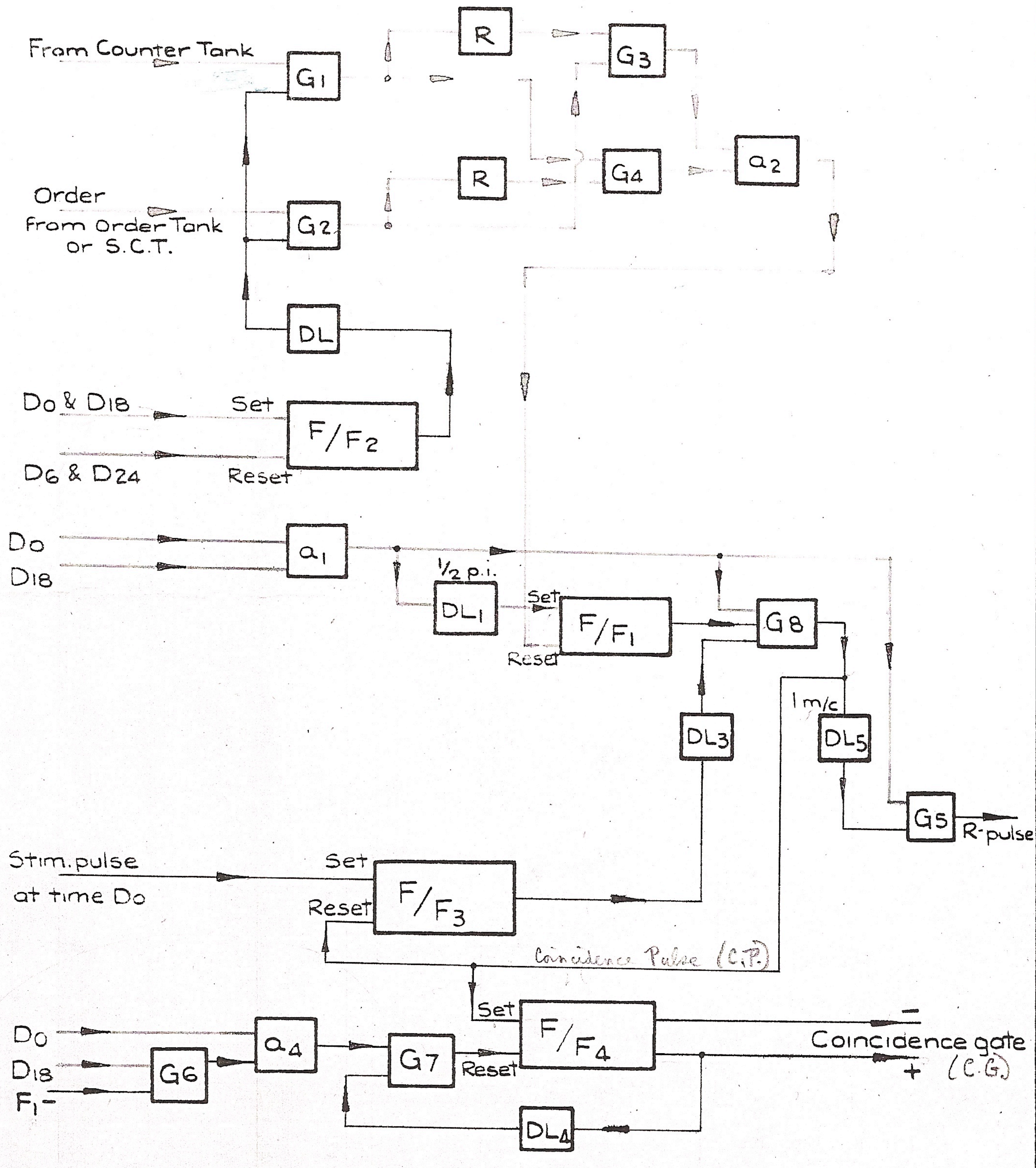


Fig. 6 COINCIDENCE UNIT

G = gate R = reverser a = adding diodes
F/F = flip-flop DL = delay line

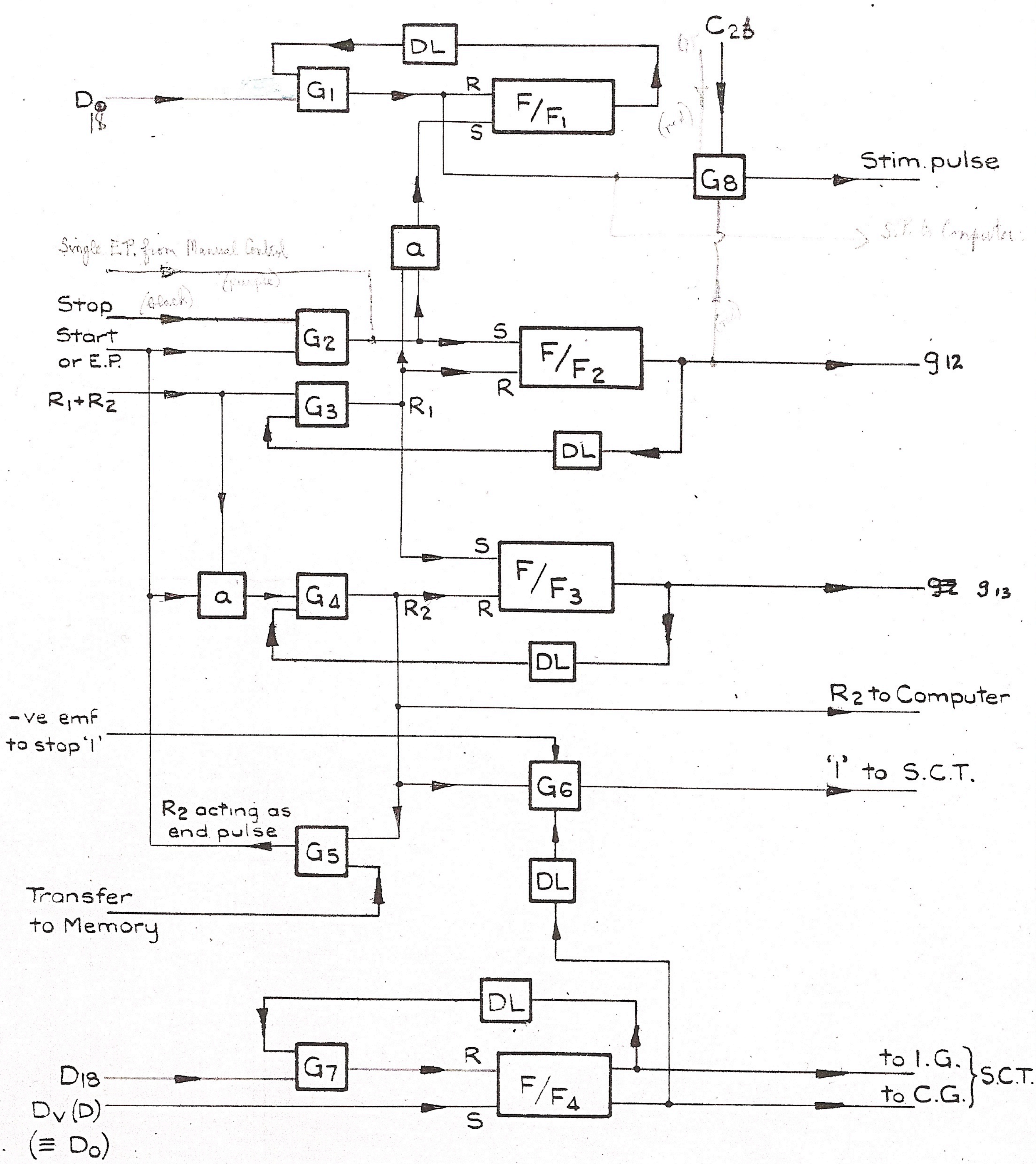


Fig. 7 MAIN CONTROL UNIT

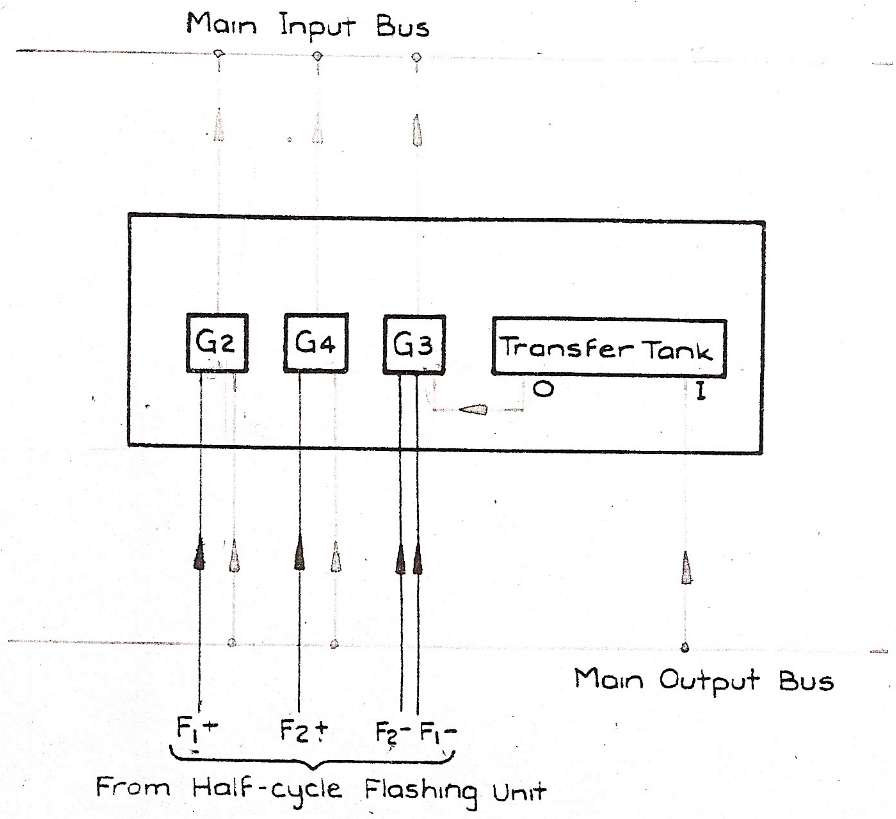


Fig. 8 TRANSFER UNIT

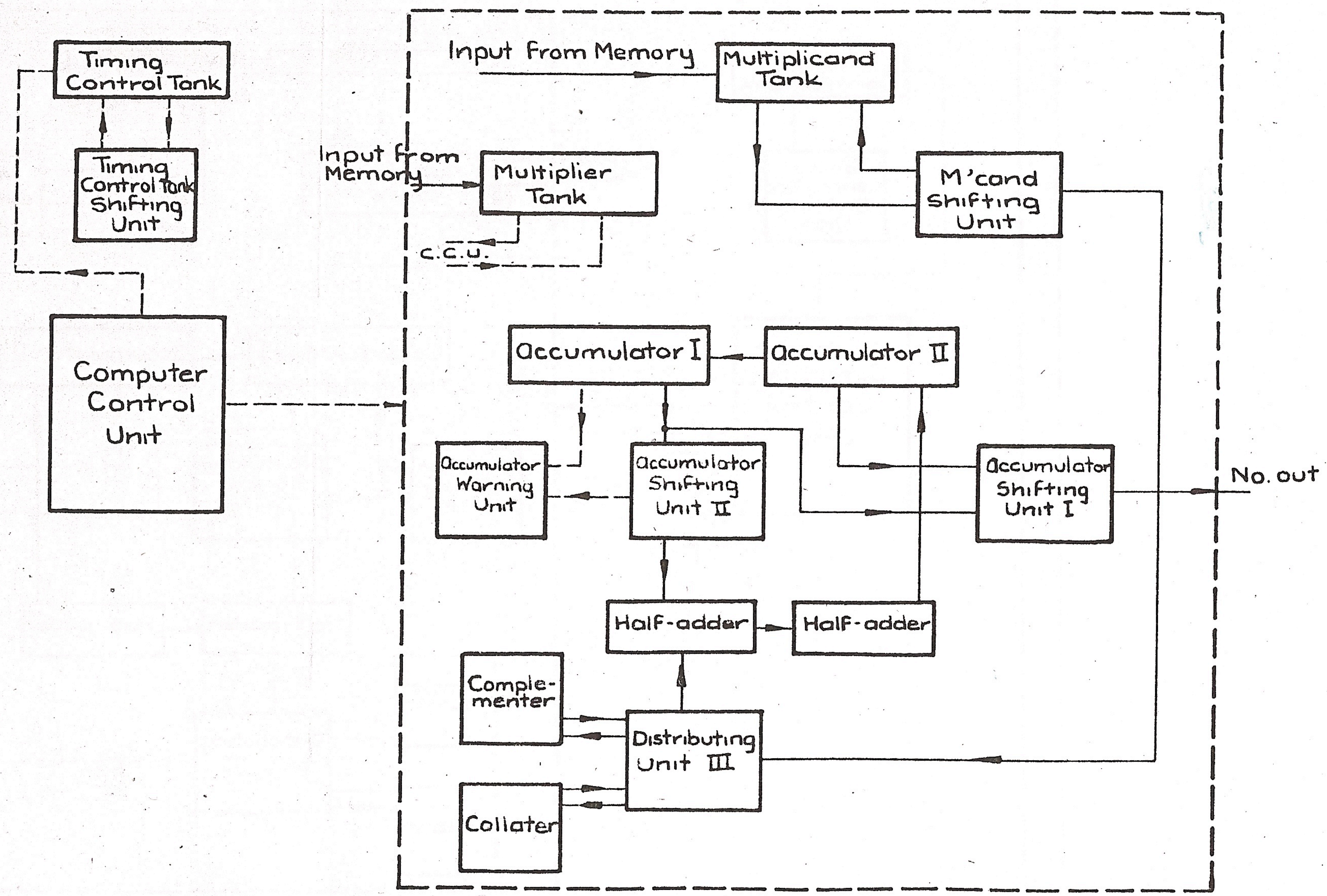
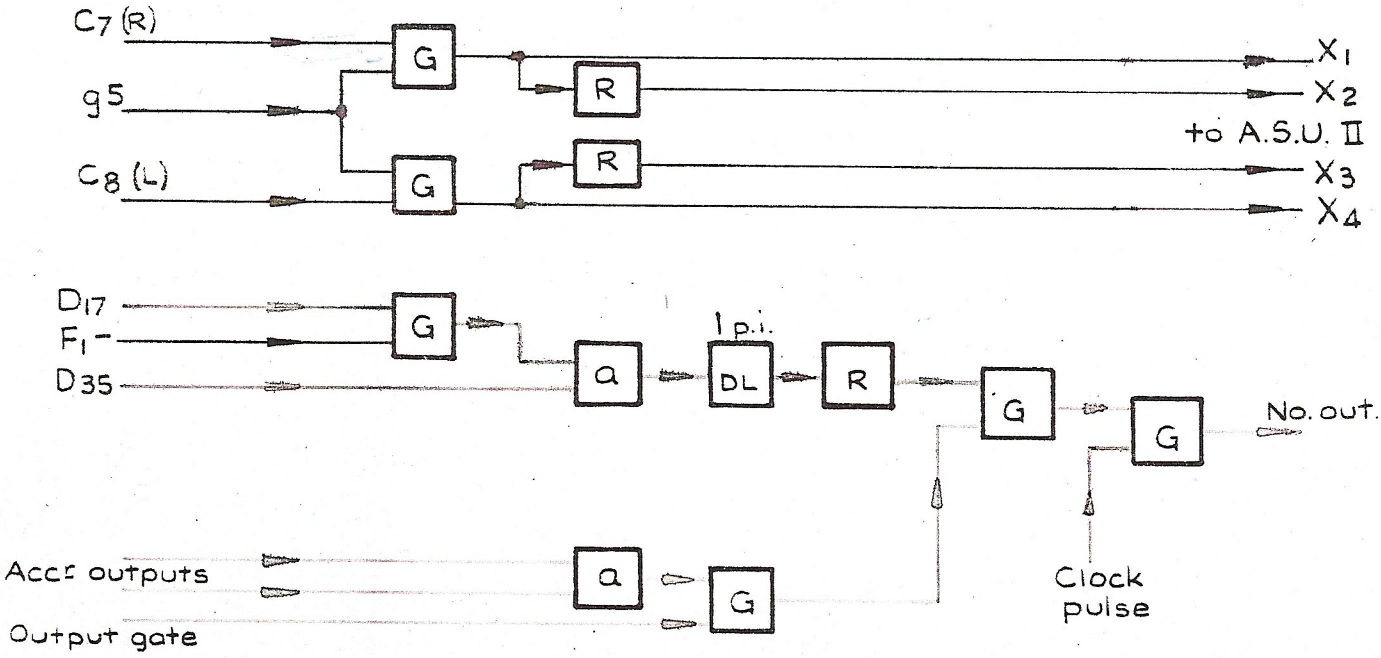
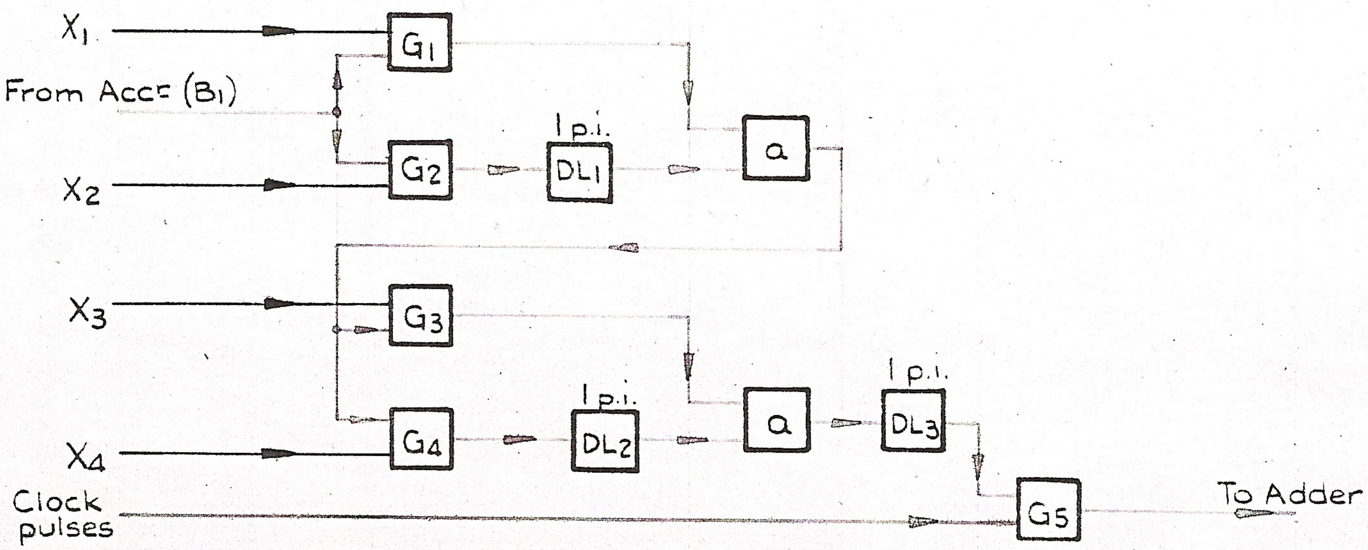


Fig. 9 COMPUTER

(Full lines indicate number pulse trains. Broken lines indicate control signals)



A. S. U. I



A. S. U. II

Fig. 10 ACCUMULATOR SHIFTING UNIT

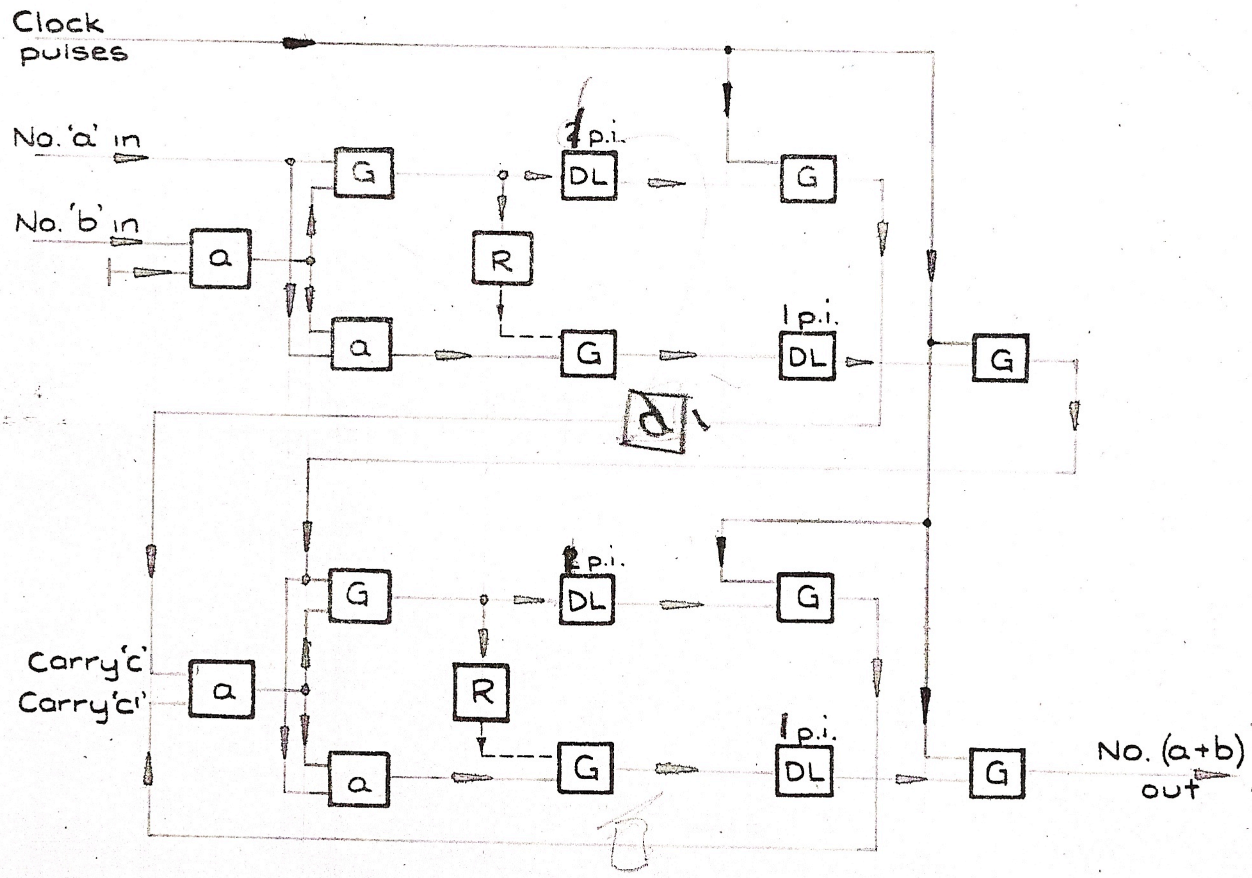

Clock pulses
No. 'a' in
No. 'b' in
G
a
a
2 p.i.
DL
R
G
1 p.i.
DL
G
G
Carry 'c'
Carry 'c''
G
a
a
2 p.i.
DL
R
G
1 p.i.
DL
G
G
No. (a+b) out

Fig. II ADDER

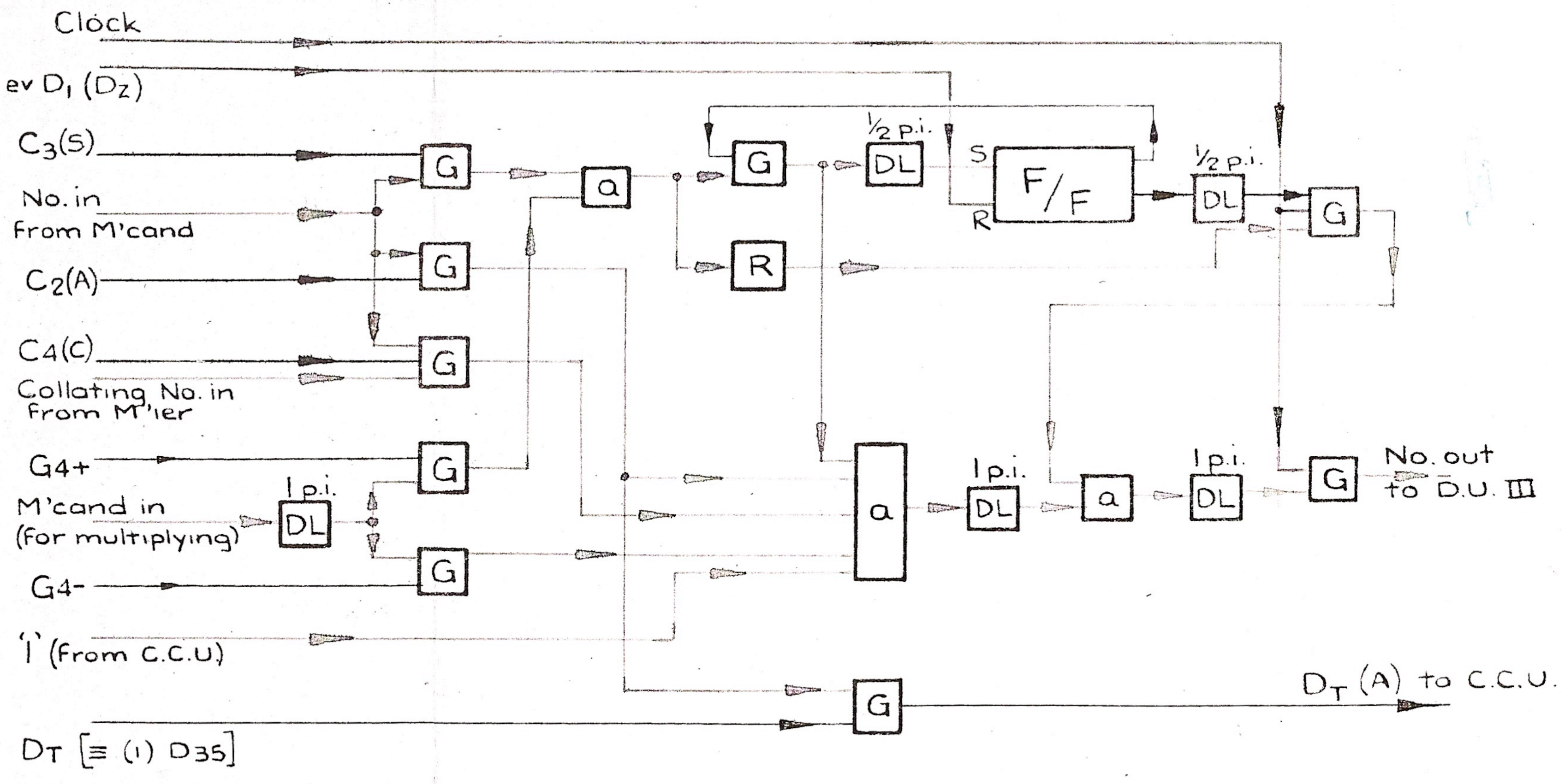


Fig. 12 COMPLEMENTER - COLLATER

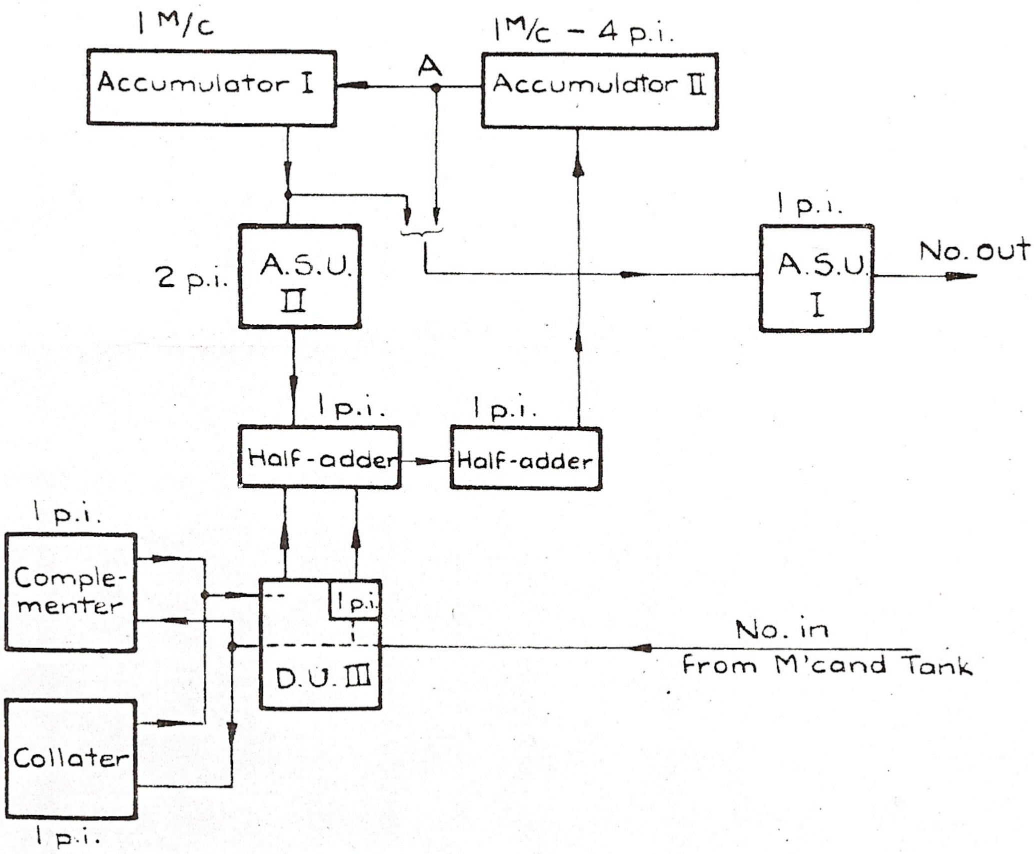


Fig. 13. DELAYS IN COMPUTER

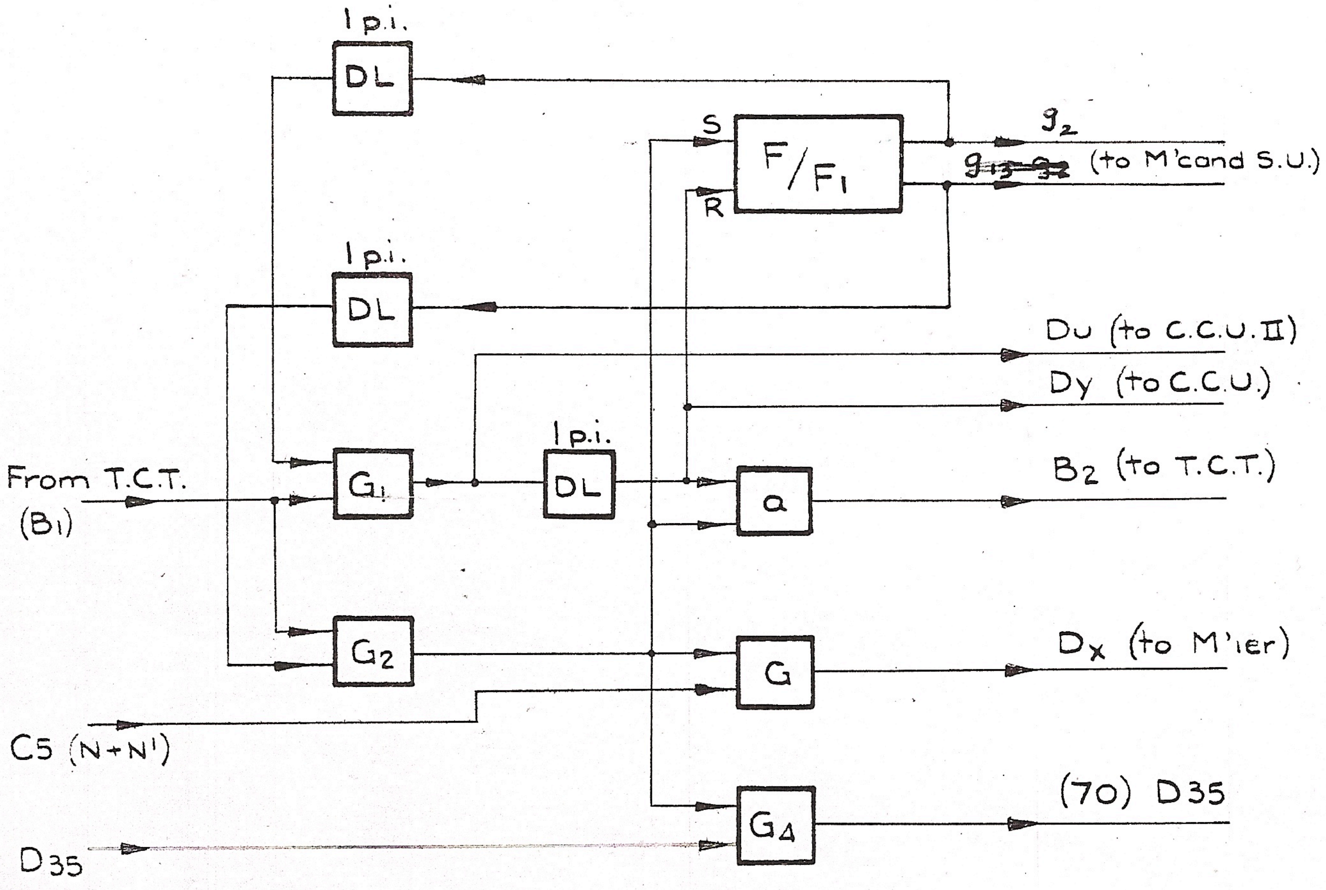
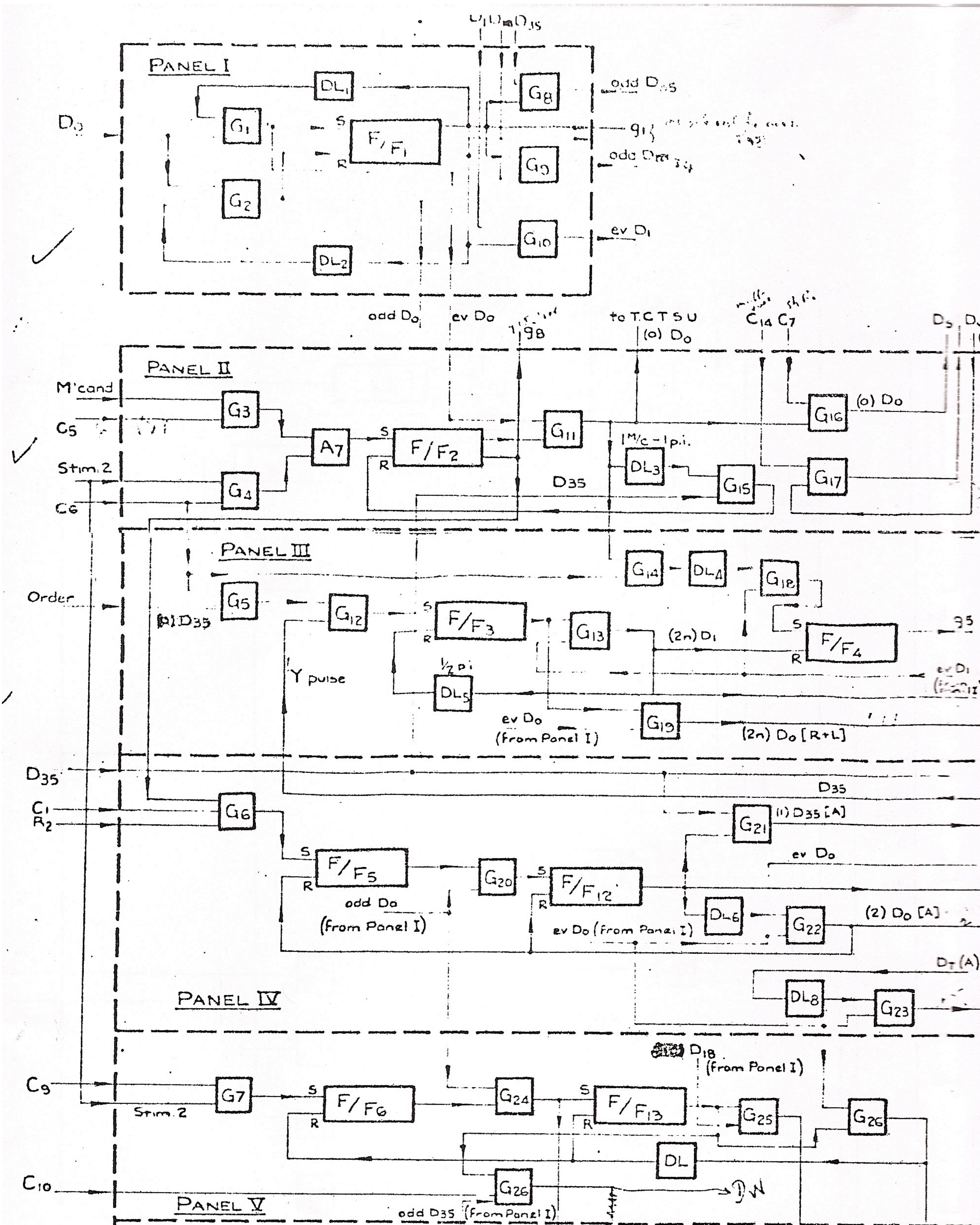
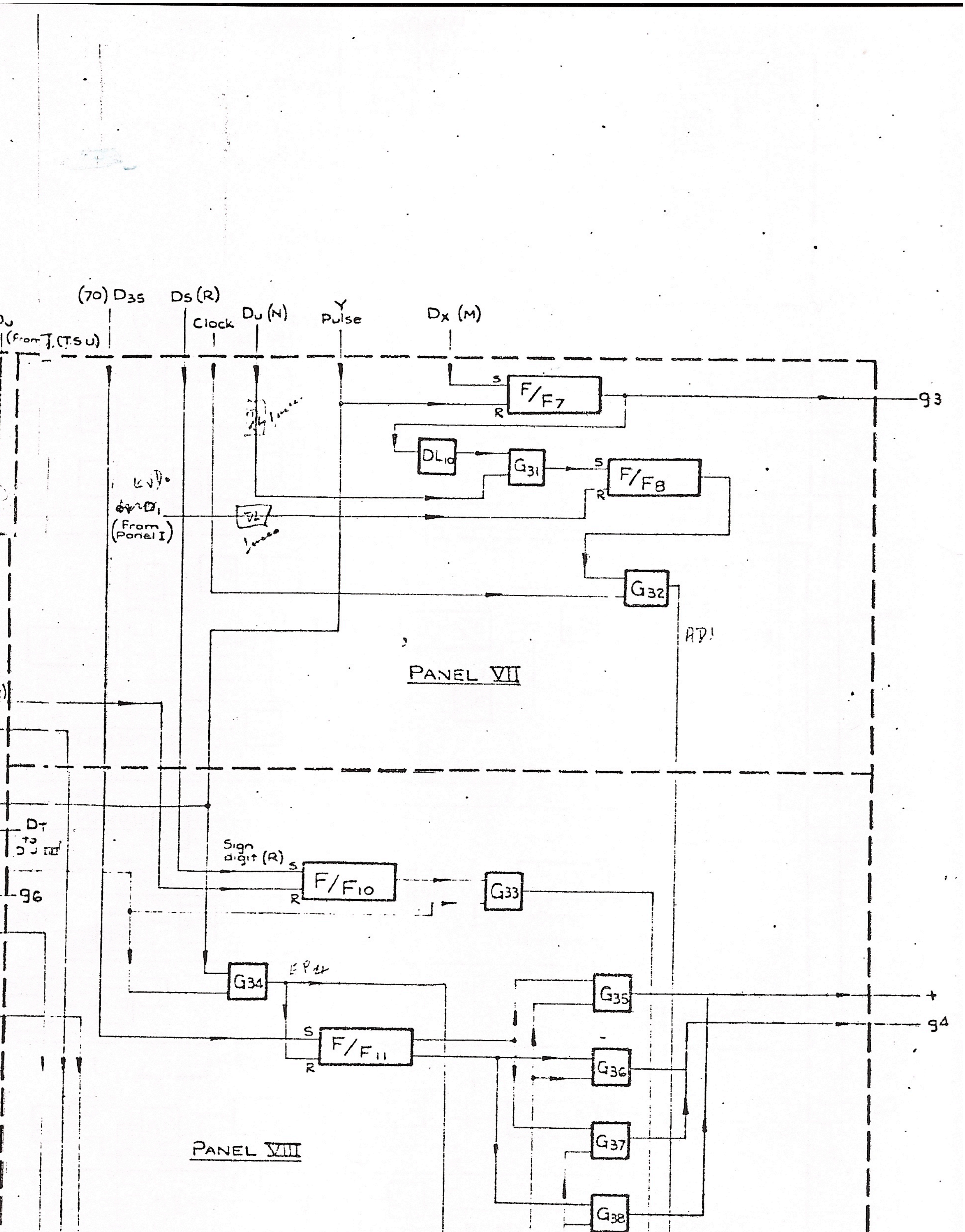


Fig. 14 TIMING CONTROL TANK SHIFTING UNIT


PANEL I
DL1
DL2
G1
G2
G8
G9
G10
F/F1
S
R
odd D35
odd D34
ev D1
odd D0
ev D0
to T.C.T.S.U
(0) D0
C14 C7
PANEL II
M'cand
C5
Stim. 2
C6
G3
G4
A7
F/F2
G11
G15
G16
G17
DL3
1 M/c - 1 p.i.
D35
(0) D0
PANEL III
Order
G5
(1) D35
G12
G13
G14
DL4
G18
F/F3
F/F4
(2n) D1
ev D1
Y pulse
½ p.i
DL5
ev D0
(From Panel I)
G19
(2n) D0 [R+L]
D35
C1
R2
G6
D35
G21
(1) D35 [A]
ev D0
F/F5
G20
F/F12
odd D0
(From Panel I)
ev D0 (From Panel I)
DL6
G22
(2) D0 [A]
D7 (A)
DL8
G23
PANEL IV
D18
(From Panel I)
C9
G7
Stim. 2
F/F6
G24
F/F13
G25
G26
DL
C10
G26
PANEL V
odd D35 (From Panel I)


(70) D35
Ds (R)
Clock
Du (N)
Y
Pulse
Dx (M)
(From J. (T.S.U)
S
R
F/F7
93
DL10
G31
F/F8
(From Panel I)
G32
PANEL VII
Sign digit (R)
F/F10
G33
96
G34
F/F11
G35
G36
G37
G38
+
94
PANEL VIII

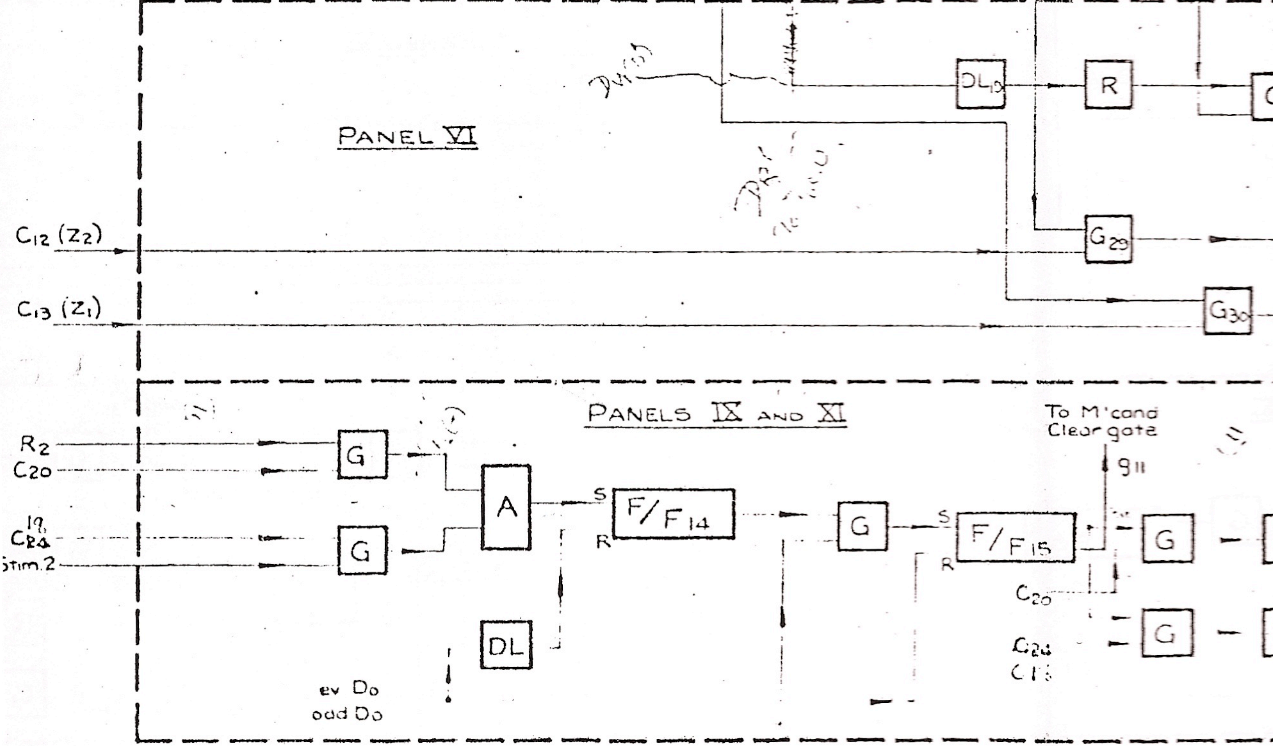
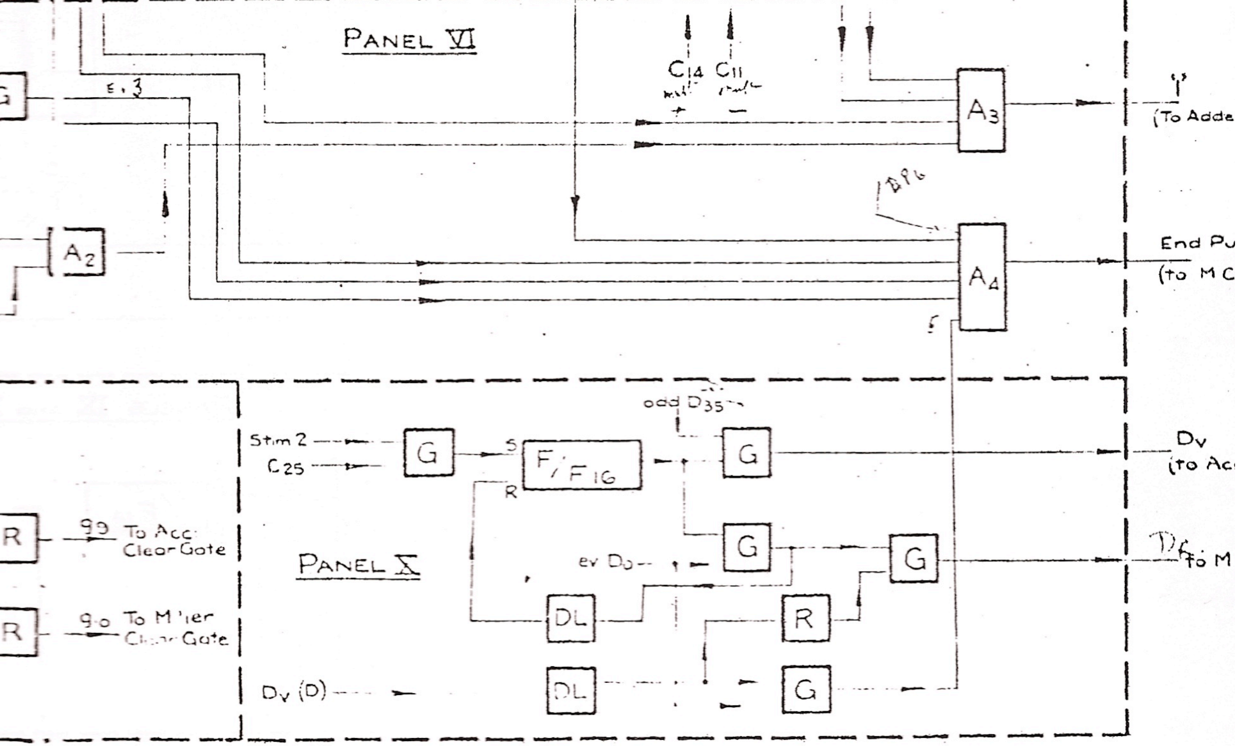


Fig. 15 COMPUTER C


PANEL VI
C14
C11
A3
(To Adde
End Pu
(to M C
A2
A4
Stim 2
C25
S
R
odd D35
Dv
(to Ac
99 To Acc
Clear Gate
9.0 To M'ier
Clear Gate
PANEL X
ev D0
Dv (D)
DL
To M

ONT ROL UNIT