in Memory, a delay of one half M/C is applied in the Transfer Unit. (A delay is as effective as an advance, since the number appears at the input has every M/C and the transfer is effected only when coincidence has been achieved).

The Transfer Unit comprises the Transfer Tank, together with the system of gates shown in Fig. 6, to determine whether the conditions exist which require a half M/C shift in the position of the number. These gates are controlled by the Half-cycle Flashing Unit.

4.46. Decoders, Coder and Flashing Units.

A Decoder consists of a series of diode gates arranged as a binary distribution system. They are provided with cathode followers from which positive gating e.m.fs. are obtained. Negative e.m.fs., where required, are provided by additional cathode followers in the Distributor Units.

The Tank Number Decoder serves to route a coincidence gating e.m.f. to the appropriate tank. It consists of a primary Decoder and eight Secondary Decoders.

The primary Decoder receives the Coincidence e.m.f. and two of the five outputs of the Tank Number Flashing Unit. In addition it receives one output from the Order Coder specifying whether the order involves transfer into or out of Memory. This provides a route for the Coincidence e.m.f. to one of eight possible outputs, which are connected to the eight secondary Decoders. In addition, each of these receives, in parallel, the three remaining outputs from the Flashing Unit, so that of the 64 possible outputs from the Decoder, the coincidence e.m.f. may pass through the one specified. Of these 64 outputs, 32 are connected to input gates

and 32 to output gates of the Memory tanks, via the Distributor Unit, which also provides the negative e.m.fs. for the clear gates.

The Order Decoder differs from the Tank Number Decoder in that:

(a) only 32 outputs are provided

(b) the Coincidence gating e.m.f. is replaced by a fixed e.m.f.

(c) the distributing data are provided by the Order Flashing Unit,

and (d) all the outputs are positive, since no clear gates are used. Thus no Distributing Unit is required.

The Order Coder is simply a series of adding diodes and cathode followers, which convert the Decoder Output to appropriate gating e.m.fs., and thus fulfils certain of the functions of a distributing unit.

The gating e.m.fs. emitted by the Order Coder are designated as follows:

C_1	for orders	A, S, C, N or N'	
C_2	"	"	A
C_3	"	"	S
C_4	"	"	C
C_5	"	"	N or N'
C_6	"	"	R or L
C_7	"	"	R
C_8	"	"	L
C_9	"	"	Z_1, Z_2, D' (conditional transfer with opposite criterion)
C_{10}	"	"	D'
C_{11}	"	"	N'

C_{12}	for	orders	Z_2
C_{13}	"	"	Z_1
C_{14}	"	"	N
C_{15}	"	"	Not specified at present
C_{16}	"	"	I
C_{17}	"	"	T, T' or I
C_{18}	"	"	M
C_{19}	"	"	T or T'
C_{20}	"	"	T
C_{21}	"	"	O
C_{22}	"	"	Z_3
C_{23}	"	"	Not specified at present
C_{24}	"	"	M or C
C_{25}	"	"	D
C_{26}	"	"	A, S, C, N, N' or M
C_{27}	"	"	I or O

Of these, all are positive except C_{27} (which is negative) and C_{16} and C_{17} (which may be either positive or negative).

A Flashing Unit consists of a group of flip-flops, arranged in pairs, each receiving a setting pulse from the Sequence Control (or Order) Tank through a gate which is opened by the appropriate digit pulse. For each such unit, a common resetting line is provided.

4. 5. Computer.

The Computer carries out all arithmetical operations required in the solution of a problem. It comprises separate units for addition, complementing, collating, shifting and multiplying, but these units can not be regarded as completely independent. For example, each number entering the Accumulator does so through the Adder and the Complementer - Collater, even though the corresponding operations are not necessarily performed on it. The sequence of operations in the Computer is supervised by the Computer Control Unit (C.C.U.), which carries out, within the Computer, a function similar to that of the Main Control Unit in the Control Section.

Since the Accumulator contains 2 M/C, and since operations in the Computer may occupy a considerable number of M/C, it is convenient to denote a specific digit pulse by the symbol (m) Dn, where m refers to the particular M/C and n to the pulse position in the M/C.

Thus (1) D_0 indicates pulse D_0 in M/C 1, (odd) D_1 indicates pulse D_1 in every odd M/C, etc.

This convention will be used when dealing with the various pulses and gating e.m.fs. emitted in the Computer.

In describing the operation of the C.C.U., it is desirable to consider first the detailed functions of the components which it controls. The components of the Computer are shown schematically in Fig. 9.

4.51. Accumulator.

The Accumulator is used to accept the result of a computation. It consists of two tanks, known as Accumulator I, of 1 M/C delay, and Accumulator II, of 1 M/C - 4 pulse intervals delay. These tanks, together

with Accumulator Shifting Unit II, the Adder and the Complementer - Collater, form a closed circulating system, the total delay in the electronic components being normally 4 pulse intervals, and the delay in the whole system being 2 M/C. The Accumulator thus has the capacity to store a 67 binary digit number which may result from the multiplication of two long numbers.

4.52. Accumulator Shifting Unit (A.S.U.)

This is in two parts, shown in schematic form in Fig. 10. A.S.U. I, which is used for the extraction of numbers from the Accumulator, serves also to provide gating e.m.fs. X_1, X_2, X_3 and X_4 according to whether an order is present for a right or left shift, this being determined by the input C_7 or C_8 from the Order Coder. The duration of the gate coincides with that of g_5, emitted by the Computer Control Unit.

Since the delay in the Computer is 2 M/C, the number to be extracted, of not more than 1 M/C, may be in either of the two tanks when required, so that the output of both is made available at the output gate. The pulses D_{35}, and D_{17} for a short number, are used to close the output gate at the appropriate time.

A.S.U. II provides the mechanism for the actual shifting operation. In the case of a right shift, the gating e.m.fs. are such that G_2 and G_4 are closed, while G_1 and G_3 are open, so that the number by-passes DL_1 and DL_2 and receives only one pulse interval delay in DL_3. This, together with two pulse intervals delay in the Adder, results in a total circulation time of 2 M/C - 1 pulse interval in the Accumulator network. Conversely, for a left shift, G_2 and G_4 are open, and the number receives an additional delay

of 2 pulse intervals in DL_1 and DL_2, so that the circulation time is 2 M/C + 1 pulse interval. G_5 is used only to provide fresh clock pulses.

4.53. Adder.

The Adder consists of two half-adders, as explained in § 3.41. The complete unit is shown schematically in Fig. 11. The first half-adder has no feed-back, and provides a delay of 1 p.i. in the apparent sum, and 2 p.i. in the carry. The second half-adder introduces a similar delay, so that the output (sum) is delayed by 2 p.i.

The method of operation of the half-adders is self-explanatory.

4.54. Complementer - Collater and Distributing Unit III.

These units are shown schematically in Fig. 12. The Complementer is used for carrying out a subtraction (S) order, but is also required for handling negative numbers in operations such as multiplication.

All numbers coming into the Accumulator do so through the Multiplicand Tank and Distributing Unit III. From this unit, according to the nature of the order, the number goes directly to the Adder, after a delay of 1 p.i., or to the Complementer or Collater. From the Complementer or Collater, it is returned to the Distributing Unit and through it to the Adder.

Since delays occur in the Distributing Unit, Complementer and Collater, it is important to consider the 'phase' of a number passing into the Accumulator. The alternative routes are shown in Fig. 13.

In the closed circulating system consisting of the Accumulator,

Shifting Unit II and Adder, the total delay is made up as follows:

Accumulator I	1 M/C
Accumulator II	1 M/C - 4 p.i.
A.S.U. II	2 p.i.
Adder	2 p.i.

The total is thus exactly 2 M/C, and there is no change of phase in a complete circulation.

However, a number from the Multiplicand Tank loses 1 p.i. in either the Complementer or Collater, or in the Distributing Unit in the case of an A - order, before entering the circulating system, a further 2 p.i. in the Adder before entering the Accumulator, and 1 p.i. in extraction from the Accumulator. In passing through Accumulator II, it is further delayed by 1 M/C - 4 p.i., so that if taken out at the point A between the two Accumulator tanks, the total delay is exactly 1 M/C, and the number, both at this stage and at the output of Accumulator I, is in phase with the incoming number from the Multiplicand Tank. Thus it may be extracted at either of these points.

The Collater itself consists simply of a triple gate, opened by the receipt of a C - order, and admitting every pulse in the incoming number which coincides with a pulse in the collating number from the Multiplier Tank.

4.55. Accumulator Warning Unit.

The Warning Unit is used to stop the Machine and ring an alarm if the Accumulator is overloaded, as shown by inequality of the two sign pulses. In the case of overloading, a pulse passes through a gate system

and sets a flip-flop, which in turn sets a relay to initiate the necessary action.

4.56. Multiplication Units.

The operations of Multiplication and Collation are preceded by an M - order, which causes the transfer of the Multiplier (or Collating number) to the Multiplier Tank, where it is kept in circulation until required. The receipt of an N - order causes the Multiplicand to be transferred from Memory to the Multiplicand Tank, and initiates the appropriate sequence of additions of partial products into the Accumulator. This involves repeated shifting of the Multiplicand, which is achieved by the Multiplicand Shifting Unit, associated with the Timing Control Tank and its Shifting Unit.

The addition of a partial product into the Accumulator takes place only if there is a pulse in the appropriate place in the Multiplier. The sequence of selection and addition takes approximately 2 M/C, so that a shift in the Multiplicand must take place every second M/C.

The master pulses controlling these operations are emitted by the T.C.T.S.U., and are known as D_x and D_y. D_x is the pulse which causes the appropriate digit of the Multiplier to be examined; if it is 1, a pulse D_x (M) is passed to the C.C.U., which emits a gating e.m.f. g_3, admitting the Multiplicand to the Accumulator. D_y is used to reset the C.C.U. in readiness for the next D_x. Thus, D_x and D_y initiate and terminate each transfer, and in order to provide for a shift every second M/C. they occur at the following times:

D_x	D_y
o D_0	1D_1
2D_1	3D_2
4D_2	5D_3
6D_3	7D_4
-	-
-	-
-	-
70D_{35}	72D_0

4.57. Timing Control Tank and Shifting Unit.

The T.C.T. is a tank of 1 M/C delay, through which a single pulse may circulate. It is used, together with the T.C.T.S.U., to provide the alternate delays of 1 M/C and 1 M/C + 1 p.i., required in forming D_x and D_y. The T.C.T.S.U. is shown schematically in Fig. 14. The output pulse from the T.C.T. is passed alternately through G_1 and G_2, these gates being controlled by the output of F/F_1. The pulse through G_1 is delayed by 1 p.i. and forms the D_y pulse which is sent to the C.C.U. The pulse through G_2, without further delay, goes to the Multiplier Tank as a D_x pulse, provided an N- or N'- order is present. Both pulses are also fed back to the T.C.T. for circulation.

The gate G_4, opened at each D_{35} pulse, admits the only D_x pulse appearing in this position, namely 70 D_{35}.

F/F_1 also provides the gating e.m.f. g_2 for the Multiplicand Shifting Unit.

4.58. Computer Control Unit.

The C.C.U. supervises the operation of the Computer components described above. It is shown schematically in Fig. 15, and is divided into a number of panels.

The control of operations in the Computer depends on the emission of various pulses or gating e.m.fs., the more important being as follows:

Gating e.m.fs.

Designation	Produced in	Purpose
g_1	C.C.U(I)	M/C gate for output from Accumulators I and II
g_2	T.C.T.S.U.	Multiplicand and Shifting Gate
g_3	C.C.U. (VII)	Multiplicand output
g_4	C.C.U. (VIII)	Complementer gate
g_5	C.C.U. (III)	Accumulator shifting gate
g_6	C.C.U. (IV)	Multiplicand shift for A.S.C. orders
g_7	Accumulator Warning Unit	Warning gate
g_8	C.C.U. (II)	T.C.T. clear gate
g_9	C.C.U.(IX & XI)	Accumulator clear gate
g_{10}	do.	Multiplier " "
g_{11}	do.	Multiplicand " "
g_{12}	M.C.U.	Stage I of main control
g_{13}	do.	Stage II of main control

Pulses.

D_V = sign questioning pulse for D- order. $D_v(D)$ = return pulse if neg.

D_n " " " " N- order. $D_n(N)$ " " " "

D_R " " " " R- order. $D_R(R)$ " " " "

D_P " " " " A- order. $D_P(A)$ " " " "

D_W " " " " D'-order* $D_W(D^1)$ " " " "

D_X digit " " " Multiplier $D_X(M)$ " " " '1'

D_y resetting pulse after addition of partial product

D_z suppression pulse, occurring at ev. D_0.

S_1, S_2, R_1, R_2 = stimulating and resetting pulses in main control sequence.

Gate and Pulse Emission - Panel I.

Since a number in the Accumulator may occur in either of the 2 M/C, it is necessary to have two sets (g_1) of gating e.m.fs., one for the odd M/C and one for the even. These are provided by F/F_1, which is alternately set and reset by successive D_0 pulses, by means of G_1 and G_2. In addition to providing g_1, panel I also selects the following pulses, which are required in various operations:

even D_0 from G_1

odd D_0 from G_2

even D_1 from G_{10}

odd D_{35} from G_8

odd D_{18} from G_9

---

* D'- order is D - order with opposite criterion for transfer.

Multiplication - Panels II, VII and VIII.

These panels deal with the initiation of a multiplication, when the Multiplier is already present. In the presence of an N or N' (C_5) order, the first digit of the arriving multiplicand sets F/F_2, which allows the next even D_0, (oD_0), from section I, to pass to the T.C.T.S.U. and elsewhere, as a start pulse for the whole operation. This pulse, delayed by 1 M/C - 1 p.i. in the phantastron DL_3, lets the next D_{35} through G_{15} to reset F/F_2. In the presence of an N - order (C_{14}), the sign questioning pulse D_4, from the T.C.T.S.U. passes G_{17} and goes to the Multiplier Tank. If the Multiplier is negative, the return pulse $D_4(N)$ sets F/F_8, permitting the gate G_{32} to admit a succession of 1's to the Accumulator, until F/F_8 is reset by even D_1.

The return pulse $D_x(M)$ from the multplier (if the appropriate digit is 1) sets F/F_7 which emits g_3, to allow the Multiplicand to pass to the Accumulator. F/F_7 is reset by the next D_y. F/F_8, which is used to provide the gating e.m.f. for G_{32}, is reset by the next even D_1.

This process is repeated until the end of the 70th M/C, irrespective of whether the numbers concerned are long or short.

The pulse 70 D_{35} sets F/F_{11}, which ensures that the partial product resulting from the sign digit, passes to the Complementer instead of the Adder. Thus this product is subtracted if the Multiplier is negative, while the partial product is 0 if the Multiplier is positive, and therefore makes no contribution.

The combination of gates, G_{35} to 38, provides for the complementary operations to take place in the case of a N'-, rather than a N - order.

It should be noted that the operation of Panel II does not commence until the arrival of a pulse in the Multiplicand. If the Multiplicand is zero, a fictitious addition of 0 is carried out, to admit R_2 through G_6 as an end pulse.

Shifting - Panels II and III.

In the case of a shift order, L or R, the numerical part is coded, not in binary form, but by the position of a single pulse in the train 0_1 to 0_{10}.

The process is initiated by a stimulating pulse from the M.C.U., which sets F/F_2 and allows the first ev D_0 to pass as o D_0 to the T.C.T. In the case of a right shift, the next D_0-pulse, passing through G_{16}, is used as D_8, to examine the sign digit in the Accumulator. If negative, the return pulse D_8 (R) provides for the addition of complementary 1's just as in multiplication. In this case, however, only one complementary digit is added, since shifting occurs only by one digit at a time. This is done through F/F_{10} and G_{33}.

The pulse (o)D_0 also goes to G_{14} and is delayed 1 p.i. in D_4, becoming (o)D_1, which sets F/F_4. This provides a gating e.m.f. g_5 which goes to the Accumulator Shifting Unit.

The shift then carries on, one place at a time, until coincidence is reached in G_{12} between the order position pulse and D_y. At this stage, F/F_3 is set, allowing the next ev D_1 through to reset F/F_4 and F/F_{10}. F/F_3 is also reset after a delay of $\frac{1}{2}$ p.i., after allowing the next ev D_0 through as an end pulse.

Addition, Subtraction, Collation - Panel IV.

The gating e.m.f. G_1, appears for any of the orders N, N', A, S, C. The sequence is initiated by an R_2 pulse from the M. C. U., which sets F/F_5. Addition always commences immediately after odd D_o, and the addend always goes to the Accumulator via the Multiplicand Tank. F/F_5 opens G_{20} to admit the first odd D_o, which sets F/F_{12}. This produces the e.m.f. g6, which provides for the transfer of the number in the Multiplicand Tank to the Accumulator, via Distributing Unit III and, if the order is S or C, via the Complementer or Collater. In the case of a C- order, g6 also admits the collating number in the Multiplier Tank to the Collater.

F/F_{12} is reset by the next ev D_o, which also goes out as an end pulse.

When adding a negative number into the Accumulator, it is necessary to add the additional sign pulse. To do this, G_{21} allows the next D_{35} to pass as pulse D_T, which explores the sign of the number in the Multiplicand Tank. If this is negative, the return Pulse D_T (A), delayed by 1 p.i. in DL_8, allows the next ev D_o to pass G_{23} and so to be added into the Accumulator.

Rounding-off Orders - Panels V and VI.

The input G_9 appears for either a Z_1 or Z_2 order. This allows the stimulating pulse S_2 from the M. C. U. to pass through G_7 and set F/F_6, which in turn allows the next odd D_o to pass G_{24}. This sets F/F_{13} and also passes through G_{30} when C_{13} (Z_1 order) is present.

The positive output from F/F_{13} allows the next D_{18}, which must be odd, to go to an adding diode through G_{29} if C_{12} (Z_2 order) is present.

The output adds 1 in the appropriate position in the Accumulator, thus completing the rounding-off order. F/F_{13} also allows the next ev D_0 to pass as an end pulse, and resets itself and F/F_6.

The Z-order does not include the transfer to Memory of significant figures, which must be done by a transfer order.

Clearing Computer Tanks - Panel IX.

The Accumulator, Multiplier and Multiplicand tanks are not automatically cleared by new inputs as in the case of Memory tanks. Provision has therefore to be made to clear them at the appropriate times.

For a transfer order, C_{20} appears and allows the R_2 pulse to set F/F_{14}, which permits the next odd D_0 to set F/F_{15}. The negative output goes to the Multiplicand clear gate, while the positive output, gated by C_{20}, is reversed and goes to the Accumulator clear gate.

In the presence of an M-order, C_{24} appears and causes the Multiplier tank also to be cleared.

C_{24}, which appears in the presence of a C, A, S, N, N' or M Order, allows the stimulating pulse S_2 to pass to F/F_{14}. F/F_{15} provides a gating e.m.f. which allows the next ev D_0 to reset F/F_{14} and F/F_{15}.

Conditional Transfer - Panel X.

The e.m.f. C_{25}, in the presence of a D-order, allows the next odd D_{35} to pass as the investigating pulse, D_v, to the Accumulator. It also allows the following pulse, ev D_0, to reset F/F_{16} and also to pass through a normally open gate to the M. C. U. If the number in the Accumulator is negative, a $D_v(D)$ pulse appears (at D_{35}) and, after a delay of 1 p.i. and

reversal, closes the normally open gate G_2, so that the M.C.U. does not receive a pulse. The delayed pulse, however, is gated with ev D_0 to provide an end pulse, so that the machine will carry on with its normal sequence.

Warnings.

Provision is made in the C.C.U. for appropriate action to be taken in the case of a Z_3-order, or of a warning from the Accumulator Warning Unit if the Accumulator is overloaded.

4.6. Output.

The operation of the Output, on receipt of an O-order, is very similar to that of the Input. Coincidence is found and the four digits specified in the order are transferred to flashing units which set relays. A '1' is then added to the S.C.T., and the machine carries on with its sequence, the data in the relays being transferred meanwhile to a standard teleprinter output mechanism, either as punched tape, or in printed tabular form, as required. This transfer is achieved by a set of solenoids, which set up the fingers of the teleprinter mechanism in accordance with the data on the relays.

Inhibition of the next O-order, if it overlaps the O-order being executed, is provided as in the Input. As soon as the mechanism is set up for printing, the relays and flashing units are reset, and the inhibition removed.

Printing takes place on receipt of the next O-order, and it is therefore necessary to provide an additional arbitrary O-order when programming. Printing orders, coded in accordance with teleprinter practice,

appear as O-orders in Memory, and must also be taken into account when programming.

4.7. Pulse Generators and Power Supplies.

Clock and digit pulses are required in various parts of the machine, and are provided by units which cannot logically be included in any of the sections of the machine already described.

The clock pulse generator consists of a basic oscillator with a frequency of approximately 500 Kc/s., the output of which is squared and thus formed into clock pulses. The output is scaled down twice by a factor of 6 in phantastron circuits, providing a minor cycle gating e.m.f. It is proposed to replace the existing oscillator by another whose frequency will be controlled by a mercury delay line, for reasons given in § 3.1.

The digit pulse generator accepts the M/C gating e.m.f. from the clock pulse generator, and produces pulse D_{17}, together with a gating e.m.f. for D_{18}. This, in turn, is used to produce a D_{18} pulse, and a gating e.m.f. for D_{19}, and so on. Cathode followers are provided for each output.

The machine, as planned at present, will contain some 3000 or more valves, including diodes, and will require a H.T. supply at 250 V. with a capacity of 12 - 15 amps. The heater load will be approximately 6 K.W. The degree of stabilisation required has yet to be determined.