AMULET2e

32-bit Integrated Asynchronous Microprocessor

Features

- Compatible with ARM instruction set
- On-chip 4Kbyte memory, configurable as cache or RAM
- Direct interface to static and dynamic memory devices.
- Low power sleep mode.
- Dynamic external bus sizing.
- 128 pin Plastic Quad Flat Package
- 0.5 micron CMOS, 3 layer metal process
- 3.3V supply voltage

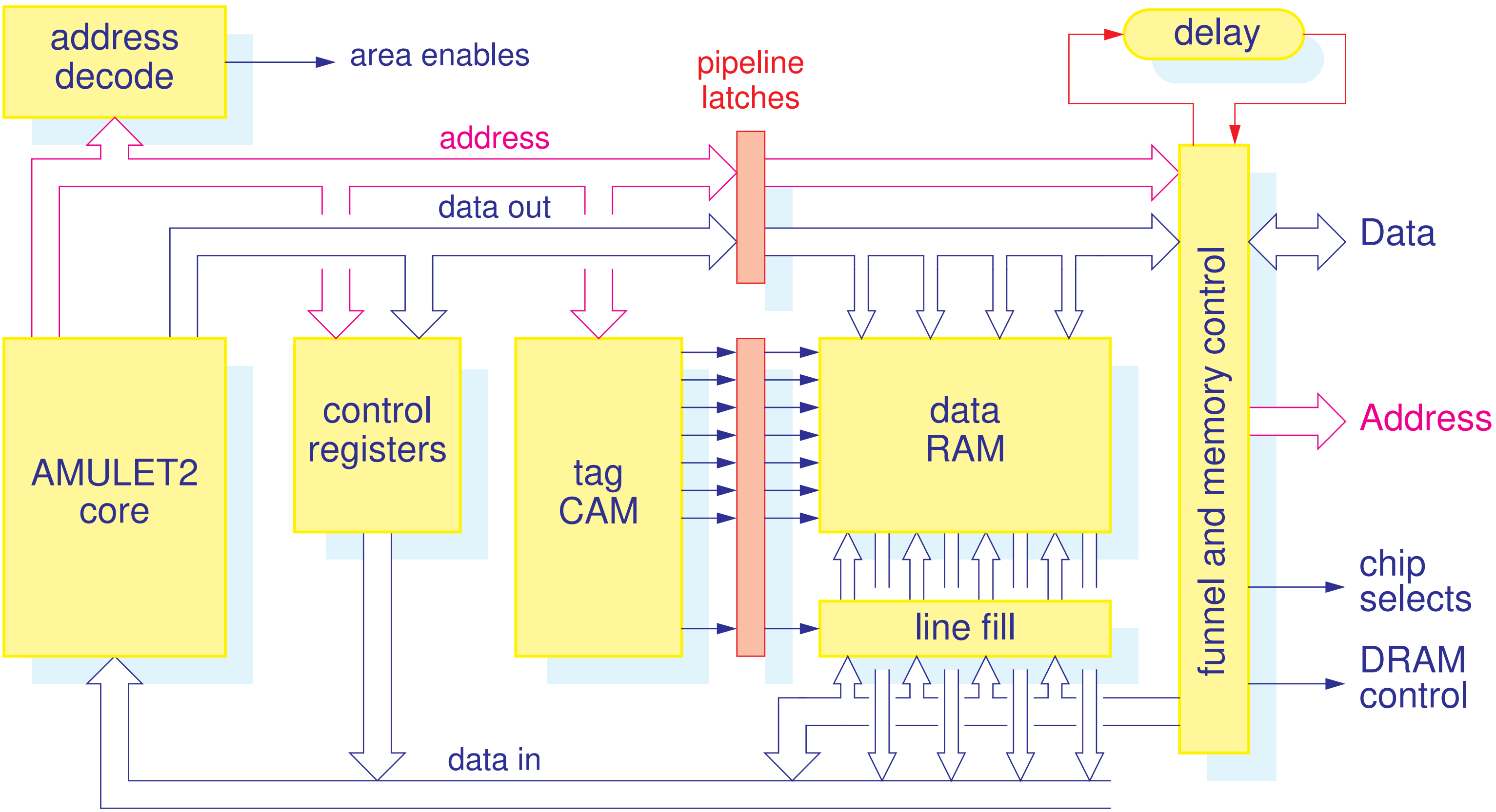
Introduction

AMULET2e is an integrated asynchronous microprocessor based around AMULET2; a 32-bit asynchronous microprocessor, compatible with the ARM instruction set. AMULET2e was designed to be suitable for embedded applications and hence the memory interface is as simple as possible so that the number of support devices can be minimised. To reduce system cost further, the ability to reduce the width of the data bus is provided. This allows one or two byte wide memory devices to be used instead of the four usually required to match a 32 bit data bus.

In addition to the AMULET2 processor, AMULET2e contain 4K bytes of static memory which can be configured as memory-mapped RAM or as a cache. It also contains memory interface logic which allows it to directly interface to a wide variety of memory and peripheral devices. The memory interface is directly configurable by the processor. Static memory devices, such as SRAM, EPROM and peripheral chips, can be directly connected to the processor with no extra logic. In addition, DRAM is supported, again with no external support logic.

The device also contains a crystal oscillator circuit and divider chain which may be used to maintain accurate timing information.

AMULET2e Block Diagram



External Interface

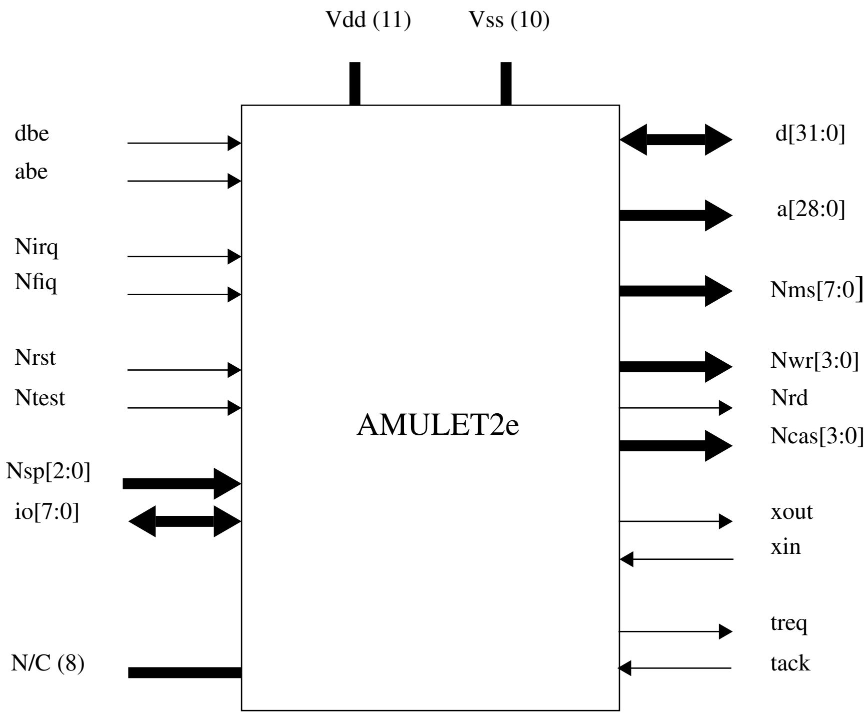


Table 1: Pin descriptions

Signal	Pins	Type	Function
a[28:0]	29	OZ	Address bus, used to address memory devices.
d[31:0]	32	IOZ	Bidirectional data bus, used to transfer data to/from memory devices. Also used to read pre-configuration data on d[7:0].
Nwr[3:0]	4	OZ	Write strobes, active low, one per byte, used to write data into memory devices.
Nrd	1	OZ	Read enable, active low, used to enable data from memory devices.
Nms[7:0]	8	OZ	Memory selects, configurable, active low, used as chip select or RAS for DRAM memory
Ncas[3:0]	4	OZ	Column address strobes (CAS), one per byte, for DRAM.
treq	1	O	Timing delay out, 2-phase. A transition is produced at this pin which is delayed externally and fed back to **tack**. Each memory cycle takes a fixed number of **treq/tack** cycles.
tack	1	I	Timing delay in, 2-phase. External logic delays the transition on **treq** and feeds it back to **tack**.

Table 1: Pin descriptions

Signal	Pins	Type	Function
xin	1	I	Crystal oscillator input.
xout	1	O	Crystal oscillator output.
Nirq	1	I	Interrupt, active low.
Nfiq	1	I	Fast interrupt, active low.
Nrst	1	I	Reset, active low.
Ntest	1	I	Test mode. High for normal operation, low for test mode.
abe	1	I	Active high enable for tri-state outputs **a[28:0]**, **Nms[7:0]**, **Nwr[3:0]**, **Nrd**, **Ncas[3:0]**. Tied high for normal operation.
dbe	1	I	Active high enable for **d[31:0]** outputs. Tied high for normal operation.
io[7:0]	8	IOZ	Input/output port
Nsp[2:0]	3	IOZ	I/O special function select pins
Vdd	11	P	+ve power supply.
Vss	10	P	-ve power supply.

Memory Map

The 32 bit (4 Gb) address space is divided into 8 equally sized regions of 0.5Gb (Region 0 to Region 7). Associated with each region is a memory select pin (**Nms[7:0]**), which is active when the region is being addressed. Each region is associated with a particular type of memory and various timing and other parameters can be configured for each region using on-chip control registers.

The area of memory from 0xffffff00 to 0xffffffff contains control registers which control how the chip operates. These mask external memory at the same address. The memory map is shown below.

Table 2: Memory Map

Start Address	End Address	Region
0x00000000	0x1fffffff	0
0x20000000	0x3fffffff	1
0x40000000	0x5fffffff	2
0x60000000	0x7fffffff	3
0x80000000	0x9fffffff	4
0xa0000000	0xbfffffff	5
0xc0000000	0xdfffffff	6
0xe0000000	0xfffffeff	7

Table 2: Memory Map

Start Address	End Address	Region
0xffffff00	0xffffffff	Control registers

Memory Timing

All external memory timing is based on an externally defined delay. During memory accesses, the chip produces a transition on the delay-out pin (**treq**). External logic delays this transition and then feeds it back to the delay-in pin (**tack**). All memory timing is based on this basic timing unit (Dt). Each region has timing information which indicates the number of times this delay will be applied in the access cycle.

The delay can be provided by an RC delay in low cost systems or by a delay line where more closely controlled timing is required.

Action on reset

The chip is reset by taking the **Nrst** pin low. This resets the AMULET2 processor and flushes the cache (however, the contents of the on-chip RAM will be preserved). In addition, all control registers are set to predefined values. These values are shown below the register disgrams in the descriptions which follow.

When the **Nrst** pin goes high the chip reads a single byte of data (the pre-configuration byte or PCB) by performing a single read cycle on **d[7:0]** using **Nms[0]** with the slowest possible memory timing (see later). This byte describes the endianism and width of the memory device attached to **Nms[0]** as well as certain configuration options for the AMULET2 processor. The address used to fetch the byte is 0x14, which is an unused exception vector.

The PCB has the following format. The width field is copied into the RAR0 control register. The Endianism, Nabt and BTBon bits are copied into the CCR. See below for descriptions of these registers.

reserved	reserved	reserved	BTBon	Endianism	Nabt	Region0 width

After the pre-configuration byte has been read, the reset signal to the AMULET2 processor is released and this then begins fetching code from address 0. Initially, this will be the memory device selected by **Nms[0]** which will usually be a ROM. All memory accesses will be done with the slowest possible memory timing and one of the first things that the application code will normally do is to program the control registers to suit the memory devices in the system.

Region Swap Mechanism

The region swap mechanism allows a region other that Region 0 to be ‘swapped’ with Region 0. This allows the system to boot from ROM and then to move another block of memory (eg RAM) into Region 0 either for faster access to the exception vectors or to make them writable. This is achieved by connecting the bootstrap ROM to the Region 0 select pins (**Nms[0]**) and the RAM to another select pin, such as **Nms[6]**. The application code then designates Region 6 as the *swap region* by writing to a control register (see below) and then when the processor performs a read access anywhere within Region 6 the swap occurs. From this point on (including the access which caused the swap), accesses to Region 6 cause **Nms[0]** to be asserted and accesses to Region 0 cause **Nms[6]** to be asserted. Note that this mechanism can only be used once between resets.

Control registers

AMULET2e contains a number of control registers which are mapped into the address space between 0xffffff00 and 0xffffffff. These are mostly 8 bits wide with the exception of the Timer and its associated Compare Register which are 16 bits wide. The registers appear in the bottom byte(s) of the word when a word access is used to read or write them. On reading, the upper 3 bytes (or 2 for Timer and Compare Registers) will be undefined.

Table 3: Control Registers

Address	Type	Register
0xfffffff4	R/W	RAR7 - region7 architecture
0xfffffff0	R/W	RTR7 - region7 timing
0xffffffe4	R/W	RAR6 - region6 architecture
0xffffffe0	R/W	RTR6 - region 6 timing
0xffffffd4	R/W	RAR5 - region5 architecture
0xffffffd4	R/W	RTR5 - region 5 timing
0xffffffc4	R/W	RAR4 - region4 architecture
0xffffffc0	R/W	RTR4 - region4 timing
0xffffffb4	R/W	RAR3 - region3 architecture
0xffffffb0	R/W	RTR3 - region3 timing
0xffffffa4	R/W	RAR2 - region2 architecture
0xffffffa0	R/W	RTR2 - region2 timing
0xffffff94	R/W	RAR1 - region1 architecture
0xffffff90	R/W	RTR1 - region1 timing
0xffffff84	R/W	RAR0 - region0 architecture
0xffffff80	R/W	RTR0 - region0 timing
0xffffff54	R/W	PDR - i/o port data register
0xffffff50	R/W	PCR - i/o port control register
0xffffff4c	R/W	CCR - macrocell control register
0xffffff48	R/W	TCR - timer control register
0xffffff44	R/W	RCR - on-chip RAM control register
0xffffff40	R/W	MCR - misc control register
0xffffff04	R/W	CPR - compare register (16 bits)
0xffffff00	Read only	TMR - timer register (16 bits)

Region timing register

There is one instance of this register for each region and it controls the memory timing for the region. Sample timing diagrams are given in a later section.

RTR	spare	DRAM	sync	setup	hold	slow	timing/DRAM type	
RTR0	X	0	1	1	1	1	1	1
RTR1-7	X	0	0	0	0	0	0	0

If the DRAM bit (D6) is set it indicates the region contains DRAM memory. In this case the type bits (D1,D0) give the number of address lines on the DRAMs as shown in the table below. Bits 5 through 2 should be zero if the DRAM bit is set. The largest DRAM that can be attached is 16Mbit and the smallest is 256Kbit.

Table 4: DRAM address size

D1	D0	DRAM Type
0	0	9 bit address
0	1	10 bit address
1	0	11 bit address
1	1	12 bit address

If the DRAM bit is zero, the memory is assumed to be static and the Slow (D2) and Timing (D1-D0) fields encode the timing as follows. Note that the Slow bit simply multiplies the number of time periods by 4. Read cycles use the timings from the table below. Write cycles always add an extra **treq/tack** delay at the beginning of the memory access. During this time, the write strobes (**Nwr[3:0]**) go high while the address is changing to prevent accidental writes to unintended addresses. The Setup bit (D4) is used to add setup time to static memory cycles. For fast cycles

Table 5: Static RAM timings

D2	D1	D0	Multiple	Dt=10nS	Dt=25nS	Dt=50nS
0	0	0	1	10	25	50
0	0	1	2	20	50	100
0	1	0	3	30	75	150
0	1	1	4	40	100	200
1	0	0	4	40	100	200
1	0	1	8	80	200	400
1	1	0	12	120	300	600
1	1	1	16	240	600	1200

(D2=0) a single Dt is added at the start of the cycle. For slow cycles (D2=1), four Dt delays are added. The Hold bit (D3) performs a similar function at the end of the cycle.

The Sync bit (D5) is used to specify that **treq** should return to a known state (high) before the memory cycle occurs. This allows simple external logic to be clocked off **treq**.

Region Architecture Register

There is a copy of this register corresponding to each region and it controls various memory parameters associated with the region.

RAR	Spare	Spare	Width		Cacheable	Protection		
RAR0	X	X	PCB[1]	PCB[0]	0	1	0	0
RAR1-6	X	X	0	0	0	0	0	0
RAR7	X	X	0	0	0	1	0	0

The Cacheable bit (D3) indicates if this region is eligible for placement in the cache. If it is set, the region's memory will be cached if the on-chip cache is enabled.

The Width field indicates the size of the data bus of the memory in this region. This can be 8, 16 or 32 bits. Where a word transfer is required and the region width is less than 32, the memory interface will perform 2 or 4 memory accesses to transfer a word. The bits have the following format.

Table 6: Memory Width Encoding

D5	D4	Width
0	0	8 bit
0	1	16 bit
1	0	32 bit
1	1	reserved

The protection field (D2-D0) specifies what type of accesses are allowed on the region as follows -

Table 7: Memory Protection Encoding

D2	D1	D0	Supervisor	User
0	0	0	None	None
0	0	1	(reserved)	
0	1	0	Read Only	None
0	1	1	Read Only	Read Only
1	0	0	Read/Write	None
1	0	1	Read/Write	Read Only
1	1	0	Read/Write	Read/Write
1	1	1	(reserved)	

Note that the protection mode for the control registers is specified by the protection mode for Region 7. Thus any external memory devices in Region 7 should require the same protection that the application uses for the registers.

When a memory protection violation occurs, an abort is signalled to the processor which will normally cause an exception routine to be called. If the aborting cycle was a write, the write is supressed.

On-chip RAM Control Register

This register controls the behaviour of the 4KB of on-chip memory. This may be configured either as normal RAM mapped into one of a number of fixed places in the memory map or as a cache.

RCR	Spare	Spare	Spare	RAM Control		RAM Region		
	X	X	X	0	0	0	0	0

The RAM Control bits determine the behaviour of the RAM as follows -

Table 8: RAM Control Bit Encoding

D4	D3	Function
0	0	RAM disabled
0	1	RAM memory mapped at RegionN + 0
1	0	RAM memory mapped at RegionN + 0x8000
1	1	RAM enabled as cache

The RAM Region bits determine which of the regions the on-chip RAM is mapped into when it is in the memory-mapped mode. In this mode the on-chip RAM overlays any off-chip memory at the same address.

When the memory is configured as cache, each region is marked as cacheable or not by a bit in the appropriate RAR. The cache is flushed by any write to the RAM Control Register (RCR). It is also flushed and disabled on chip reset.

The contents of the RAM are preserved across resets but any cache mappings are lost so this behaviour is only likely to be of use if the RAM is memory-mapped.

Timer Control Register

This register controls the operation of the timer which is a binary counter clocked by the **xin** pin.

TCR	Spare	Spare	Spare	Spare	FIQ on	IRQ on	Timer enable	Timer compare
	X	X	X	X	0	0	0	0

The Timer Enable bit (D1) enables the timer. The timer is cleared and disabled when this bit is zero and counts up when it is one. The IRQ and FIQ bits (D2, D3) determine which interrupt will be generated when the Timer register matches the Compare register.

The Timer Compare bit (D0) is read-only and set when the Timer and Compare registers are equal. It is cleared by reading the TCR.

Miscellaneous Control Register

This register controls the region swap mechanism and also DRAM refresh.

MCR	Spare	Spare	Swap Region			Refresh Prescale		
	X	X	0	0	0	0	0	0

The Refresh Prescale bits (D2-D0) define the refresh frequency as a function of the frequency at the **xin** pin as follows -

(NOTE: the *Xin * 2* case means that a refresh occurs on both rising and falling edges of the **xin** pin.)

Table 9: Refresh Control Encoding

D2	D1	D0	Refresh rate
0	0	0	Refresh disabled
0	0	1	xin * 2
0	1	0	xin
0	1	1	xin / 2
1	0	0	xin / 4
1	0	1	xin / 8
1	1	0	xin / 16
1	1	1	xin / 32

The Swap Region defines the region of memory which will be swapped with Region 0. Note that Region 0 is not valid in this context and so this field is initialised to zero when the chip is reset.

I/O Port Registers

These registers control the 8 bit I/O port pins **io[7:0]**. There is a control register (PCR) and a data register (PDR).

PCR/ PDR	io[7]	io[6]	io[5]	io[4]	io[3]	io[2]	io[1]	io[0]
	0	0	0	0	0	0	0	0

When a bit in the control register is one, the corresponding bit in the I/O port is an output, otherwise it is an input. Outputs are controlled by writing the appropriate data bit in the data register and inputs are reflected in the PDR when it is read. Bits which are configured as inputs still have an output latch which is affected by writes to the PDR. These bits would then be reflected in the I/O port if the PCR was changed to make that bit an output.

The special function pins **Nsp[2:0]** are used to modify the behaviour of **io[7:5]** respectively. When a special function pin is high, the corresponding I/O pin behaves as described above. When the special function pin is low, the corresponding I/O pin is configured to be an active-low interrupt input driving the internal IRQ interrupt line. In this case, the corresponding bit in the Port Control Register acts as an enable for the interrupt - a one enables the interrupt and a zero disables it.

Core Control Register

This register controls the configuration of the AMULET2 processor. Some bits (D2-D0) are initialised from the pre-configuration byte (PCB) which is loaded when the chip is reset and should not normally be changed under program control

CCR	Spare	LDRlr Enable	ALUlr Enable	HALT Enable	BTB Flush	BTB Enable	BigEnd	Nabt
	X	0	0	0	0	PCB[4]	PCB[3]	PCB[2]

The Nabt bit (D0) is set to disable the processors abort mechanism. This overrides all of the protection bits so that aborts can never occur and this can improve performance in systems which do not require any memory protection.

The BigEnd bit (D1) determines the Endianness of the processor. It is high for Big Endian operation.

The BTB Enable bit (D2) enables the Branch Target Buffer (BTB).

The BTB Flush bit (D3) enables flushing of the BTB when a SWI instruction is executed.

The Halt Enable bit (D4) allows the processor to halt when a branch instruction which branches to itself is executed.

The ALUlr Enable bit (D5) enables the last result re-use mechanism for operands from the ALU.

The LDRlr Enable bit (D6) enables the last result re-use mechanism for operands from memory.

Timer and Compare Registers

The Timer (TMR) is a 16 bit binary counter incremented by both rising and falling transitions of the **xin** pin. It may be turned on and off by a bit in the timer control register (TCR). The timer is set to zero by reset and whenever it is disabled. It may not be altered by the processor other than as already described.

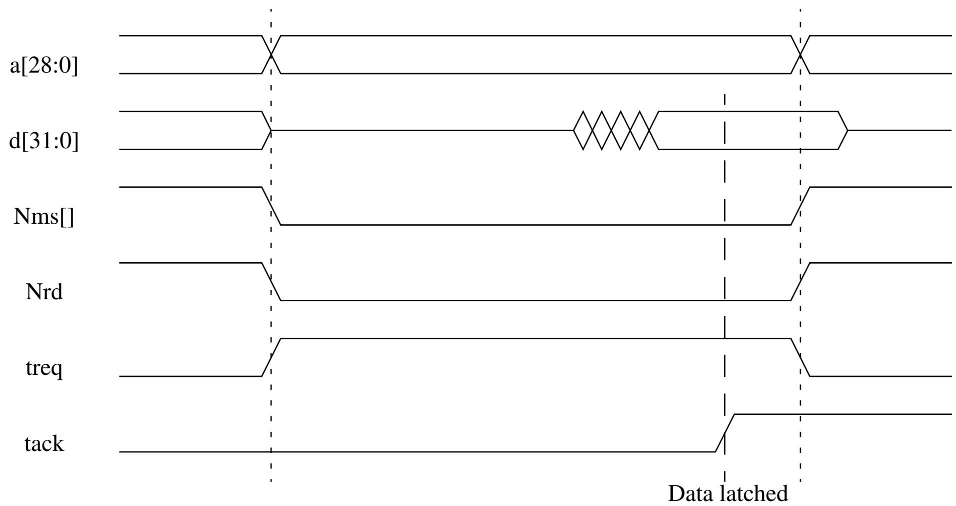
The Compare Register (CPR) is a 16 bit register which is compared with the Timer each time it is incremented. When the two registers are equal a flag is set which is visible in the Timer Control Register and may be used to cause an interrupt.

Sample Memory Cycles

The timing for memory cycles is controlled by the Region Timing Registers (RTR) and by the external delay (Dt) between the **treq** and **tack** pins. In any system with a variety of memory devices, the chosen value of Dt will be a compromise dictated by the range of access times needed and the limited flexibility offered by the RTR. If the system contains DRAM, Dt must be chosen to suit that and the other memory timings arranged around that value.

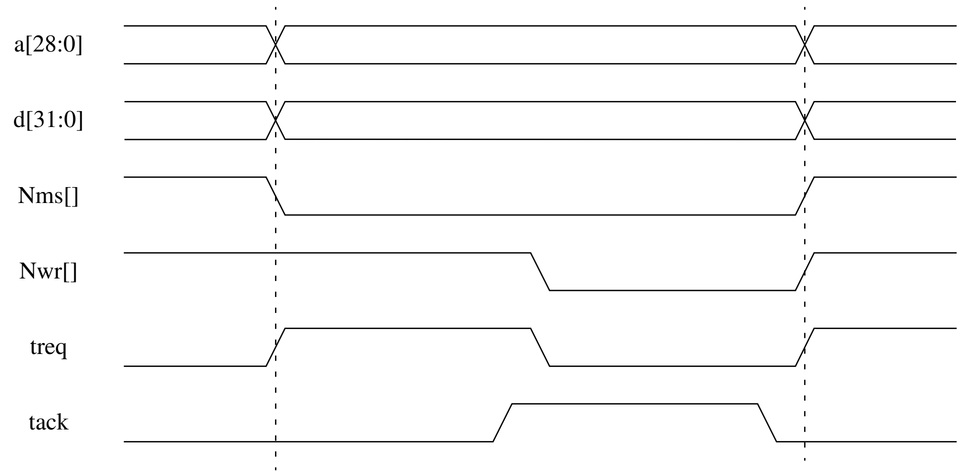
Read - minimum timing (1Dt + no setup/hold)

In this case one **treq/tack** cycle is used to determine the access time. This is achieved by writing 0x00 to the RTR. In a read cycle, data is latched on the final transition of **tack** which occurs while **Nrd** is active.



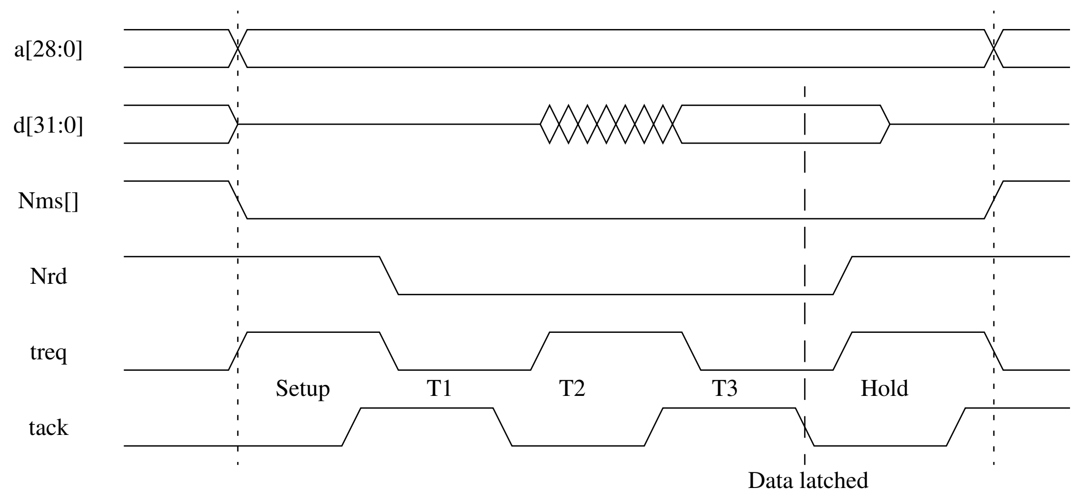
Write - minimum timing (1Dt + no setup/hold)

Here the same timing parameters are programmed into the RTR but the memory interface forces an extra **treq/tack** cycle to ensure that the address is stable when the write strobe becomes active.



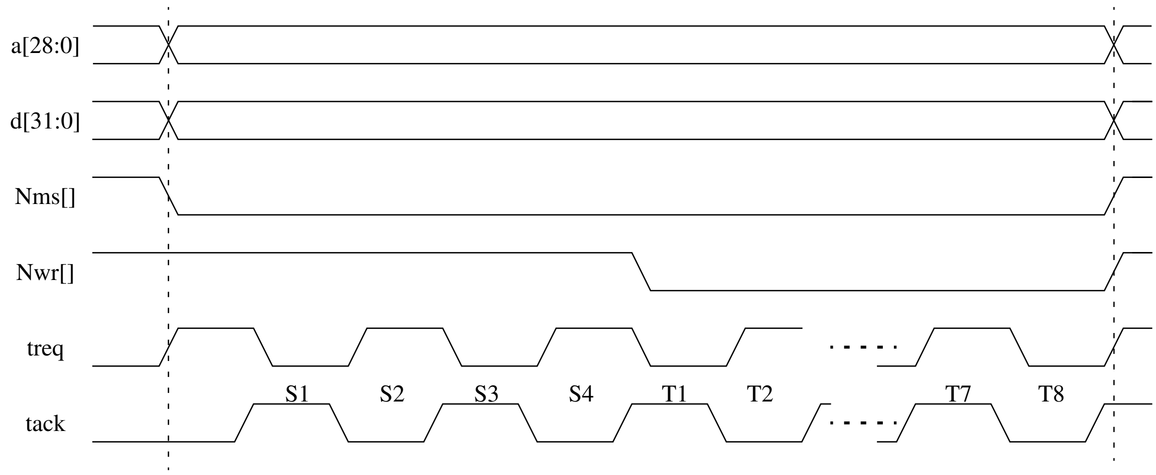
Read - 3Dt + setup/hold

In this example, setup and hold have been specified in the RTR. The value written to the RTR is 0x1A. The effect of setup and hold is to extend the time that the address is valid and the memory select strobe (**Nms[]**) asserted around the data strobe signals, **Nwr[]** or, in this case, **Nrd**. This is particularly useful for peripheral devices which often have long data turn off times, where the use of hold time can help prevent data bus conflicts following read cycles. Such devices also often require significant address setup time in write cycles. Note that all write cycles have an inherent setup time of a single Dt and specifying additional setup time in the RTR may not always be necessary.



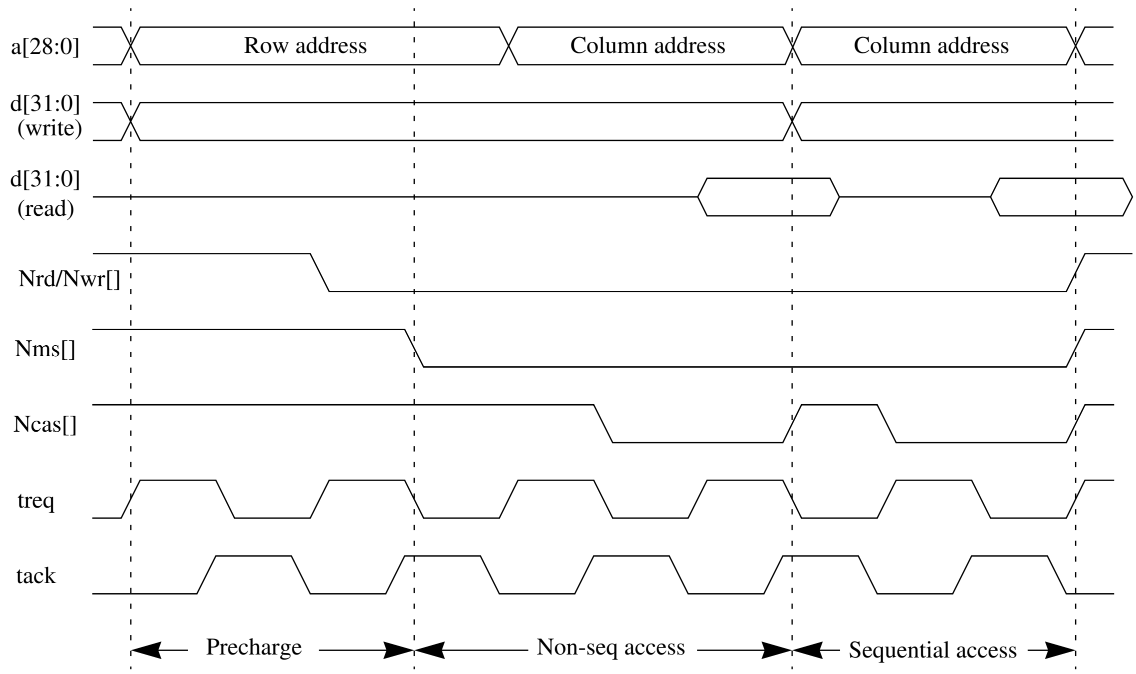
Write - 8Dt + setup

In this case the RTR has been written with 0x15 which specifies setup and slow timing. As the cycle is a write, there is a single Dt delay at the beginning. This is followed by 4Dt of setup and then a write strobe of 8Dt.

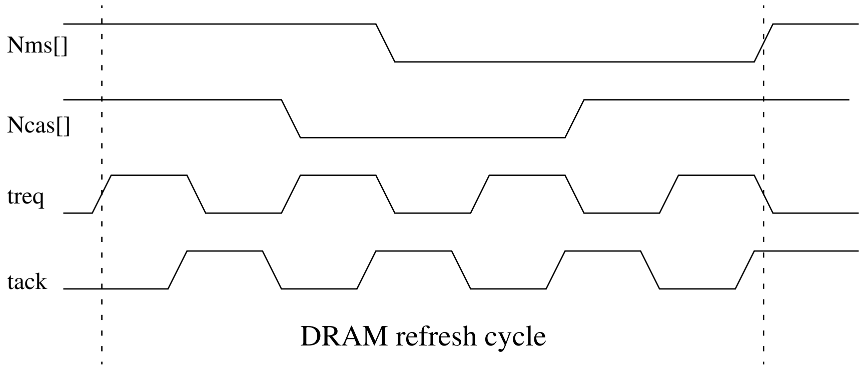


Dynamic Memory Timing

A basic DRAM cycle is 7 Dt, 3 of which are used for RAS precharge and 4 for the actual access. Where page-mode access is possible, that is, the following access uses a sequential address, the basic cycle is extended in multiples of 3Dt.

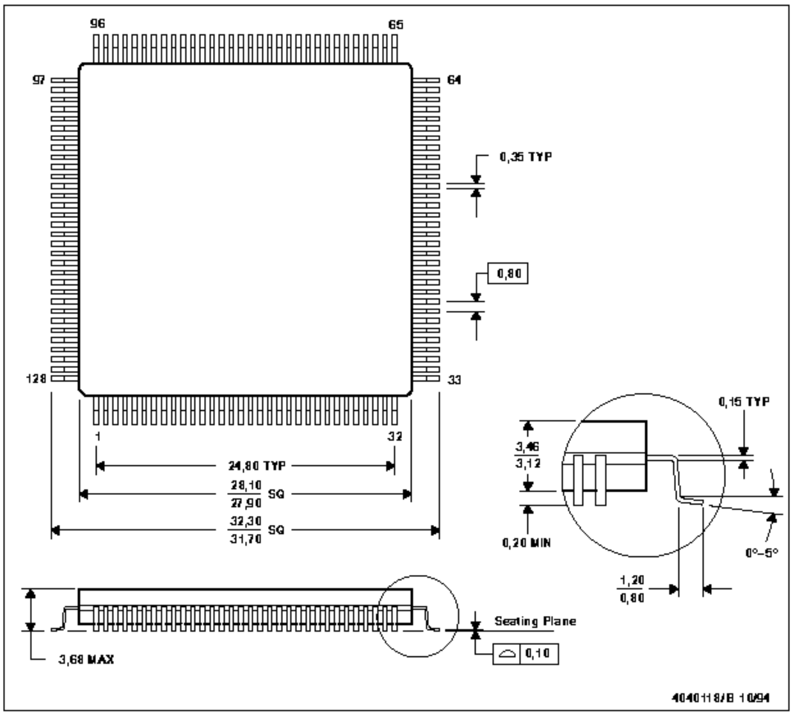


Refresh cycles also use a pattern of 7Dt. They perform a CAS before RAS refresh and do not supply a refresh address. The **Nrd** and **Nwr[3:0]** pins go high at the start of the refresh cycle, the data bus (**d[31:0]**) goes high impedance and the address bus contains an unspecified value. Those **Nms[]** pins which are marked as being connected to DRAM by the Region Timing Registers will become active in the refresh cycle as will some or all of the **Ncas[3:0]** pins depending on the width fields of the Region Architecture Registers.



DRAM refresh cycle

Mechanical Data & Pinout



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Table 10: Pin List.

Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
1	N/C	33	N/C	65	N/C	97	N/C
2	Nwr[1]	34	a[11]	66	d[12]	98	io[5]
3	Nwr[0]	35	a[10]	67	d[13]	99	io[6]
4	Ncas[3]	36	a[9]	68	d[14]	100	io[7]
5	Ncas[2]	37	a[8]	69	d[15]	101	sp[0]
6	Vdd	38	Vdd	70	Vdd	102	sp[1]
7	Vss	39	Vss	71	Vss	103	sp[2]
8	Ncas[1]	40	a[7]	72	d[16]	104	Vdd
9	Ncas[0]	41	a[6]	73	d[17]	105	Vss
10	Nrd	42	a[5]	74	d[18]	106	Nfiq
11	a[28]	43	a[4]	75	d[19]	107	Nirq
12	a[27]	44	a[3]	76	d[20]	108	dbe
13	a[26]	45	a[2]	77	d[21]	109	abe
14	a[25]	46	a[1]	78	d[22]	110	tack
15	a[24]	47	a[0]	79	d[23]	111	treq

Table 10: Pin List.

Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
16	Vdd	48	Vdd	80	Vdd	112	Nrst
17	Vss	49	Vss	81	Vss	113	Ntest
18	a[23]	50	d[0]	82	d[24]	114	Xin
19	a[22]	51	d[1]	83	d[25]	115	Xout
20	a[21]	52	d[2]	84	d[26]	116	Vdd
21	a[20]	53	d[3]	85	d[27]	117	Vss
22	a[19]	54	d[4]	86	d[28]	118	Nms[7]
23	a[18]	55	d[5]	87	d[29]	119	Nms[6]
24	a[17]	56	d[6]	88	d[30]	120	Nms[5]
25	a[16]	57	d[7]	89	d[31]	121	Nms[4]
26	Vdd	58	Vdd	90	Vdd	122	Nms[3]
27	Vss	59	Vss	91	io[0]	123	Nms[2]
28	a[15]	60	d[8]	92	io[1]	124	Nms[1]
29	a[14]	61	d[9]	93	io[2]	125	Nms[0]
30	a[13]	62	d[10]	94	io[3]	126	Nwr[3]
31	a[12]	63	d[11]	95	io[4]	127	Nwr[2]
32	N/C	64	N/C	96	N/C	128	N/C

Test Mode

In test mode (the **Ntest** pin is low), all signals of the AMULET2 processor macrocell are brought out to pins for testing or simply to use the chip in this mode. Note that **dbe** is the output enable for all pins marked IOZd and **abe** is the output enable for all pins marked OZa. In test mode, the **tack** pin should be held low to keep some internal logic in a known state. The pin correspondence between normal and test modes is as follows

Table 11: Test mode pins

AMULET2e	(Type)	AMULET2	(Type)
d[31:0]	IOZd	d[31:0]	IOZd
a[28:0]	OZa	a[28:0]	OZa
Nrd	OZa	a[29]	OZa
Ncas[0]	OZa	a[30]	OZa
Ncas[1]	OZa	a[31]	OZa
Ncas[2]	OZa	seq	OZa
Ncas[3]	OZa	inc	OZa
Nwr[0]	OZa	ren	OZa

Table 11: Test mode pins

AMULET2e	(Type)	AMULET2	(Type)
Nwr[1]	OZa	wen	OZa
Nwr[2]	OZa	usr	OZa
Nwr[3]	OZa	opc	OZa
treq	O	(-)	O
xout	O	(-)	O
xin	I	(-)	I
Nrst	I	Nrst	I
tack	I	Nrst (2e logic)	I
dbe	I	dbe	I
abe	I	abe	I
Nirq	I	Nirq	I
Nfiq	I	Nfiq	I
Ntest	I (=1)	Ntest	I (=0)
Nms[0]	OZa	dabt[0]	I
Nms[1]	OZa	dabt[1]	I
Nms[2]	OZa	pabt	I
Nms[3]	OZa	ack	I
Nms[4]	OZa	drq	I
Nms[5]	OZa	byte	OZa
Nms[6]	OZa	req	OZa
Nms[7]	OZa	dak	OZa
IO[7]	IOZ	BTBpson	I
IO[6]	IOZ	ALUlr	I
IO[5]	IOZ	LDRlr	I
IO[4]	IOZ	HALTon	I
IO[3]	IOZ	BTBfl	I
IO[2]	IOZ	BTBon	I
IO[1]	IOZ	BigEnd	I
IO[0]	IOZ	Nabt	I