

# Automatic Scan Insertion and Pattern Generation for Asynchronous Circuits

Aristides Efthymiou  
Dep. of Computer Science,  
Un. of Manchester,  
Manchester M13 9PL, UK  
a.efthymiou@cs.man.ac.uk

Christos Sotiriou  
Institute of Computer Science,  
FORTH  
Heraklion, GR 711 10 Greece  
sotiriou@ics.forth.gr

Douglas Edwards  
Dep. of Computer Science,  
Un. of Manchester,  
Manchester M13 9PL, UK  
d.edwards@cs.man.ac.uk

## Abstract

*This paper presents  $3\phi$ LSSD, a novel, easily-automatable approach for scan insertion and ATPG of asynchronous circuits.  $3\phi$ LSSD inserts scan latches only into global circuit feedback paths, leaving the local feedback paths of asynchronous state-storing gates intact. By employing a three-phase LSSD clocking scheme and complemented by a novel ATPG method, our approach achieves industrial quality testability with significantly less area overhead testing the same number of faults compared to full-scan LSSD. The effectiveness of our approach is demonstrated on an asynchronous SOC interconnection fabric, where our  $3\phi$ LSSD ATPG tool achieved over 99% test coverage.*

## 1. Introduction

In the class of “bundled-data” asynchronous circuits (data arrive as a bundle w.r.t. a request or acknowledgement signal), the datapath is a collection of pipeline latches and combinational circuits, as in a standard synchronous system. Thus, testing the datapath is straightforward and standard testing techniques can be applied. On the other hand, testing asynchronous control is harder because there is a large number of local state variables which are not updated with a global clock signal. Moreover, C gates, which are commonly used as storage elements, hold the state in a feedback loop, rather than in a conventional latch or flip/flop. C gates are effectively a special form of set-reset latches, e.g. a 2-input C gate waits until both its inputs assume the same logic value, then sets its output to that value.

Conventional, full-scan methods have been successfully employed for testing asynchronous circuits [1]: each feedback loop is broken, in test mode, by inserting a LSSD-type scan-latch. The contribution of this paper is a systematic partial-scan approach, which avoids inserting scan latches to break the *local* feedback loops present in C gates.

## 2. Testing C gates

Since the feedback loops in the C-gates are not ‘scanned’, sequential patterns must be generated to provide adequate fault coverage. In our experience, due to the existence of the feedback path, commercial ATPG tools are unable to generate test patterns that produce satisfactory fault coverage. Even adding gates to control the feedback value, does not raise the coverage of the patterns over 89%.

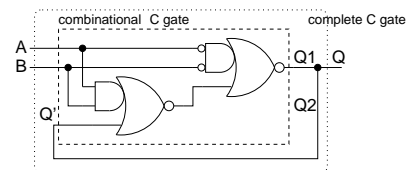


Figure 1. The 2-input C-gate.

Figure 1 shows an implementation of a 2-input C gate using common std. cells. If the feedback is removed, i.e. the output feeding back is considered as another primary input, a C gate is transformed into a combinational circuit for which ATPG can trivially produce test patterns. It can be shown (the proof is not included due to space limitations) that the faults in the “complete C gate” dominate those of the “combinational C gate”, thus the patterns generated for the latter can be used for testing the complete C gate.

Care must be taken to put the automatically generated patterns in the right order, so that the output of the C gate, when a pattern is applied, becomes the Q’ input of the next pattern. Moreover hazards, which can occur when both inputs of the C gate change in opposite directions, should be avoided. Table 1 shows a safe pattern sequence for a 2-input C gate, which achieves 100% stuck-at fault coverage. Note that two patterns are used twice to avoid hazards (marked with \*).

