Power Consumption and Testability of CMOS VLSI Circuits

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Abstract

A relationship between the power consumption and the testability of CMOS VLSI circuits is demonstrated in this paper. The method used to estimate this correlation is based on elements of information theory. It is shown that the average output information content of a circuit node is proportional to its signal transition probability. As a consequence, design for low power consumption and design for testability are in direct conflict. The resolution of this conflict lies in separating the testing issues from the low power issues by giving the circuit distinct operating and test modes.

1: Introduction

The rapid development of CMOS technology makes transistors smaller allowing a chip to incorporate ever larger numbers of them [1]. CMOS VLSI circuits are increasingly used in portable environments where power and heat dissipation are vital issues. Examples of such applications are portable calculators, digital watches, mobile computer systems, etc. As a result, the power dissipation of CMOS VLSI circuits is a growing concern for design engineers.

The power dissipated by CMOS circuits can be divided into three categories [1,2]:

- static power consumption due to leakage current (PW_{stat});
- dynamic power dissipation caused by switching transition current (PW_{sw});
- transient short-circuit current (PW_{sc}).

The total power dissipation of a CMOS circuit can therefore be represented by the following sum:

$$PW_{total} = PW_{stat} + PW_{sw} + PW_{sc}.$$

In "well-designed" data processing circuits the switching power is typically from 70% to 95% of the total power consumption (if the circuit is badly-designed the proportion of static and short-circuit power dissipation increases) [3]. The majority of power estimation tools are oriented towards calculating only the average switching power of CMOS circuits using the following formula [2]:

$$PW_{sw} = f \cdot V_{dd}^2 \cdot \sum_{i=1}^{M} \left(P_{tr_i} \cdot C_i \right), \tag{1}$$

where f is the clock frequency; V_{dd} is the power supply voltage; M is the total number of nodes in the circuit; C_i is the ith nodal capacitance; P_{tr_i} is the transition probability of the ith node.

After fabrication, a digital circuit must be tested to ensure that it is fault free. This is not an easy task since the increasing number of logic elements placed on a chip leads to a reduction in the controllability and observability of the internal nodes of the circuits. Several design for testability (DFT) methods have been developed for digital circuits [4,5] which aim to facilitate the testing of digital circuits for fabrication faults. Since DFT methods affect the circuit design, this raises the question: "How do DFT methods affect the power consumption of a circuit?". In this paper, we attempt to answer this question.

The rest of the paper is organised as follows: section 2 describes aspects of information theory and its application to digital circuits; section 3 shows how the average information content of a circuit node correlates with its transition probability; section 4 is a discussion of the implications for low power designs; section 5 summarises the principal conclusions of the paper.

2: Information theory and digital circuits

Output node capacitances create memories in static CMOS circuits. The circuit itself can also have state holding elements. Let us consider a circuit with one output. This circuit has only two possible states: zero and one. The circuit changes its states during the application of patterns to its inputs. This process can be represented by the Markov chain shown in Figure 1 regardless of whether the circuit is a sequential one or a combinational one. The Markov chain contains two states marked by zero and one. The transition probabilities between the states are placed on the correspondent arcs of the chain where $p_i(j)$ denotes the probability of the transition from state i to state j (i,j=0,1).

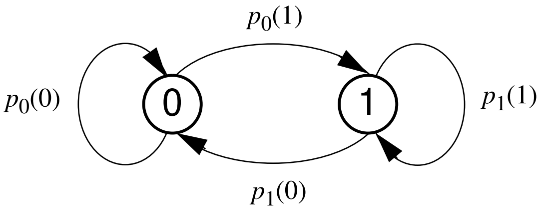

Figure 1: *Markov chain representing the mechanism of changing the states of the circuit with one output*

The following system of equations describes the behaviour of the Markov chain illustrated in Figure 1:

$$\begin{gathered} P_0 = P_0 \cdot p_0(0) + P_1 \cdot p_1(0) , \\ P_1 = P_0 \cdot p_0(1) + P_1 \cdot p_1(1) , \\ P_1 + P_0 = 1 , \end{gathered} \tag{2}$$

where P_0 and P_1 are the probabilities of state 0 and state 1, respectively.

Note that for the Markov chain shown in Figure 1

$$p_0(1) + p_0(0) = 1 , \tag{3}$$

$$p_1(0) + p_1(1) = 1 . \tag{4}$$

Solving system (2) the probabilities of states 0 and 1 can be found as

$$P_1 = p_0(1) / (p_0(1) + p_1(0)) , \tag{5}$$

$$P_0 = p_1(0) / (p_0(1) + p_1(0)) . \tag{6}$$

Thus, only two transition probabilities $p_0(1)$ and $p_1(0)$ are required to fully describe the behaviour of the circuit with one output.

For combinational circuits

$$p_0(1) = p_1(1) = p , \tag{7}$$

$$p_1(0) = p_0(0) = q , \tag{8}$$

where $p + q = 1$. As a result, $P_1 = p$ and $P_0 = q$.

Figure 2 shows six two-input logic blocks and their transition probabilities. It is assumed that input signal probabilities p_a and p_b are independent. The last three logic blocks shown in Figure 2 are Muller C-elements [6]. A C-element is a memory element which is widely used in asynchronous circuits.

The logic function of the two-input symmetric C-element (the first C-element) is

$$c_t = a \cdot b + a \cdot c_{t-1} + b \cdot c_{t-1} , \tag{9}$$

where a and b are the inputs; c_t is the output of the C-element at time t.

The output of the symmetric C-element is high or low when both inputs are high or low, respectively. The C-element preserves its current state when the inputs are different. In order to calculate the output signal probability of the two-input symmetric C-element we use equations (5) and (6). As a result,

$$P_1 = p_a \cdot p_b / (p_a \cdot p_b + q_a \cdot q_b) , \tag{10}$$

$$P_0 = q_a \cdot q_b / (p_a \cdot p_b + q_a \cdot q_b) . \tag{11}$$

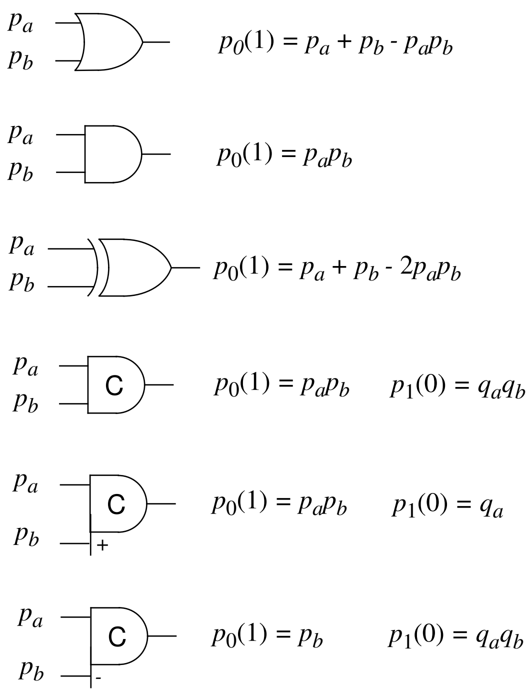

Figure 2: *Logic elements and their transition probabilities*

The last two C-elements are asymmetric C-elements which perform different functions:

- for the second C-element:

$$c_t = a \cdot b + a \cdot c_{t-1}, \tag{12}$$

- for the third C-element:

$$c_t = b + a \cdot c_{t-1}. \tag{13}$$

The output of the asymmetric C-element which performs according to function (12) is high if both its inputs are high and low if only input a is low. It keeps its current state zero when input a or b is low and preserves state one if input a is high. The output of the asymmetric C-element whose behaviour is described by function (13) is low if both its inputs are low and high if input b is high. It does not change its current state zero if input b is low and preserves its state one if input a or b is high. The state probabilities of the asymmetric C-elements can easily be found using equations (5) and (6).

Let us estimate the average information content on the output of a circuit. According to information theory, the average information content or entropy (H) of a discrete finite state type source is [7,8]

$$H = \sum_i P_i H_i = -\sum_{i,j} P_j p_j(i) \log_2 p_j(i), \tag{14}$$

where P_j is the probability of state j; $p_j(i)$ is the probability of the transition from state j to state i.

Thus, the average output information content of the circuit described by the Markov process shown in Figure 1 is calculated as follows:

$$H = P_0 H_0 + P_1 H_1, \tag{15}$$

i.e.,

$$H = -P_0 p_0(0) \log_2 p_0(0) - P_0 p_0(1) \log_2 p_0(1)$$
$$-P_1 p_1(0) \log_2 p_1(0) - P_1 p_1(1) \log_2 p_1(1). \tag{16}$$

The average information content on the output of the combinational circuit is equal to

$$H = -p \log_2 p - (1-p) \log_2 (1-p). \tag{17}$$

Let $p_0(1) = x$ and $p_1(0) = y$ then

$$H(x, y) = -\frac{x}{x+y} H(y) - \frac{y}{x+y} H(x), \tag{18}$$

where $H(y) = y \log_2 y + (1-y) \log_2 (1-y)$ and $H(x) = x \log_2 x + (1-x) \log_2 (1-x)$.

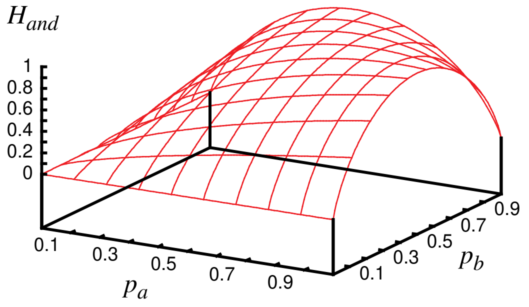

Figure 3: *Average ouput information content of the two-input AND gate*

In order to find an extremum of function $H(x,y)$ the following system of two equations must be solved:

$$\frac{\partial}{\partial x} H(x, y) = 0,$$
$$\frac{\partial}{\partial y} H(x, y) = 0. \tag{19}$$

System 19 can be modified as

$$(x+y)(\log_2(1-x) - \log_2 x) + H(y) - H(x) = 0,$$
$$(x+y)(\log_2(1-y) - \log_2 y) + H(x) - H(y) = 0. \tag{20}$$

The only solution of system 20 is x=y=0.5. It is easy to show that

$$Max(H(x, y)) = H(0.5, 0.5) = 1.$$

Thus, the maximum information content can be reached when the transition probabilities between the states of the circuit are equiprobable. This result can easily be generalised for any number of circuit states.

Figures 3 and 4 illustrate graphically the dependencies between the average output information content (H) and input signal probabilities p_a and p_b of the two-input AND and XOR gate, respectively. Figures 5 and 6 show graphs

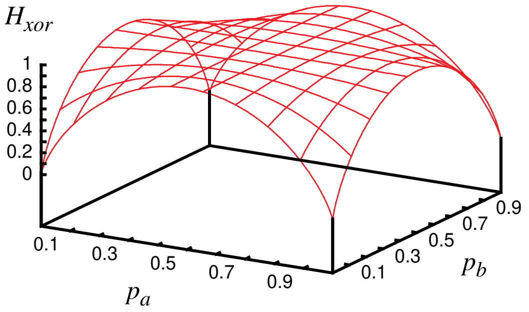

Figure 4: *Average ouput information content of the two-input XOR gate*

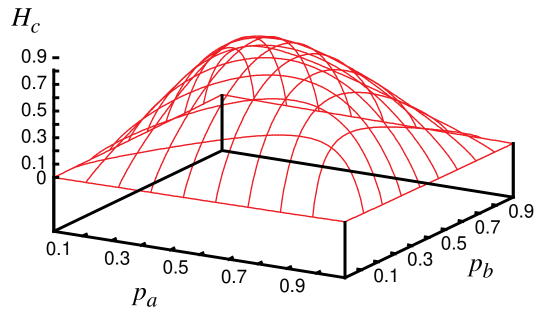

Figure 5: *Average ouput information content of the two-input symmetric C-element*

$H_c(p_a,p_b)$ and $H_{ac}(p_a,p_b)$ of the two-input symmetric and asymmetric C-elements which perform according to equations 9 and 12, respectively. Note that the maximum information content is reached when the transition probabilities of the logic elements are equal to 0.5. For instance, H_{and}=1 when $p_a p_b$=0.5. For the XOR gate (see Figure 4), H_{and}=1 when p_a=0.5 or p_b=0.5. The maximum value of the average output information content of the symmetric C-element (see Figure 5) never reaches 1 ($MAX(H_c)$=0.81) even when its probability of state 1 or 0 is 0.5 (when p_a=p_b=0.5). In fact, the transition probabilities of the symmetric C-element can never be equal to 0.5. The average output information content of the asymmetric C-element described by equation 12 reaches 1 at point (p_a=0.5;p_b=1) (see Figure 6). This is because the asymmetric C-element works as a repeater of the information from its input *a* when *b*=1.

3: Information content and transition probability

Let us consider the following expression:

$$\log_2 v = \frac{\ln(1-v)}{\ln 2}. \qquad (21)$$

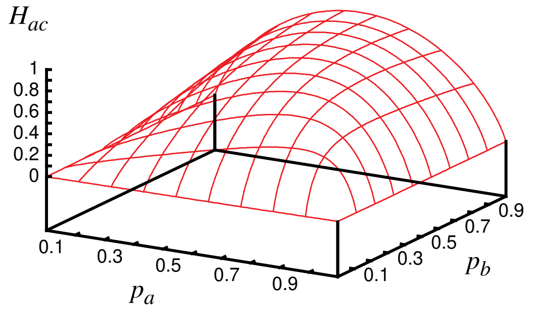

Figure 6: *Average ouput information content of the two-input asymmetric C-element*

It is known that

$$-\ln(1-v) = \sum_{r=1}^{\infty} \frac{v^r}{r},$$

where $0 \le v < 1$ [9].

Hence,

$$-\ln v = \sum_{r=1}^{\infty} \frac{(1-v)^r}{r} = (1-v) \sum_{r=1}^{\infty} \frac{(1-v)^{r-1}}{r}. \qquad (22)$$

Equation 22 can be substituted by the following inequality:

$$-\ln v \ge 1 - v \qquad (23)$$

since $\sum_{r=1}^{\infty} \frac{(1-v)^{r-1}}{r} \ge 1$ for $0 \le v < 1$.

Taking into account equation 21 and inequality 23, equation 16 can easily be transformed into the following inequality:

$$H \ln 2 \ge P_0 p_0(0)\,[1 - p_0(0)] + P_0 p_0(1)\,[1 - p_0(1)]$$
$$+ P_1 p_1(0)\,[1 - p_1(0)] + P_1 p_1(1)\,[1 - p_1(1)]. \qquad (24)$$

Inequality 24 can be simplified bearing in mind the basic relationships between transition probabilities of the Markov process described by equations 3 and 4. Hence,

$$H \ln 2 \ge P_0 p_0(0)\, p_0(1) + P_0 p_0(1)\, p_0(0)$$
$$+ P_1 p_1(0)\, p_1(1) + P_1 p_1(1)\, p_1(0)$$

or

$$H \ge 2\,[P_0 p_0(0)\, p_0(1) + P_1 p_1(1)\, p_1(0)] / \ln 2. \qquad (25)$$

Substituting the probabilities of states 1 and 0 by expressions 5 and 6, respectively, inequality 25 can be written as

$$H \ge \gamma \frac{2 p_0(1)\, p_1(0)}{[p_0(1) + p_1(0)]}, \qquad (26)$$

where

$$\gamma = \frac{[p_0(0) + p_1(1)]}{\ln 2} \text{ and } \gamma \ge 0.$$

The signal transition probability (P_{tr}) on the output of the circuit is calculated as follows:

$$P_{tr} = P_0 p_0(1) + P_1 p_1(0). \qquad (27)$$

The following equation can be derived by substituting state probabilities P_1 and P_0 in equation 27 by expressions 5 and 6, respectively:

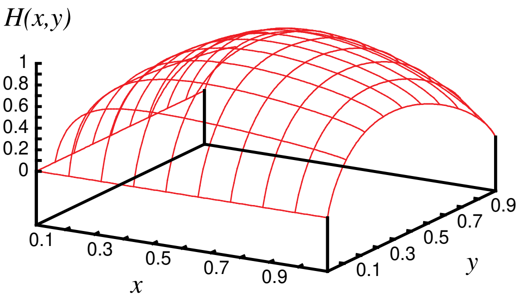

Figure 7: *Graph of function H(x,y)*

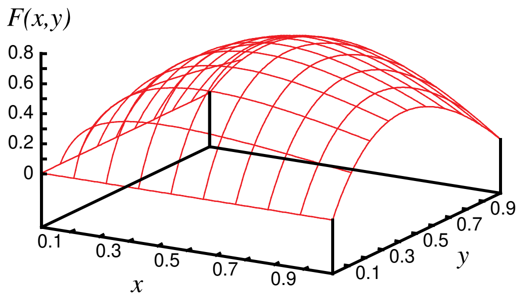

Figure 8: *Graph of function F(x,y)*

$$P_{tr} = \frac{2p_0(1)p_1(0)}{p_0(1)+p_1(0)}. \qquad (28)$$

The comparison of expressions 26 and 28 allows us to conclude that

$$H \geq \gamma P_{tr}. \qquad (29)$$

For combinational circuits (see equations 7 and 8) the following expressions can easily be obtained:

$$H \geq \frac{2pq}{\ln 2},\ P_{tr} = 2pq,\ \gamma = (\ln 2)^{-1}. \qquad (30)$$

Therefore, the average output information content and the output signal transition probability correlate strongly.

Consider the following function:

$$F(x, y) = \gamma(x, y)P_{tr}(x, y) = \frac{2xy(2-x-y)}{(x+y)\ln 2}, \qquad (31)$$

where variables x and y have the same meaning as in equation 18.

In order to find an extremum of function $F(x,y)$ the following system of two equations must be solved:

$$\frac{\partial}{\partial x}F(x, y) = 0, \qquad \frac{\partial}{\partial y}F(x, y) = 0. \qquad (32)$$

After trivial manipulations system 32 is modified as

$$2y/(x+y)^2 - 1 = 0, \qquad 2x/(x+y)^2 - 1 = 0. \qquad (33)$$

The solution of system 33 is x=y=0.5. It can easily be shown that

$$Max(F(x, y)) = F(0.5, 0.5) = (2\ln 2)^{-1}.$$

Thus, functions $H(x,y)$ and $F(x,y)$ exhibit very similar behaviour. The only difference is that $H(x,y)$ is always greater or equal to $F(x,y)$ when $0 \leq x, y \leq 1$. Figures 7 and 8 illustrate graphs of functions $H(x,y)$ and $F(x,y)$.

In order to estimate how close functions $H(x,y)$ and $F(x,y)$ are, we investigate the following function:

$$\varepsilon(x, y) = H(x, y) - F(x, y), \qquad (34)$$

where $\varepsilon(x,y)$ is the absolute error between function $H(x,y)$ and its approximation $F(x,y)$.

It is trivial to prove that the maximum of function $\varepsilon(x,y)$ is reached at the point when x=y=0.5 ($Max(\varepsilon(x,y))$=0.28). As a result, the maximum absolute error of approximation $F(x,y)$ can never be more than 28%. Figure 9 shows a graph of function $\varepsilon(x,y)$.

4: Discussion

It has been shown that the testability of a circuit is proportional to its output information content [10]. This means that the more information the nodes of the digital circuit carry to its outputs, the more testable the circuit is, and vice versa. The dynamic power consumption of a CMOS circuit is also proportional to the transition probabilities of its nodes (see equation 1). Hence, the more testable a circuit is, the more dynamic power it dissipates. The converse statement, that the more power consuming the circuit is the

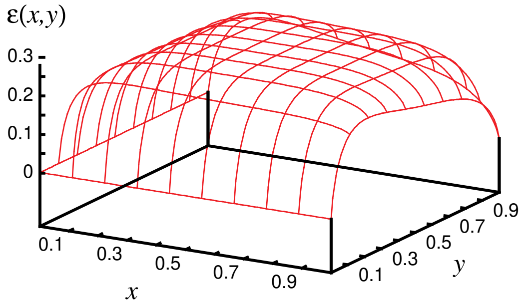

Figure 9: *Graph of function ε(x,y)*

more testable it is, can be justified only if the increase in the circuit power dissipation is caused by increased activity in its nodes.

Shen et al. observed that both the random pattern testability and the power dissipation of a combinational logic network are linked to the signal probabilities of its nodes [11]. They proposed probability modification techniques to restructure the combinational networks to improve both their transition signal probabilities and their power dissipations but these delivered insignificant improvements.

Williams and Angell showed that increasing the transition probabilities in the nodes of a circuit improves its controllability and, therefore, its testability [12]. The testability of the circuit can also be improved by inserting test points at some of its nodes, increasing the observability of the circuit. Improving controllability has a direct power cost due to the increased number of transitions, whereas improving observability only marginally increases the power dissipation due to an increased switched capacitance.

Clearly, the power dissipation of a digital circuit is of interest principally when it is in operation in its intended application. Power consumption during test is not usually important.

An approach which offers a compromise between testability and power consumption is to design the circuit to work in two distinct operating modes. In normal operation mode, it performs the specified function dissipating minimal or close to minimal switching energy. The circuit is set to test mode to make its testing simple. During the test, the circuit is tested extensively dissipating more energy.

5: Conclusions

We have shown that the testability of CMOS VLSI circuits correlates with the switching power that they dissipate. The mathematical dependencies presented allow us to conclude that improving the testability features of a CMOS circuit leads to an increase in its switching power dissipation. As a result, design for testability and design for low power dissipation are in direct conflict. The resolution of this conflict lies in separating the testing issues from low power issues by giving the circuit distinct operating and test modes.

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