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ARM CPUs

- Outline:
  - the ARM710T, 720T and 740T
  - the SA-110 StrongARM
  - the ARM920T and 940T
  - the ARM1020E
  - the ARM1176JZF

  ☞ hands-on: code profiling

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ARM CPUs

- This section contains ARM macrocells *examples*
- Many variants exist in each family
  - this should give the broad picture
  - see product manuals for specific details
- Variations:
  - cache size (and organisation)
    - especially in synthesizable macrocells (“-s”)
  - instruction set enhancements included
  - coprocessors etc. included

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ARM710T, 720T and 740T

- All have …
  - an ARM7TDMI processor core, with:
  - an 8 Kbyte instruction & data cache
    - 4-way set-associative, 16-byte lines
    - write-through
  - an AMBA interface
    - shared by instruction and data ports
  - an 8 data word, 4 address write buffer

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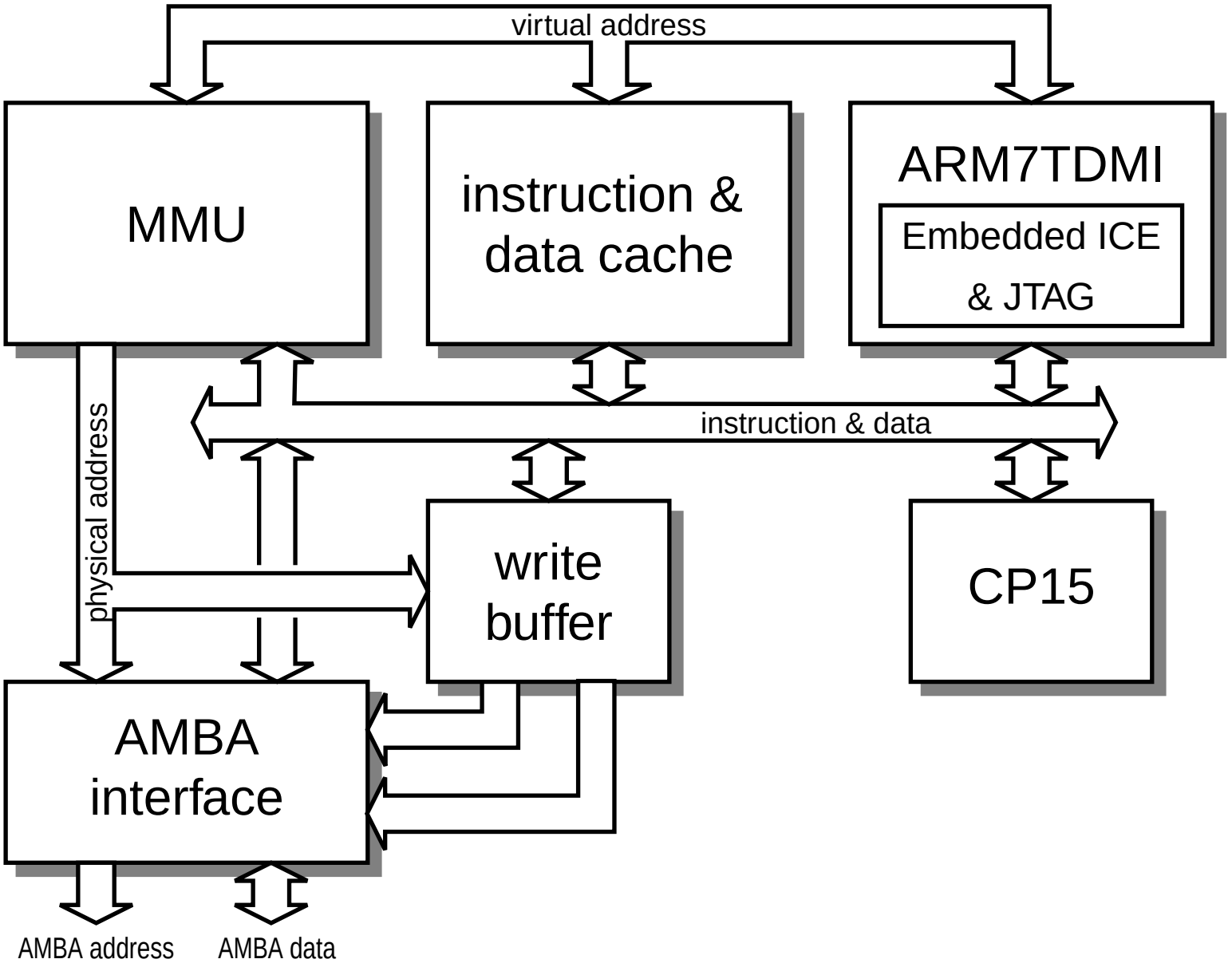
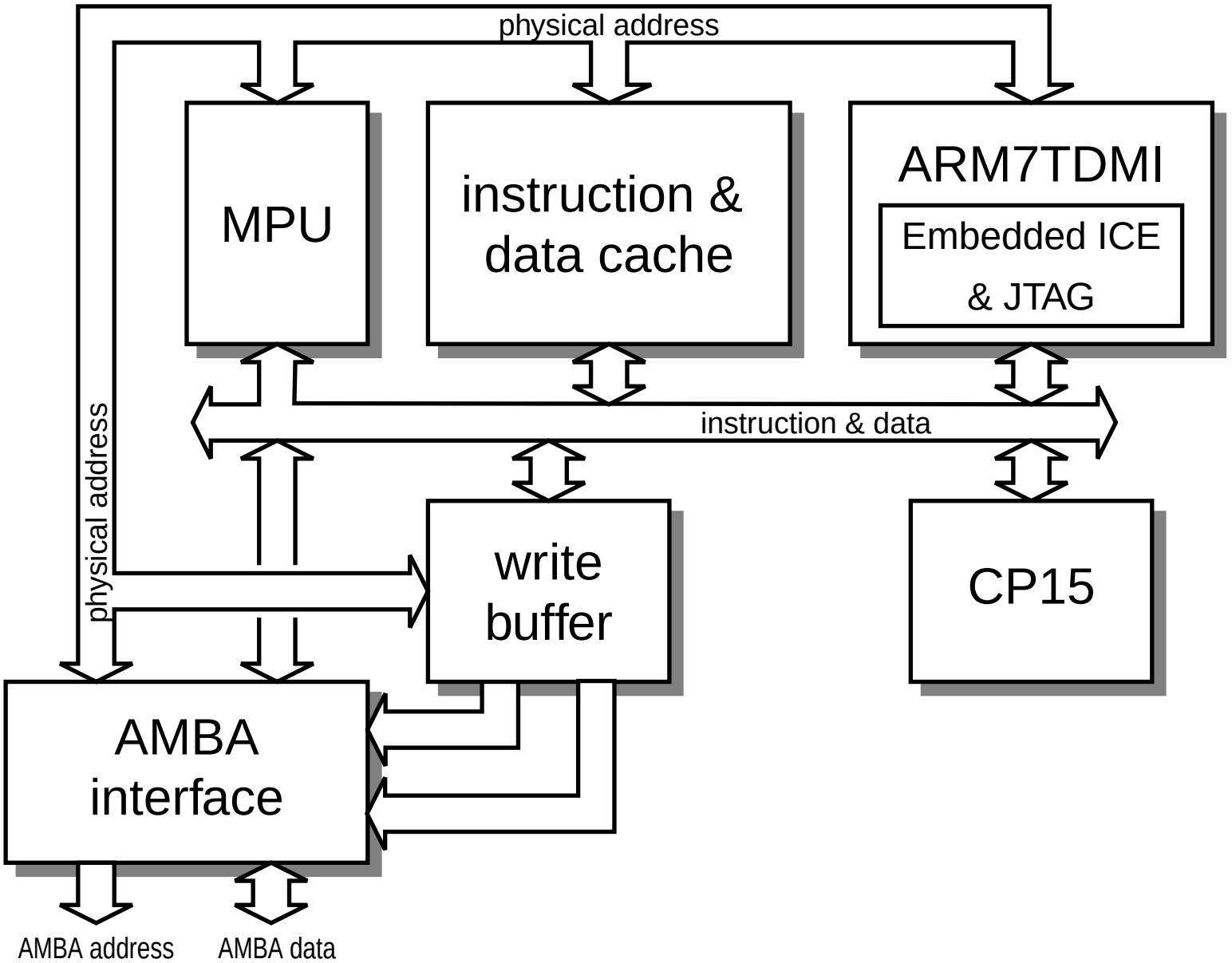
ARM710T, 720T and 740T

- The ARM710T and 720T have …
  - an MMU with a 64-entry TLB
- The ARM720T also has WinCE support
  - ProcessID register relocates the 1st 32 Mbytes of memory
  - exception vectors relocatable to 0xffff0000
- The ARM740T has …
  - a simple memory protection unit
    - there is no address translation system

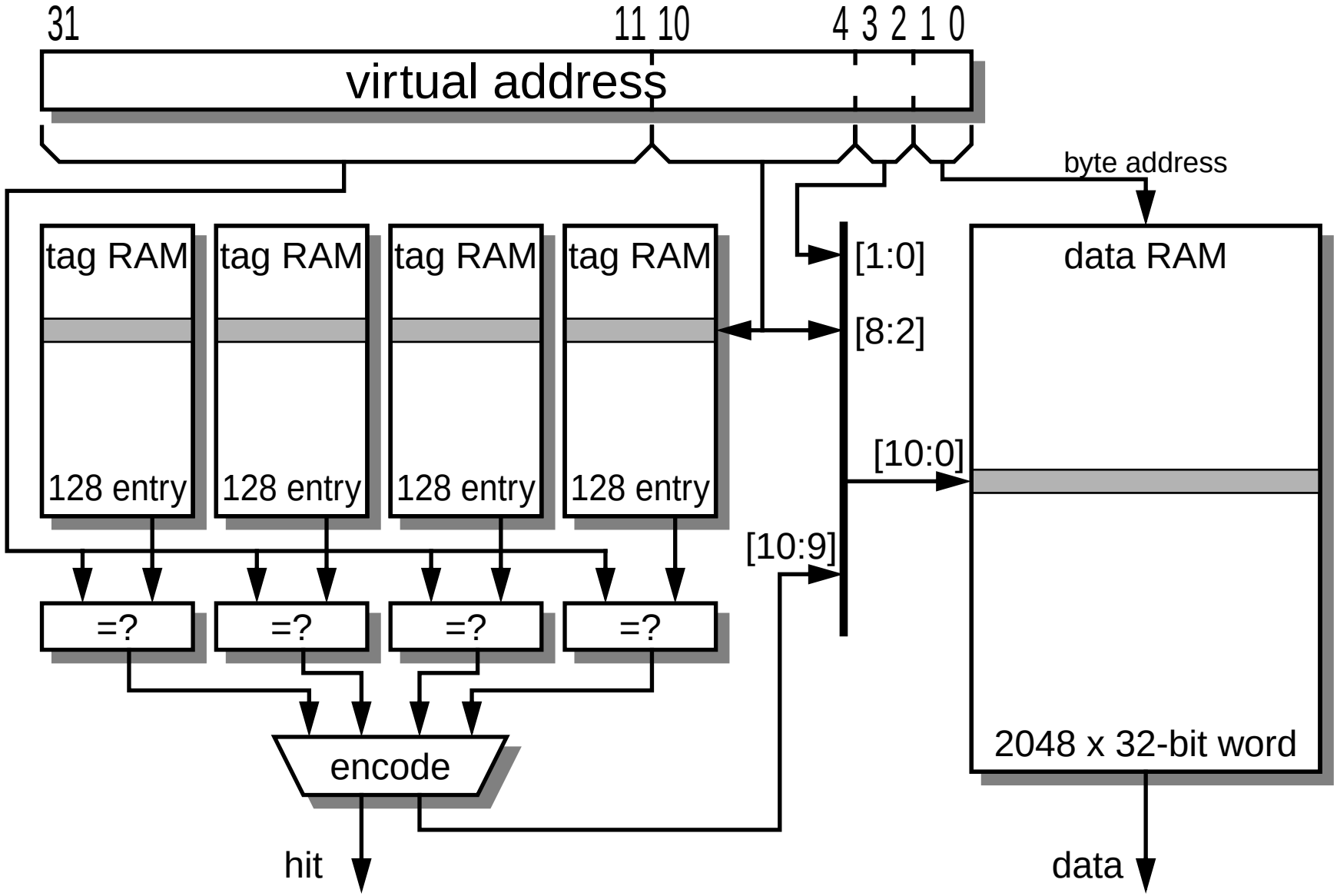
ARM710T and 720T organization



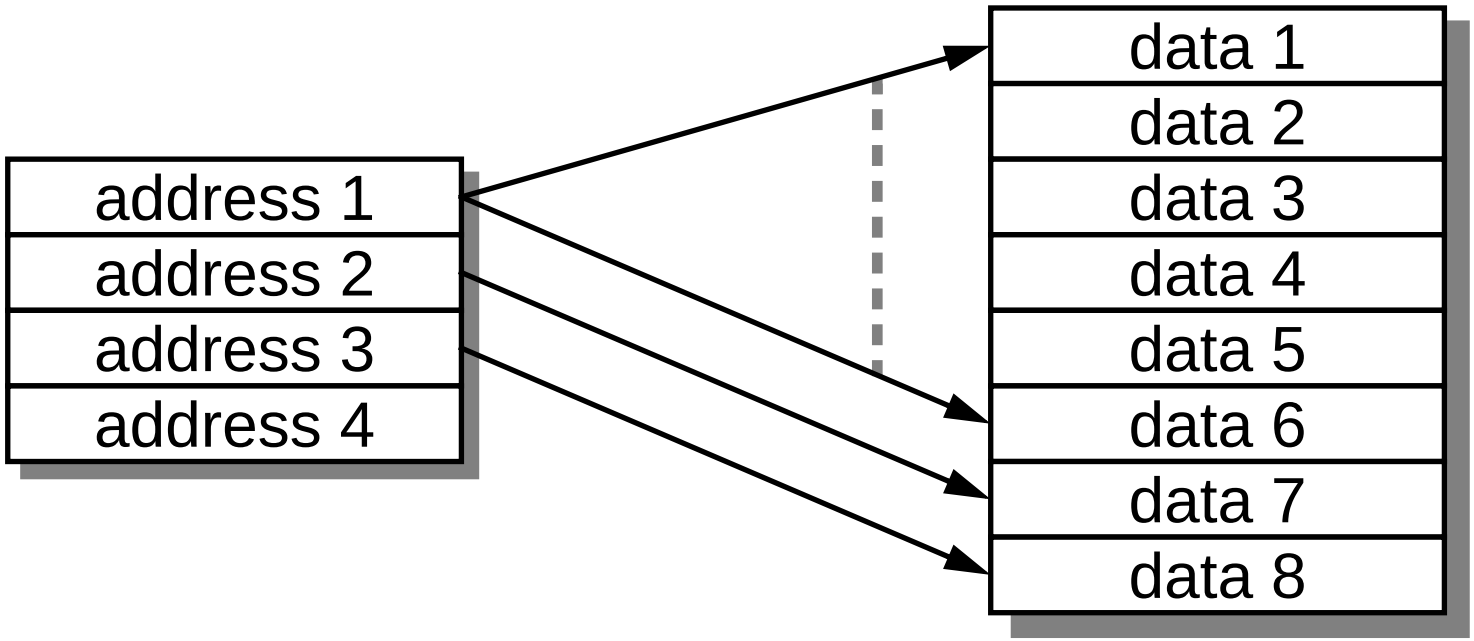
ARM740T organization



The ARM7x0T cache organization



The ARM7x0T write buffer



- One address can be associated with several data elements
  - accommodates STM

Characteristics

- ARM710T, 720T:

Process 0.35 µm	Transistors N/A	MIPS 53
Metal layers 3	Core area 11.7 mm^2	Power 240 mW
Vdd 3.3V	Clock 0 to 59 MHz	MIPS/W 220

- ARM740T:

Process 0.35 um	Transistors N/A	MIPS 53
Metal layers 3	Core area 9.8 mm^2	Power 175 mW
Vdd 3.3V	Clock 0 to 59 MHz	MIPS/W 300

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StrongARM

- Developed by Digital
  - in collaboration with ARM Ltd; later bought by Intel
- Featured:
  - 5-stage pipeline
  - 16 Kbyte I cache, 16 Kbyte D cache
    - both 32-way associative, 8 word line
  - high clock rate
  - low power consumption
    - due to low voltage (down to 1.5 V) operation

Now obsolete but demonstrated that ARMs need not be slow!

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ARM920T

- The ARM920T is …
  - an ARM9TDMI processor core, with:
    - a **16** Kbyte instruction cache
      - 64-way associative, 8 words/line
    - a **16** Kbyte copy-back data cache
      - 64-way associative, 8 words/line
    - an AMBA interface
      - shared by instruction and data ports
    - an 8 word, 4 address write buffer
    - an **MMU** with a 64-entry TLB
    - CP14 debug coprocessor

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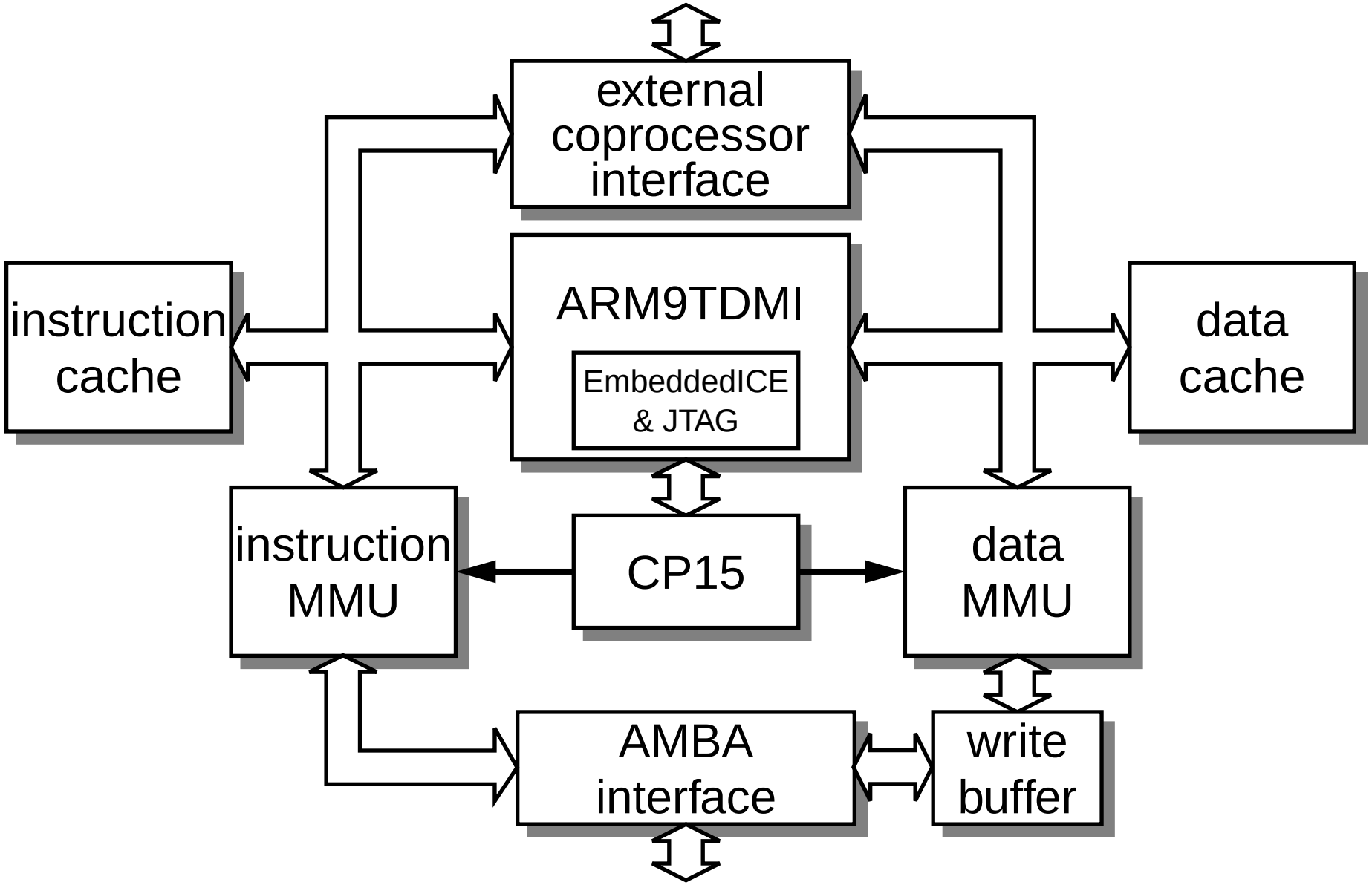
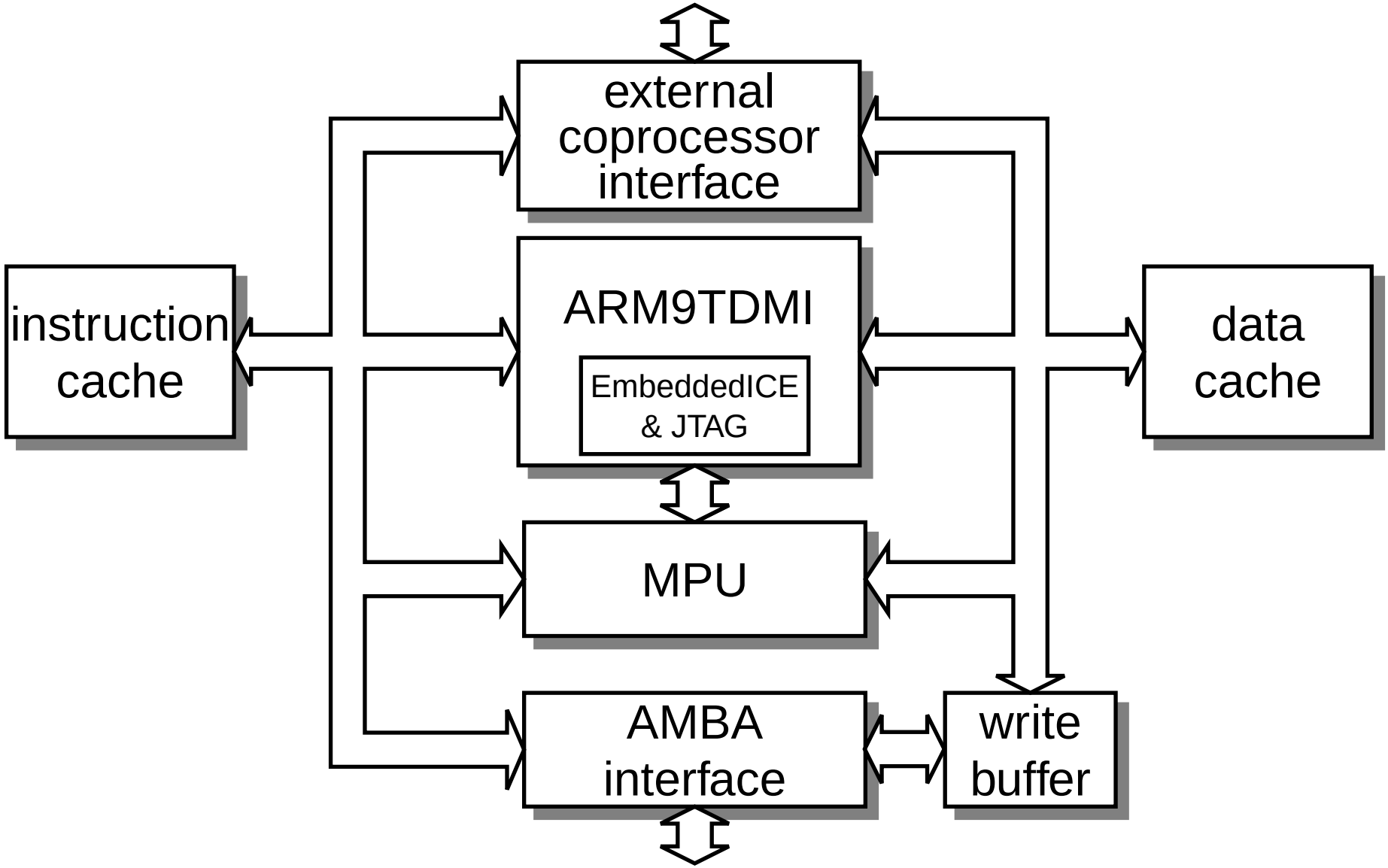
ARM940T

- The ARM940T is …
  - an ARM9TDMI processor core, with:
    - a **4** Kbyte instruction cache
      - smaller, but otherwise similar to ARM920T
    - a **4** Kbyte copy-back data cache
    - an AMBA interface
      - shared by instruction and data ports
    - an 8 word, 4 address write buffer
    - a simple **memory protection unit**
      - there is no address translation system
    - CP14 debug coprocessor

ARM920T organization



ARM940T organization



Characteristics

- ARM920T:

Process 0.25 µm	Transistors 2,500,000	MIPS 220
Metal layers 4	Core area 23-25 mm^2	Power 560 mW
Vdd 2.5V	Clock 0 to 200 MHz	MIPS/W 390

- ARM940T:

Process 0.25 µm	Transistors 802,000	MIPS 220
Metal layers 3	Core area 8.1 mm^2	Power 385 mW
Vdd 2.5V	Clock 0 to 200 MHz	MIPS/W 570

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ARM1020E

- A CPU macrocell based on the ARM10TDMI
  - 32 Kbyte 64-bit I- and copy-back D-caches
    - 64-way associative, 8 words/line
  - AMBA AHB bus interface
  - < … list of other things assumed …>

- ARM1020E target characteristics:

Process 0.18 µm	Transistors 7,000,000	MIPS 500
Metal layers 5	Core area 12 mm^2	Power 400 mW
Vdd 1.5V	Clock 0 to 400 MHz	MIPS/W 1250

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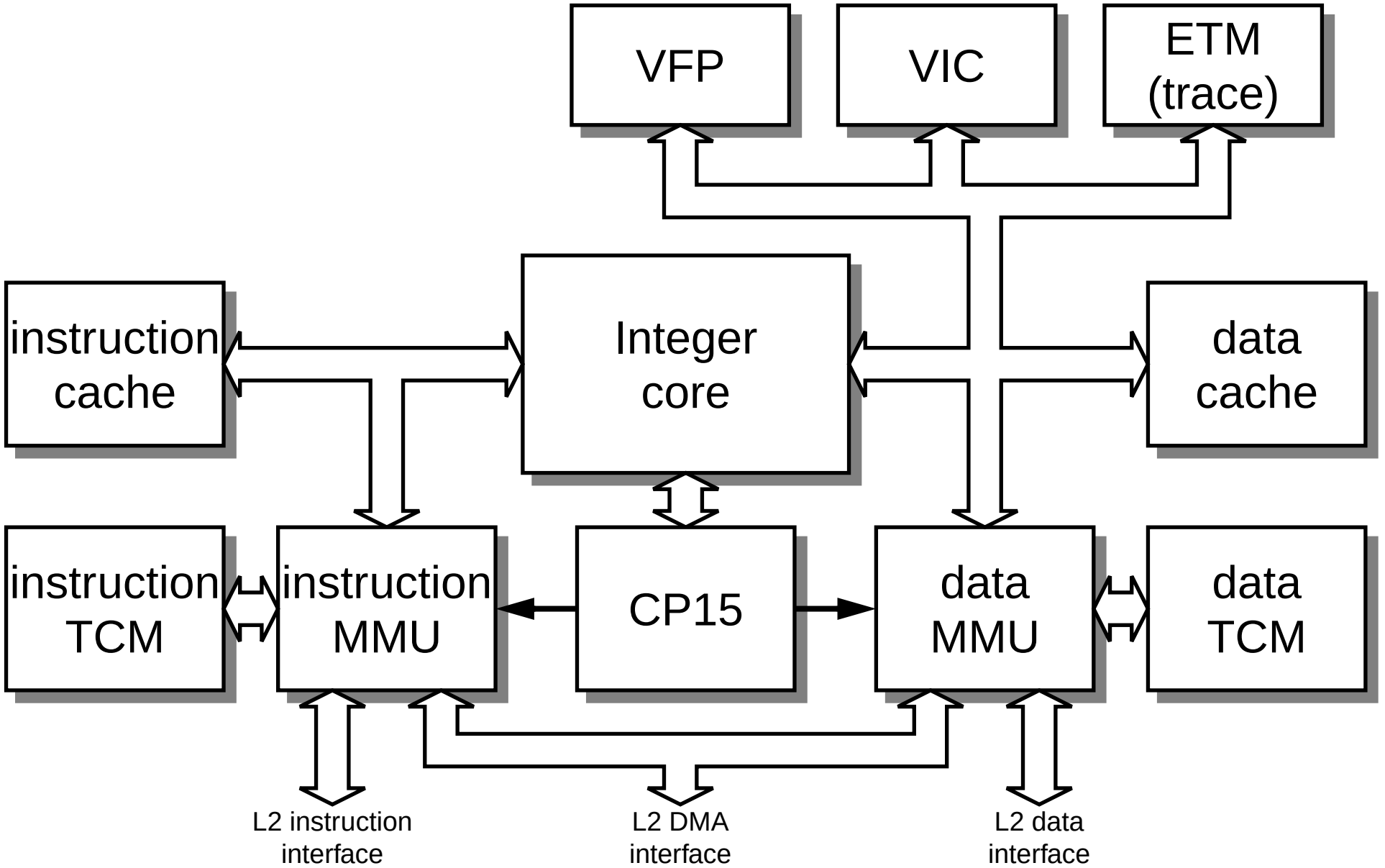
ARM1176JZF


VFP
VIC
ETM (trace)
instruction cache
Integer core
data cache
instruction TCM
instruction MMU
CP15
data MMU
data TCM
L2 instruction interface
L2 DMA interface
L2 data interface

ARM1176JZF

- ARM11 processor core
  - separate instruction and data buses
  - EmbeddedICE
  - debug coprocessor (CP14)
- Instruction and data MMUs
  - two-level TLB
- Vector floating point coprocessor
- Vectored interrupt controller
- Embedded trace

ARM1176JZF

- Up to 64 Kbytes of L1 instruction and data caches
  - 64-bit wide interface
  - 4-way set-associative (less than previous ARMs)
  - 8 words/line
  - write through or copy back
  - pseudo-random or round-robin replacement
  - lockdown – each ‘way’ can be locked
  - sequential access mode (to save power)

ARM1176JZF

- Tightly coupled memory (TCM)
  - configuration of part/all of cache memory {4, 8, 16, 32, 64KB}
  - physically addressed
  - supported by internal DMA
    - 2 channels (only one active at once)
    - fast transfer between TCM and memory (*not* L1 cache)

XScale® features

- An ARM v5TE implementation designed by Intel
  - "7-8 stage Superpipelined RISC"
- Some additional features:
  - a DSP coprocessor (CP0)
    - contains a 40-bit accumulator
    - eight new instructions.
  - new page attributes
  - coprocessor 15 additional functionality
  - coprocessor 14 (performance monitoring/software debug)

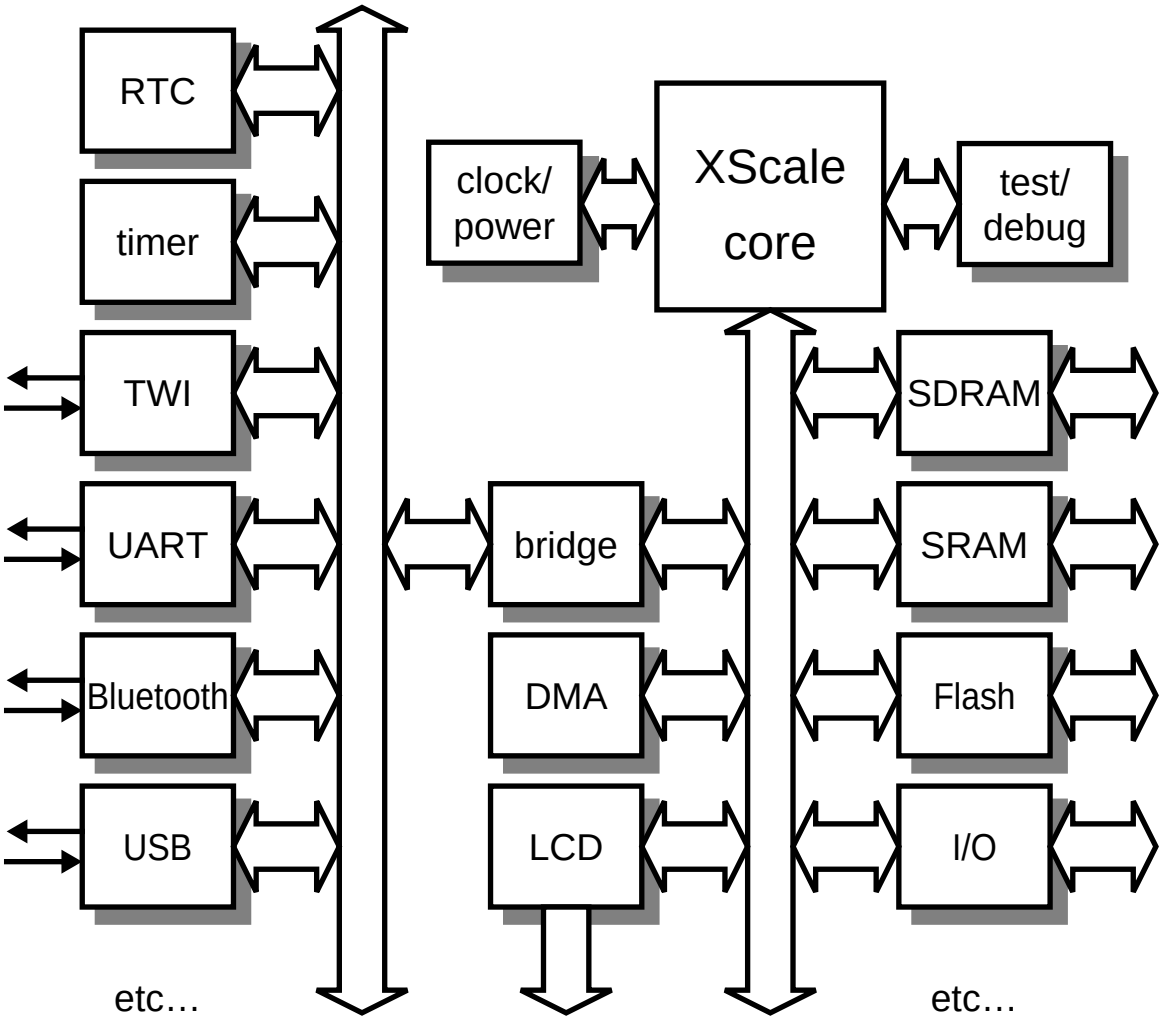
XScale® features

- ARM v5TE (plus extensions)
  - dynamic voltage/frequency scaling
  - multiply-accumulate coprocessor
  - 128-entry static 2-level BTB
  - 32 KB instruction cache
  - 32 KB data cache
    - 2 KB mini-data cache
    - hit-under-miss operation with data caches
  - performance monitoring unit
    - two 32-bit event counters
    - one 32-bit cycle counter
  - debug unit trace buffer

Some XScale variants

- PXA255
  - 32KB data and instruction caches
    - plus 2KB ‘mini data cache’
  - 200MHz - 400 MHz
  - SDRAM/Flash interfaces
  - I/O
    - USB client
    - 1.84MHz cellular interface
    - PCMCIA controller
    - etc.

PXA255


RTC
timer
TWI
UART
Bluetooth
USB
etc…
clock/ power
XScale core
test/ debug
bridge
DMA
LCD
SDRAM
SRAM
Flash
I/O
etc…

Some XScale variants

- PXA27x
  - PXA270 – up to 624 MHz
  - PXA271 – 32MB Flash – 32MB SDRAM – 416MHz
  - PXA272 – 64MB – up to 520MHz
    - stacked, multichip modules
  - Wireless MMX
  - lots of peripherals
    - clearly aimed at telephone/PDA applications

XScale DSP extensions

- DSP coprocessor (CP0)
  - separate multiply accumulate with 40-bit accumulator
- Wireless MMX
  - 43 new SIMD instructions
  - 64-bit datapath
  - for “multimedia” and games

Different evolutionary path from ARM Ltd.

Dynamic voltage/ frequency scaling

- In CMOS:
  - speed is *roughly* proportional to supply voltage
  - power consumption is *roughly* proportional to supply voltage *squared*
    - therefore a lower supply voltage gives **better energy efficiency**
- Xscale exploits this:

Clock frequency	"MIPS"	Power (mW)	MIPS/W
150MHz	185	40	4600
600MHz	750	450	1700
800MHz	1000	900	1100

Discussion

- Speed needs memory bandwidth:
  - single 32-bit I/D cache on ARM7x0T
  - split 32-bit I- & D-caches on ARM9x0T
  - split 64-bit I- & D-caches on ARM1020E
  - split 64-bit I- & D-caches on ARM1176JFZ
    - plus provision for split L2 cache
- Memory management is high cost
  - greater silicon area
  - protection unit on ARMx40T is cheaper

Discussion

- Cache & TLB lock-down helps real-time operation
  - easier to support with CAM-RAM cache
  - TCM aids performance *predictability*
    - enhanced by DMA
- Many parts now highly integrated
- Can trade ultimate performance for *energy* efficiency
  - XScale

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Hands-on: code profiling

- Investigate the profiling facilities in the ARM toolkit
  - see what proportion of time a program spends in different routines

  - ☞ Follow the ‘Hands-on’ instructions