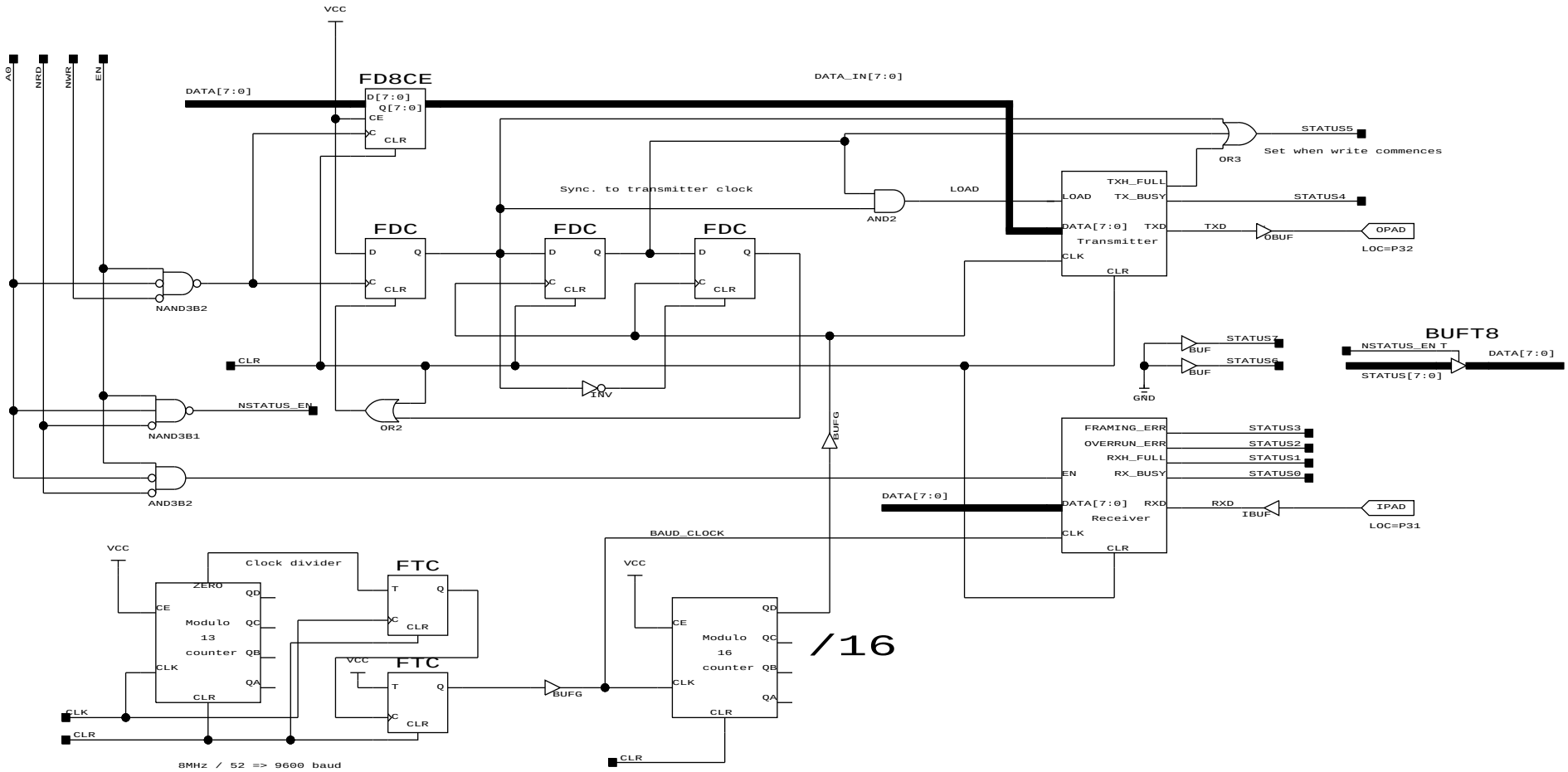
VCC
A0
NRD
NWR
EN
DATA[7:0]
FD8CE
D[7:0]
Q[7:0]
CE
C
CLR
DATA_IN[7:0]
STATUS5
OR3
Set when write commences
Sync. to transmitter clock
LOAD
AND2
TXH_FULL
LOAD
TX_BUSY
STATUS4
DATA[7:0]
TXD
Transmitter
CLK
CLR
TXD
OBUF
OPAD
LOC=P32
FDC
D
Q
C
CLR
NAND3B2
CLR
INV
STATUS7
BUF
STATUS6
BUF
GND
BUFT8
NSTATUS_EN T
DATA[7:0]
STATUS[7:0]
NSTATUS_EN
OR2
NAND3B1
BUFG
FRAMING_ERR
OVERRUN_ERR
RXH_FULL
RX_BUSY
STATUS3
STATUS2
STATUS1
STATUS0
EN
AND3B2
DATA[7:0]
DATA[7:0]
RXD
Receiver
RXD
IBUF
IPAD
LOC=P31
BAUD_CLOCK
VCC
Clock divider
FTC
T
Q
ZERO
QD
CE
Modulo
13
counter
QC
QB
QA
CLK
CLR
VCC
FTC
T
Q
C
CLR
BUFG
VCC
QD
CE
Modulo
16
counter
QC
QB
QA
CLK
CLR
/16
CLK
CLR
CLR
8MHz / 52 => 9600 baud