3.0 Simulating the design

The simulation routine is the same as it was in the Register Transfer Level design (CADEN-3 section 8-15). However there are two differences that you must note.

- Use a different Run Directory than the one you used in the Register Transfer Level design. e.g. verilog.run2
- Change the Netlisting Options so that it does not look at the Functional descriptions. Click on ***Sessions->Options->Netlisting*** to bring up the Netlist options form. Then delete ***functional*** from the ***View List***.

Remember:

First

Simulate the synthesized blocks independently.

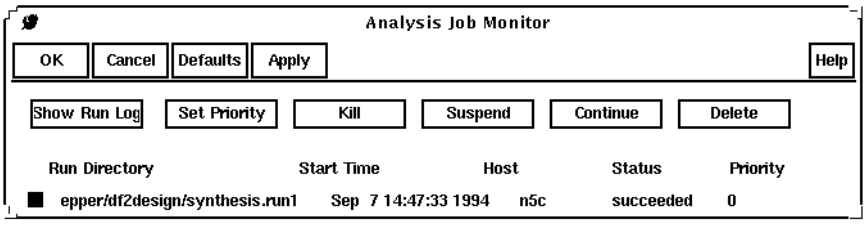
Then

Simulate the whole gate level design.

2.14 Click ***OK***.

The synthesis software may take sometime to load. ***WAIT*** until the cursor becomes an arrow in the CIW window.

2.15 Click on ***Session->Job Monitor*** in the HDL Synthesizer window.



The Job Monitor shows the ***Status*** of the synthesis tool.
Wait until the ***Status*** has changed from ***running*** to ***succeeded***.

If the Status changes to failed, ask for help from a demonstrator.

2.16 Click ***OK*** in the ***Job Monitor*** window.

2.17 Click ***Show->Output->Schematic*** in the ***HDL Synthesizer and Optimizer***window.

Examine the schematic view. Close the schematic window.

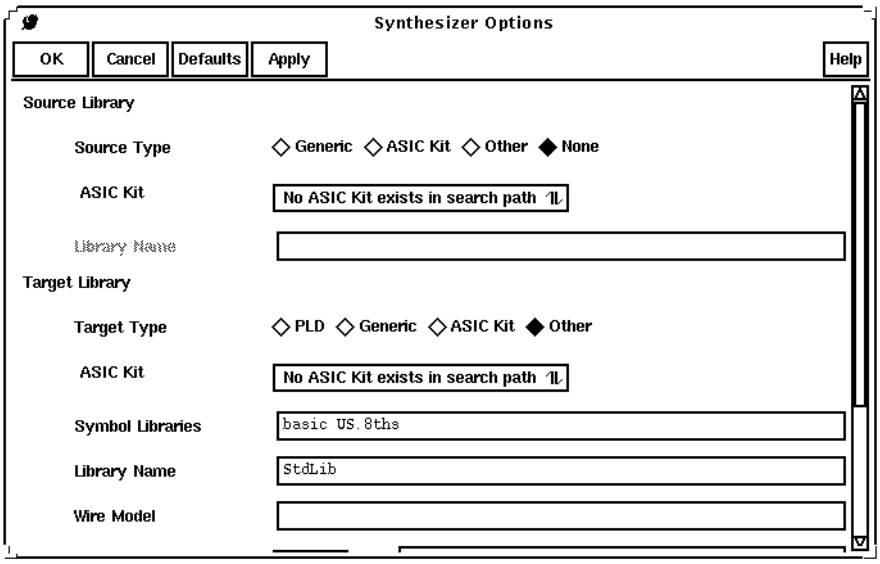
You now have to copy the ***schematic*** of the synthesized cell from the library ***Opt*** to your design library. Refer back to CADEN-1 page 10 for copying cell views.

DO NOT COPY THE SYMBOL FROM THE LIBRARY Opt

2.18 Click ***Session->Quit*** in the ***HDL Synthesizer and Optimizer*** window.

2.19 Click ***OK*** in the pop up window.

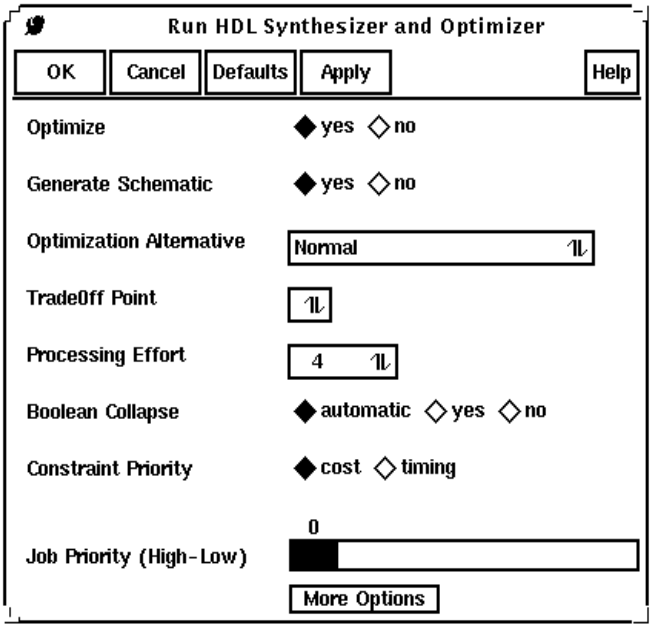
In a unix window you need to remove the synthesis run directory
e.g. ***/bin/rm -r ~/df2design/synthesis.fsm1***

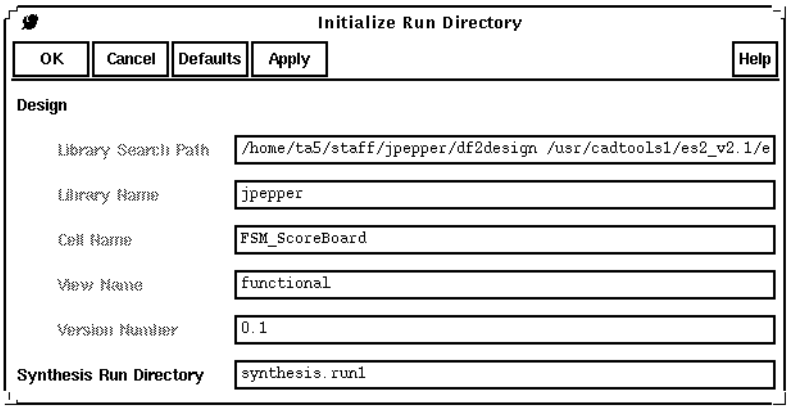


2.11 Enter ***StdLib*** in the ***Library Name*** option.

2.12 Click ***OK*** at the top of the options form.

2.13 Click on ***Run->Synthesizer*** in the ***HDL Synthesizer and Optimizer***. The ***Synthesis Run Options*** form appears. Set the options as below.

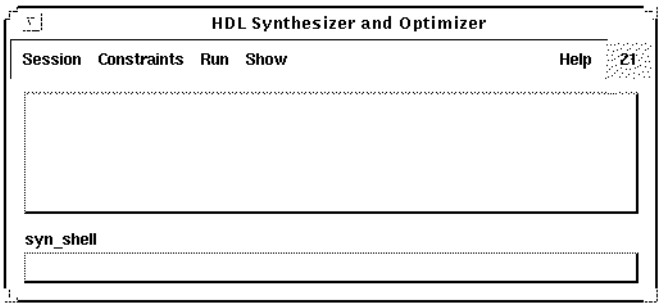




2.8 Enter a Synthesis Run Directory. Change the default directory so that you use a different name for each instance e.g. synthesis.fsm1. (Using the same name repeatedly can cause problems and confusion).

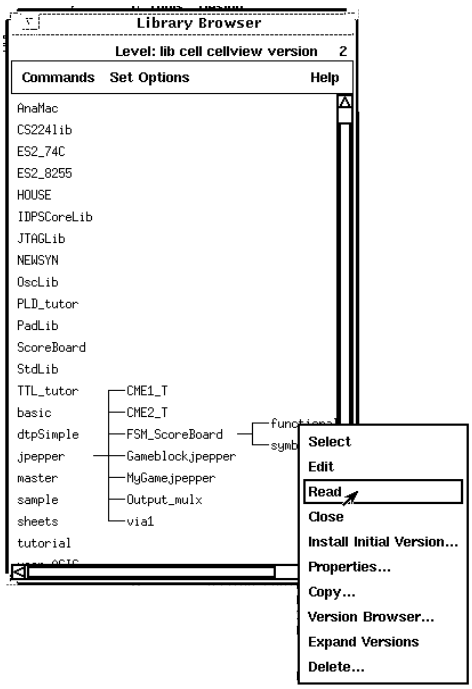
2.9 Click on ***OK.***

The HDL Synthesizer and Optimizer window now appears.This enables you to interact with the synthesis tool.



2.10 In the ***HDL Synthesizer and Optimizer*** click on ***Session->Options->Synthesis Library...***

The following options form appears.



The functional description of the cell should appear with a menu banner at the top. In the menu banner there should be ***Tools*** and ***Design.*** If you get a functional description in a textedit window, you have selected the ***Edit*** option. If this is the case quit the textedit and start again

2.7 Click on ***Tools->Design Synthesis->HDL Synthesizer*** on the menu banner.

The ***Synthesis Initialization*** form appears. This form asks you to specify the ***Synthesis Run Directory.***

Gate level design using HDL Synthesis

1.0 Introduction

The purpose of this walkthrough is to describe how a Gate Level design is implemented starting from a Register Transfer Level design. The schematics of the blocks are created by synthesis from Verilog Functional descriptions, using ES2 library components.The main steps are as follows:

- Synthesise Gate Level designs of the FSM and multiplexer block using the Cadence HDL Synthesizer.
- Simulate each of the synthesised blocks using the Verilog-XL simulator and test patterns developed for the Register Transfer Level design.
- Simulate the whole design, again using the test patterns developed for the Register Transfer Level design.

The simulation at this stage will include realistic gate delays which are not incorporated in the Register Transfer Level functional models. It is therefore possible that if the Register Transfer Level was marginal with respect to timing it will no longer work and design modification will be necessary.

The gate level design of the library blocks already exists. They can be viewed using ***descend->read***.

2.0 Synthesis

Synthesize the FSM and multiplexer as follows.

2.1 Click on ***Design Manager->Library Browser*** on the CIW menu banner.

2.2 Click on your design library.

2.3 Click on the cell you wish to synthesize.

2.4 Move the cursor onto the ***functional*** view of the cell**.**

2.5 Hold down the middle mouse button to pop up the functional menu.

2.6 Slide the mouse to the ***Read*** option and release the mouse button.