Placement and Routing

1.0 Introduction

The purpose of this walkthrough is to describe how a gate level design is placed and routed. In principle, once in this form the design can be sent off to a foundry to be fabricated. In practice there are a number of further verification and checking steps not described here, before the design can be fabricated. The main steps are as follows:

- Adding pads to the design. The pads are basically the connection between the design and the outside world, like the metal legs on a chip package.

- Placement of the design. This involves laying down all the gates required by the design ready to be wired up in the next stage.

- Routing the design. This is where all the gates are automatically wired together to complete the design.

- Layout statistics. Here you will extract some detailed information from the completed layout. In particular the track capacitances/resistances.

- The final stages of preparation for fabrication, including post-layout simulation, are described in ES2 Cadence Design Kit User Guide.

The Place and Route procedure consists of a large number of consecutive steps. For small designs it is sufficient to use default decision setting; this approach has been adopted here. To succeed, follow the steps exactly without worrying too much what they are doing.
Final year project students may wish to consult the full Cadence manuals.

2.0 Adding Pads

In this section you will create a new schematic containing the ***Gameblock<group-name>*** symbol with the pads connecting to it.

2.1 Create a new cell with a schematic view for your design.
e.g.

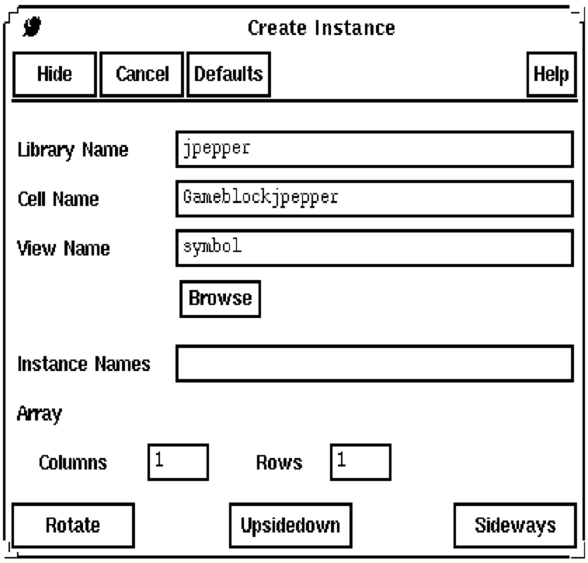
Library Name jpepper
Cell Name IN_OUT_LEVEL
View Name schematic

(Refer back to CADEN-2 page 3 if you are unsure how to create a cell)

2.2 Open the above schematic view.

2.3 Click ***Create->Instance*** option on the schematic menu banner.
The ***Create Instance*** form appears.

2.4 Fill in the form as shown below but with your design library name and place the ***Gameblock<groupname>*** symbol.



Once you have placed the Gameblock symbol you enter all the input, output, and supply pads.

2.5 Fill in the Create Instance form with:
Library Name PadLib
Cell Name LIBIPS8B

LIBIPS8B is a cmos input buffer pad.

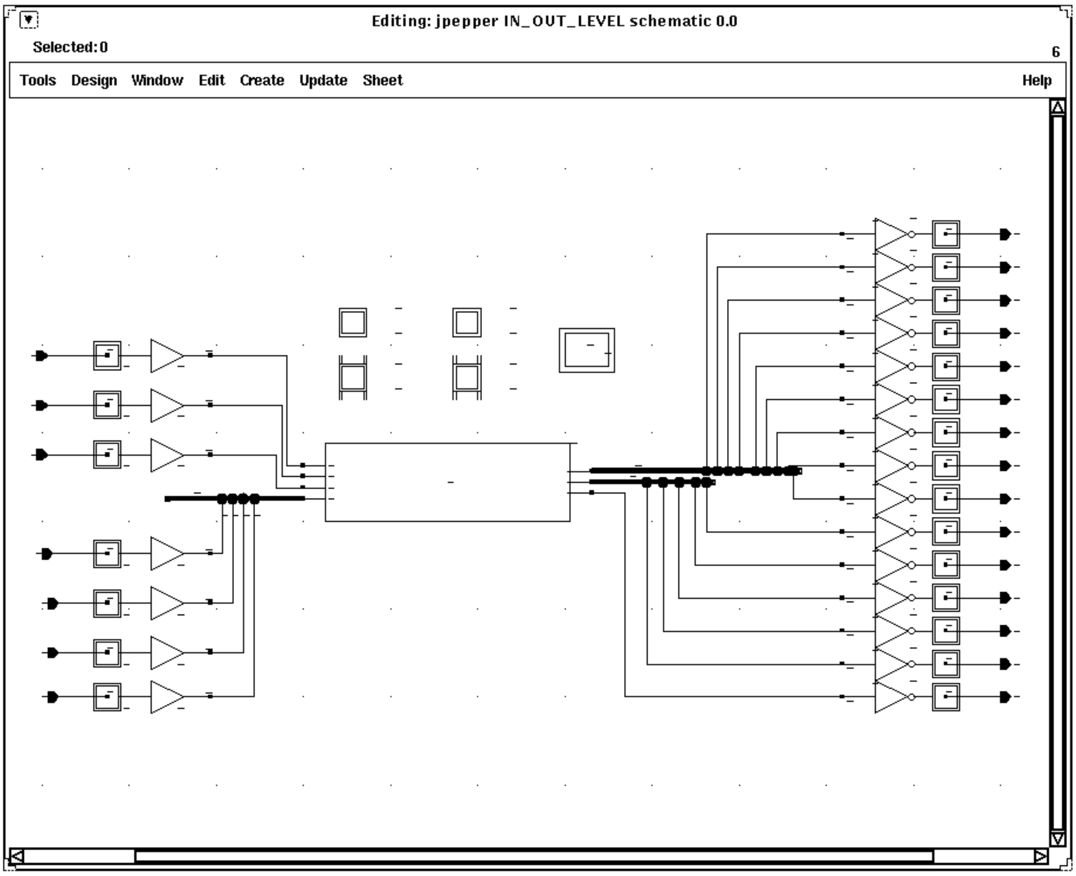
2.6 Place the instance.

Repeat section 2.5 to 2.6 but replace the Cell Name with the following:

LIBOPS0U - output pad 2mA drive
LIBGNDCO - ground pad for core design
LIBGNDPY - ground pad for periphery i.e. input/output cells
LIBPWRCO - power pad for core
LIBPWRPY - power pad for periphery
LIBTOPNETS - dummy cell needed by the software

2.7 Click ***Cancel*** on the Create Instance form.
You will require 7 input pads(LIBIPS8B) and 15 output pads(LIBOPS0U).
Use the copy command in the schematic window to generate these.
(Refer to CADEN-1 page 13 on how to copy an object).

2.8 Connect the schematic as shown below.



2.9 Check and Save the design.

3.0 Flattening the Netlist

Before a design can be placed and routed a flattened representation of the hierarchical netlist needs to be obtained. The following steps flattens the netlist and generates an AutoLayout representation for physical design.

3.1 Click ***Tools->Floorplan/Schematics*** to obtain the correct menu.

3.2 Click ***Floorplan->Hierarchy Browser*** to bring up the hierarchy fill form.

3.3 Click ***OK***.

The Hierarchy Browser Window now appears.

3.4 Click the left mouse button on the top level design block. It should change colour.

3.5 Click ***Hierarchy->Generate Physical Hierarchy*** in the ***Hierarchy Browser***

The generation of the autoLayout view is a non-interactive process.Wait until it has completed.

3.6 Close the ***Hierarchy Browser*** and ***schematic*** windows.

4.0 Placement

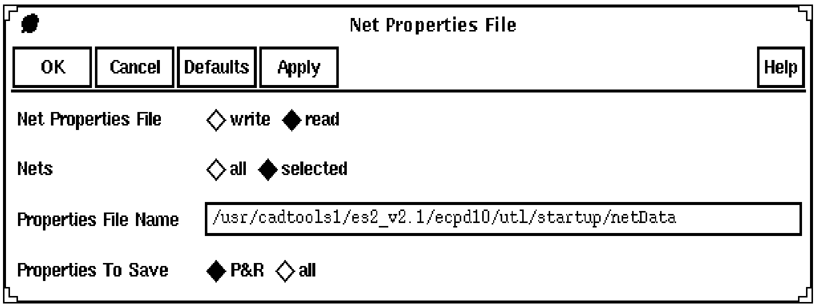
4.1 Open your top level design in the normal method but use View Name ***autoLayout***.

4.2 Activate the Place and Route tools by: click ***Tools->Floorplan/P&R->Cell Ensemble.***

You now have to allocate net priorities for your design.

4.3 Click ***Route->Modify Net->Net Properties File***.

Fill in the form as shown below.



4.4 Click ***OK***.

Now initialise the floorplan. This creates regions for the pad ring and core array.

4.5 Click ***Floorplan-> Initialise Floorplan***.

4.6 Click ***OK*** on the fill form.

4.7 Click ***Window->Fit*** to show the regions and the cells.

At this stage, all cells are unplaced. You now have to place them.

5.0 Placement of a design without Complied Megacells

5.1 Click ***Place->Automatic*** a placement fillform appears.

Fill in the form as follows:-

Method ***both***

Insert Feedthru ***on***

Feedthru Library Name ***StdLib***

Feedthru Master Name ***LIBFEED***

Feedthru Master View ***abstract***

5.2 Click the ***Initial Options*** form.

5.3 Set the ***Placement Snap Grid*** to ***0.125***.

5.4 Click ***OK*** on the ***Initial Placement*** form.

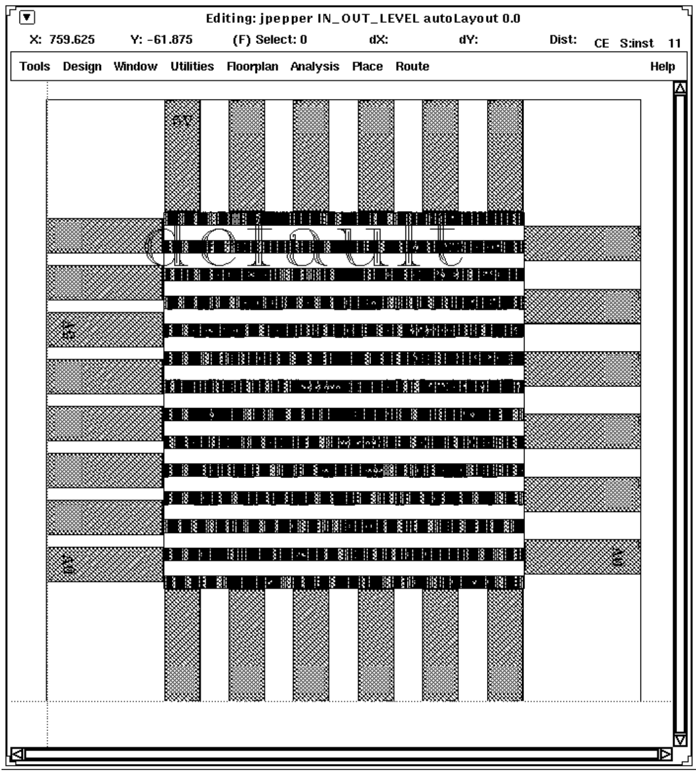
5.5 Click ***OK*** on the ***Automatic Placement*** form.

The placement software places all the unplaced cells, including the pad cells.

This will take some time. ***Wait.***

A message in the CIW appears informing you that the placement is complete. The number of cells contained in your design is also shown at this stage, in the CIW.

5.6 Click ***Window->Fit***.



The pad ring needs to be completed by the addition of corner cells which carry power and ground rails around the corners.

5.7 Click ***Place->IO Commands->Add Corners***.

5.8 Fill in the form as follows:-

Glue Cell Library Name ***PadLib***

Glue Cell Master Name ***LIBCORNER LIBCORNER LIBCORNER LIB-CORNER***

5.9 Click ***OK*** on the form.

The I/O cells now need justifying.

5.10 Click ***Place->I/O Commands->Justify***.

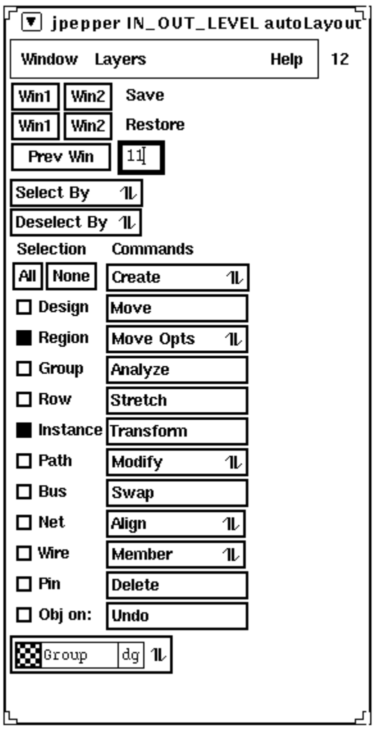
5.11 Click ***OK*** on the fillform.

5.12 Click ***Window->Fit***.

The rows of cells within the core of the design require terminating.

5.13 Click ***Utilities->Command Toolbox...***

5.14 Click on ***Region*** in the ***Command Toolbox*** to allow selection of regions.



5.15 Click the left mouse button in the core region, being careful not to have the pointer on a cell.This should select the region.

5.16 Click ***Place->Glue Cell->Add*** - fill in the form with the following values.

Glue Cell Type ***cap***

Glue Cell Library Name ***StdLib***

Glue Cell Master Name ***LIBLCAP***

Glue Cell Master View ***abstract***

5.17 Click ***Cap Cell*** on the fillform.

5.18 Set row position to ***left.***

5.19 Click OK on the ***Cap Cell Option*** form.

5.20 Click OK on the Add Glue Cell form.

This operation terminated the lefthand core cells.

Repeat steps 5.16 to 5.20 using ***LIBRCAP*** and ***right*** to terminate the righthand core cells.

It is now necessary to place every cell on the grid.

5.21 Make sure that ***Instance*** is selected on the ***Command Toolbox***.

5.22 In the ***Command Toolbox*** click ***Select By->All***.

5.23 In the ***Layout Window*** click ***Place->Snap to Grid...***

Fill in the form as follows:

Placement Snap Grid ***0.125***.

5.24 Click ***OK***.

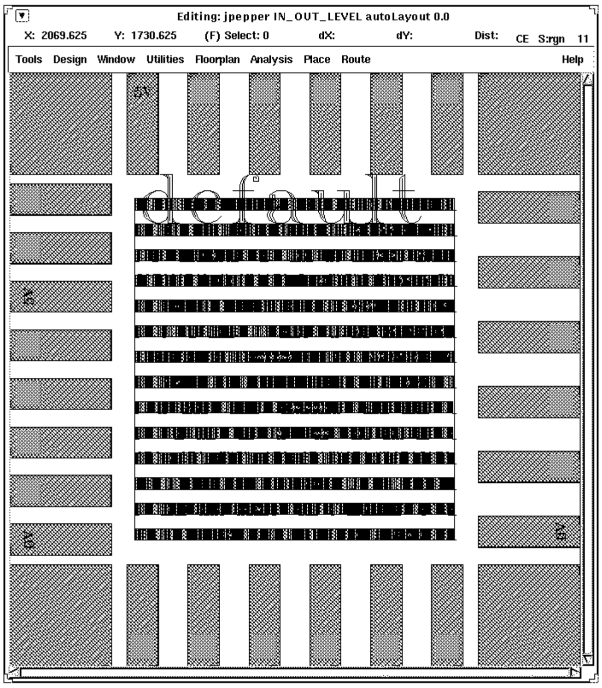
You have now placed the design. It is best to save the design at this stage.

5.25 Click ***Design->Save As...***

5.26 Fill in the form with View Name value ***placed***.

5.27 Click ***OK***.

An example placed design is shown below.



6.0 Routing a design

6.1 In the ***Command Toolbox*** click ***Deselect By->All***.

6.2 Click on ***Instance*** in the ***Command Toolbox*** to deactivate it.

6.3 Click middle mouse button on the placement region to select it.

6.4 Click ***Delete*** in the ***Command Toolbox***.

You now have to create channels to allow your design to be routed.

6.5 Click ***Route->Channels->Create...***

6.6 Click ***OK*** on the fill form.

Now you have to do a Global Route.

6.7 Click ***Route->Global-> Automatic...***

6.8 Click on the ***Optimizer Options*** on the ***Global Route Method*** form.

6.9 Fill in the following values on the ***Global Route Optimizer*** form:
Feedthru Library Name ***StdLib***
Feedthru Master Name ***LIBFEED***

Feedthru Master View ***abstract***

6.10 Click ***OK*** on the ***Global Route Optimizer*** form.

6.11 Click ***OK*** on the ***Global Route Method*** form.

The next stage is Detailed Routing.

6.12 Click ***Route->Detail->Automatic...***

6.13 Click ***OK*** on the ***Route and Compact All Channels*** form.

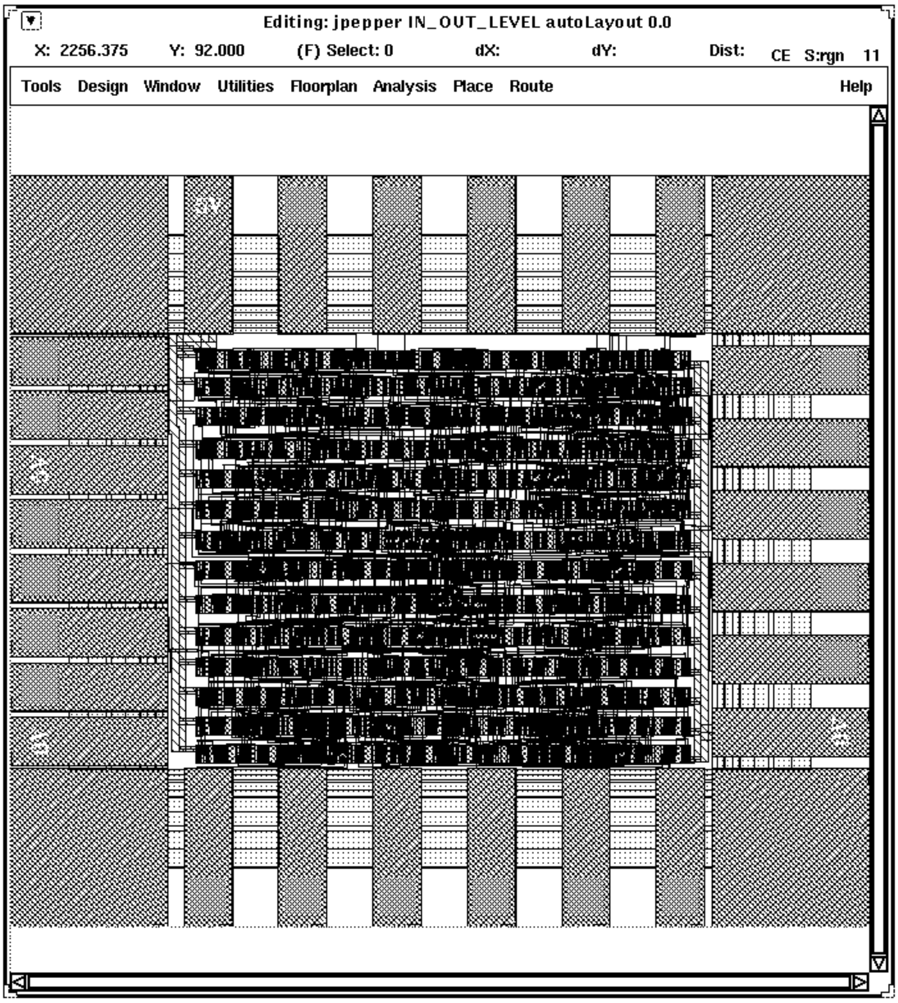
The routing software should now route your design.

6.14 Click ***Design->Save As...***

6.15 Fill in the ***View Name*** as ***routed***.

6.16 Click ***OK***.

An example routed design is shown below.

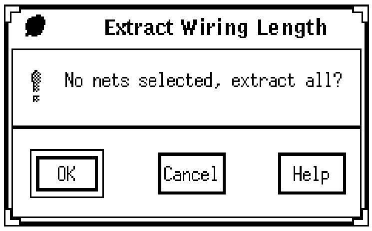


7.0 Layout Statistics

Extracting Capacitance

7.1 In the CIW type ES2capExtract.

The following form appears:



7.2 Click ***OK***.

7.3 Fill in the form as follows:

File Name ***pr.cap***

Extract select ***capacitance***

7.4 Click ***OK***.

Extracting Resistance

7.5 For extracting resistances, repeat steps 7.1 and 7.2

7.6 Fill in the form as follows:

File Name ***pr.res***

Extract select ***resistance***

7.7 Click ***OK***.

Extracting Length

7.8 For extracting lengths, repeat steps 7.1 and 7.2

7.9 Fill in the form as follows:

File Name ***pr.len***

Extract select ***length***

7.10 Click ***OK***.

The files are saved in your df2design directory, and may be viewed using a text editor.

7.11 To obtain the dimensions of your chip, use the mouse pointer. Point to the bottom left corner and note the coordinates, now point to the top right corner and note the coordinates.Subtracte one set of coordinates from the other and the result is the dimensions of the chip.