

Maintaining Real-Time Synchrony on SpiNNaker

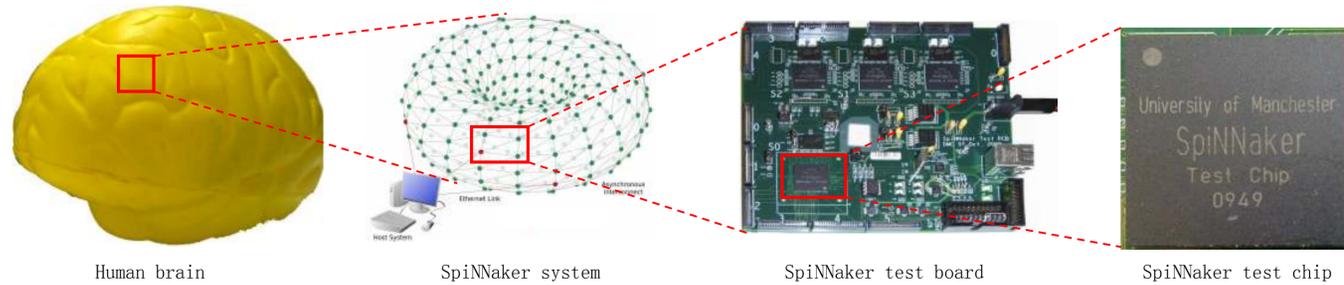
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SpiNNaker system details

SpiNNaker

Optimised custom-designed integrated circuit inspired by the biological functions of the human brain.



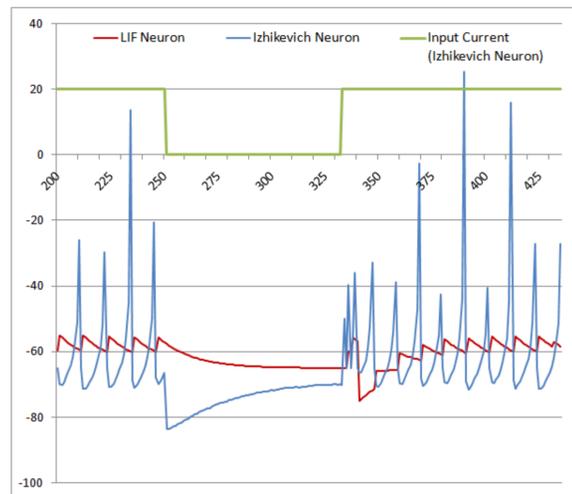
- 65,000+ SpiNNaker chips;
- Each chip contains 18 ARM9 cores each simulating ~1,000 neurons (2 ARM9 cores in the test chip);
- Total: 1 billion+ neurons;
- SpiNNaker system is able to simulate ~1% of the brain.

Features of SpiNNaker chip

SpiNNaker mimics the brain in numerous ways:

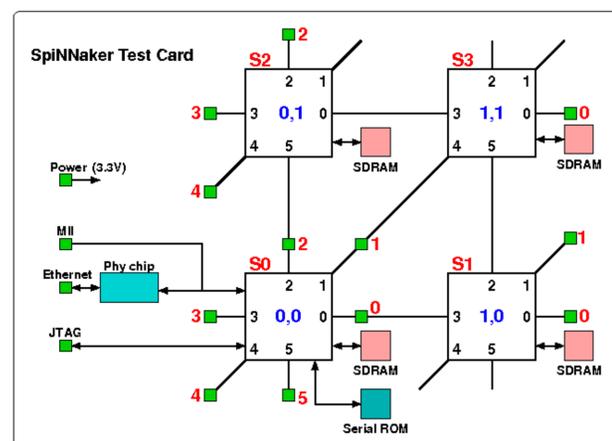
- Resilient to individual component failure;
- Maximum power efficiency;
- Asynchronous event based communication;
- High performance through many small elements.

Neural simulation



- Ability to simulate one neuron type per core
- Neuron types can be different across multiple cores in the system during the same simulation

Test board schematic

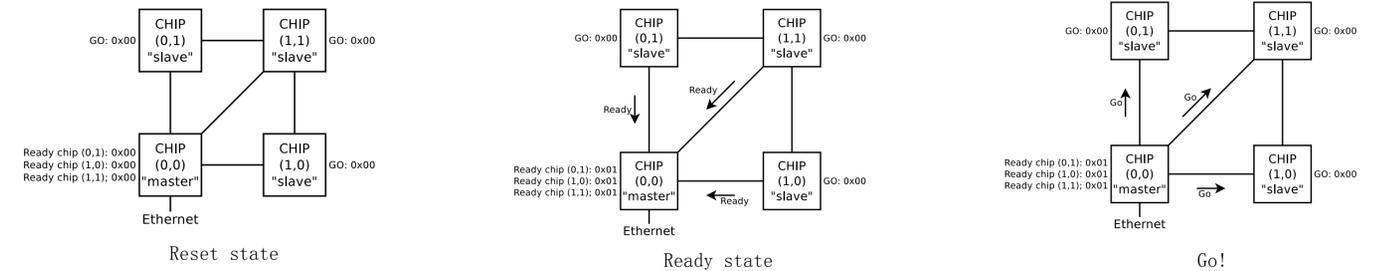


- Each green dot represents an external connection

Synchronization details

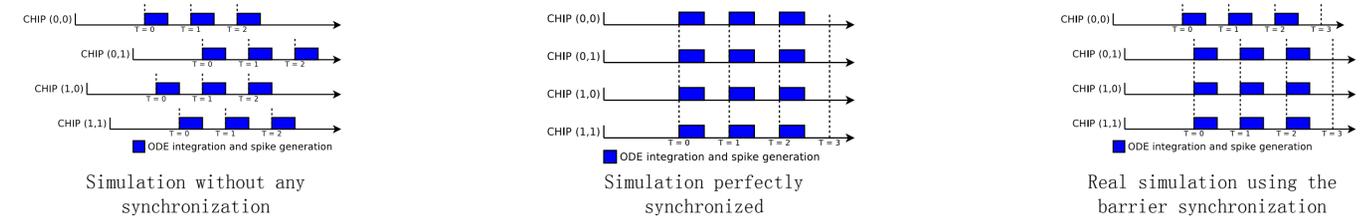
Barrier synchronization

- A three-step synchronization procedure (for multiple chip simulations):

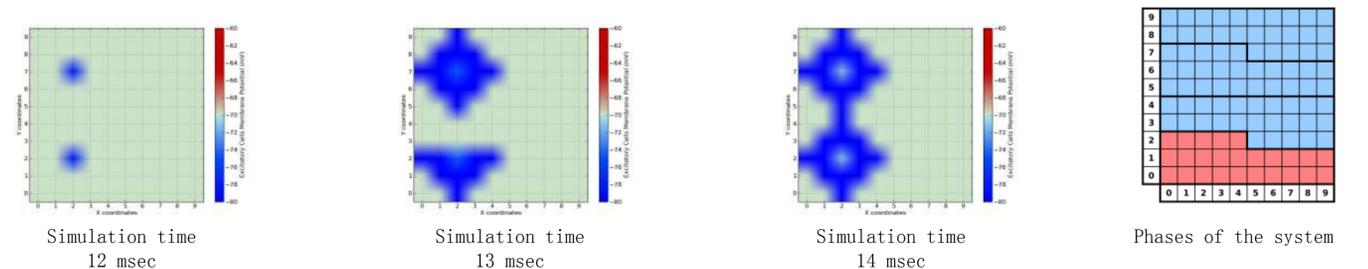


Simulation timing

- Evolution of the simulation on multiple chips

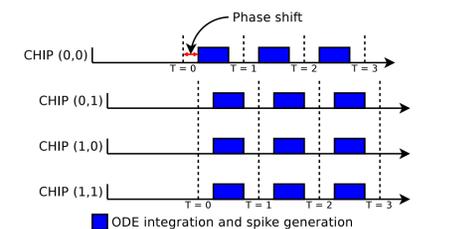


- Examples of simulation running on the SpiNNaker system with the slight de-synchronization.



Phase shifting

- Phase shifting technique to solve the de-synchronization problem;
- Available computation time reduced by this technique;
- The neural simulation is memory bounded (not CPU bounded), so this does not influence the amount of neurons that each core can simulate



Further Information

SpiNNaker website: <http://apt.cs.man.ac.uk/projects/SpiNNaker/>
 Sergio Davies' webpage: <http://apt.cs.man.ac.uk/people/davies/>

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