MAHDI JELODARI MAMAGHANI

IT302 - School of Computer Science
The University of Manchester
M13 9PL, Manchester, UK

Email: m.j.1989@ieee.org
URL: http://apt.cs.manchester.ac.uk/people/mamagham/
Phone: (161) 275-6202/0697

EPSRC Doctoral Prize Fellow hosted by the University of Manchester under Prof. Steve Furber, CBE.
Research Scholar at the University of Southern California under Prof. Peter Beerel.

RESEARCH INTERESTS

Energy Efficient Computing and Synthesis
Hardware/Software Co-Design and Heterogeneous Synthesis
CAD/EDA for Integrated Synchronous-Asynchronous Designs
FPGA-accelerated Hardware Design/Synthesis/Simulation
Globally Asynchronous Locally Synchronous (GALS-SoC) Design

EDUCATION

The University of Manchester, Manchester, UK,
Ph.D., in Computer Science, July 2012 – Feb 2016
Supervisor: Dr. Jim Garside
EPSRC Full Research Scholarship under grant EP/I038306/1
under GAELS (Globally Asynchronous Elastic Logic Synthesis) project
Thesis: High-Level Synthesis of Elasticity: From Models to Circuits

The University of Tehran, Tehran, Iran,
B.Sc., in Computer Engineering - Hardware, Sept 2007 – Feb 2012
Supervisor: Prof. Nasser Yazdani
Thesis: Design and implementation of a high-performance CCMP/GCMP architecture for high-throughput Wireless LANs

National Organisation for Development of Exceptional Talents (NODET), Tabriz, Iran,
Diploma, in Physics and Mathematics, Sept 2003 – July 2007
Examined subjects: Mathematics, Physics, Chemistry, Persian Literature, History and Arabic

HONOURS & AWARDS

EPSRC Doctoral Prize Fellowship 2015/17
UK ICT Pioneers Finalist 2015, October 2015
DATE Best IP Award 2015 sponsored by Cadence, March 2015
DASS scholarship joint with DAC 2013 and **MICRO 2014 Travel Grant**
EPSRC Full Research Scholar Award for 3 years under grant EP/I038306/1, 2012
Among the **top 5%** of the computer engineering students at ECE department of University of Tehran
Innovative Idea Award by the Science & Innovation Park of the University of Tehran for the proposal entitled "*Intelligent Navigation System*", 2011 / patented under (Iran – Patent No. 390070566).
ACM Certificate for presentation on "*Chemical Computing*" in the first seminar of "Models of Computation and Computational Models", ACM Student Chapter of University of Tehran, March 2011
Ranked 634th among 350,000 participants in the nationwide university exam, 2007
Semi-finalist in the Iran National Mathematics Olympiad, 2004

PROFESSIONAL EXPERIENCES

EPSRC Doctoral Prize Fellow, APT group at the University of Manchester, UK, since Dec. 2015.
Research Scholar, CAD/VLSI Lab, University of Southern California, USA, September 2016 -
Visiting Researcher, Computer Laboratory, University of Cambridge, UK, August 2016.
Visiting Researcher, IHP Microelectronics, Frankfurt (oder), Germany, March. 2016.
Co-Founder/Director at Nerabus, Manchester, UK, Since September 2015 -
Research Consultant, μSystems Design Group at Newcastle University, UK, April 2015 -June 2015.
PGR Mentor, PhD CS Mentors Group, University of Manchester, UK, 2013- 2015.
PhD Candidate, Advanced Processor Tech. Group, University of Manchester, July 2012 – Dec. 2015.
Visiting Researcher, Advanced Processor Tech. Group, University of Manchester, July – Sept. 2011.
Industrial Internship, Iranian Embedded Systems Co, Tehran, Iran, June – Sept. 2010.
Undergrad Researcher, Router Research Laboratory, University of Tehran, Iran, March – June 2012.
IEEE member, region 8 since May 2010.

ATTENDED COURSES

Digital IC Implementation and Sign-off at Rutherford Appleton Labs - Oxford, UK – March 2013.
FPGA Design using Xilinx HLS (Vivado) at Rutherford Appleton Labs - Oxford, UK – Feb. 2015.
Computer Architecture Design, Computer Aided Design (CAD), Computer Networks, Asynchronous Circuit Design, Microprocessors, Operating Systems, Very Large Scale Integrated Circuits (VLSI), Theory of Computation at the University of Tehran -Tehran, Iran – Sept. 2007 – Feb. 2012.

RESEARCH EXPERIENCES

eTeak/Balsa as a framework: My collaboration with μSystems Design Group at Newcastle University is part of the GAELS project. In our recent contribution [1,2] we have coined the "*Vertical and Horizontal Elasticity*" terms in a sense that exploring elasticity at Description Level (DL), Cycle Level (CL), Register Transfer-Level (RTL) and Gate Level (GL) is considered as Vertical exploration whilst the algorithmic explorations regarding the computation models are considered as Horizontal exploration in the context of elasticity.
Supervisors: Prof. Alex Yakovlev and Dr. Danil Sokolov

eTeak – A Data-driven Synchronous Elastic Synthesiser: A High-level synthesis EDA to enable the designer realise integrated Sync/Async SoCs with mixed timing disciplines from a concurrent High-level description. My research within the last three years of PhD studies is incorporated in this Tool [3,4,5,6,7,8], [eTeak on Youtube].
Supervisors: Dr. Jim Garside and Dr. Doug Edwards

Clock synchronization in SpiNNaker: The SpiNNaker project is being developed by the APT research group at university of Manchester as a hardware based simulator of the brain. During my internship at APT in 2011, I was responsible for modelling a10k NoC architecture to monitor the effect of a particular clock synchronization heuristic in the network. Supervisors: Prof. Steve Furber and Dr. Jim Garside

FPGALSim: A novel FPGA-accelerated GALS NoC simulator. This simulator is able to model a multi-core system including on-chip networks with associated interactions using virtual asynchronous routers on a single FPGA. It achieves its capability in modelling accurate and fast GALS NoC systems by taking Co-design partitioning technique into account. Supervisor: Dr. Siamak Mohammadi

A high throughput buffer-less NoC architecture for multimedia applications: in this work we developed a buffer-less NoC architecture which is able to process high throughput network packets in multimedia applications. Regarding the buffer-less communication scheme, results were satisfying in terms of static power consumptions and leakage currents. Supervisor: Dr. Hamid Noori

A centralized/distributed localization algorithm for sensor motes in wireless sensor network: in this work we proposed an algorithm that can localize the network with minimum available density of beacons (GPS equipped nodes) based on RSSI and LQI signals [9]. Supervisor: Dr. Siamak Mohammadi

A UNIX based operating system (Semi MantisOS) on wireless sensor nodes to manage power consumption: This project was done during my summer internship at Iranian embedded systems Company in 2010. An event-driven operating system was required to manage resources, sensors, and controller in order to reduce power consumption. A radio chip module driver was also mounted to the host OS kernel [10].
Supervisor: Mr. Alireza Hoseini

Design and implementation of an architecture for supporting security CCMP and GCMP protocols in very high throughput (VHT) wireless LANS (802.11ad): This work is part of my contribution for the BSc. Project. The developed system is an extension to the multi-core CCMP architecture [12]. I proposed a supporting architecture for GCM protocol by considering minimum changes to our baseline configuration. The proposed architecture achieves 8.9 Gbps throughput. Supervisor: Prof. Nasser Yazdani

WNA: A mathematical model and tool for analysing very high throughput wireless LANs regarding throughput and network delay: in this project various features of 802.11n standard such as packet aggregation scheme, blocked acknowledge, and reversed direction technique are mathematically modelled for various types of packets under this standard [11]. Supervisor: Prof. Nasser Yazdani

TECHNICAL SKILLS

System Level Design: Control-Driven and Data-driven/Dataflow & Petri-Net based modelling
Scripting Languages: Tcl, Python, Bash
Hardware (ASIC) Design Tools: Design Compiler, PrimeTime, Power Compiler, ModelSim, H-Spice, L/S-Edit
Hardware (FPGA) Design Tools: Xilinx ISE / Vivado, NIOS, Altera Quartus
Network-on-Chip simulators: Noxim (SystemC), Booksim, eNoC(on NePA platform)
Asynchronous Synthesis Tools: Balsa, e/Teak, Petrify
FPGA Platforms: Xilinx (Virtex VI, Spartan 6), Altera (Cyclon II & Stratix IV)
Network Modeling Tools: Opnet, NS2, Matlab
Operating Systems: Windows, Linux (UBUNTU Kernel Programming), Unix (Mantis, TinyOS)

Hardware Modeling Language: Verilog, VHDL, SystemC, Balsa (CSP-based), Vivado-HLS (C)
Programming Languages: Go, Haskell, C/C++, Java, Assembly (ARM, x86, 8051, MIPS)

TEACHING EXPERIENCES

Demonstrated technical tutorials and assisted lecturers for the following modules: (Sept. 2012 – May 2015)

Microcontrollers - sem II	Microcontrollers - sem II
Processor Micro-architecture - sem I	Processor Micro-architecture - sem I
Fundamentals of Computer Engineering - sem I	Fundamentals of Computer Engineering - sem I

Assisted lecturers and provided support and guidance for undergrad students: (December 2008 - June 2011)

Computer Architectures - Spring 2011	Computer Architecture Laboratory - Spring 2011
Computer Networks - Spring 2011	Physics I laboratory - Winter 2008

PEER-REVIEWD PUBLICATIONS

[13] Ana Lava, **M. Jelodari Mamaghani**, Siamak Mohammadi, Steve Furber, "Application-Aware Retiming of Elastic Circuits" (*submitted*) 14th IEEE/ACM Memocode Conference, 2016

[12] M. Jelodari Mamaghani, Milos Krestic, J. Garside, "Automatic Clock: A Promising Approach Towards GALSification" (*to appear*) 22nd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), May 2016

[11] M. Jelodari Mamaghani, D. Sokolov, J. Garside, "Asynchronous Dataflow De-Elastisation for Efficient Heterogeneous Synthesis" (*to appear*) In Proc. of the 16th International Conference on Application of Concurrency to System Design (ACSD), Poland, June 2016

[10] M. Jelodari Mamaghani, J. Garside, D. Edwards, "De-Elastisation: From Asynchronous Dataflows to Synchronous Circuits," in Proc. of IEEE/ACM Conference on Design, Automation and Test in Europe (DATE). March 2015 [**DATE Best IP Award Winner**]

[9] M. Jelodari Mamaghani, J. Garside, W. Toms, D. Edwards, "Optimised Synthesis of Asynchronous Elastic Dataflows by Leveraging Clocked EDA," In Proc. of the 17th Euromicro Conference on Digital Systems Design (DSD), Verona, Italy. August 2014

[8] M. Jelodari Mamaghani, W. Toms, J. Garside, "Exploiting Synchrony for Area and Performance Improvement in the Asynchronous Domain," In Proc. of 20th International Symposium on Asynchronous Circuits and Systems (ASYNC), Potsdam, Germany. May 2014

[7] M. Jelodari Mamaghani, J. Garside, "High-level Synthesis of GALS Systems," In Proc. of PAnDA Workshop on Designing with Uncertainty - Opportunities & Challenges, York, UK. March 2014

[6] M. Jelodari Mamaghani, W. Toms, J. Garside, "eTeak: A Data-driven Synchronous Elastic Synthesiser," In Proc. of 13th International Conference on Application of Concurrency to System Design (ACSD), PhD Forum, Barcelona, Spain. July 2013

[5] S. A. Edwards, "MEMOCODE 2012 hardware/software codesign contest: DNA sequence aligner," In Proc. of 10th IEEE/ACM International Conference on Formal Methods and Models for Codesign (MEMOCODE), Virginia, US. July 2012

[4] M.Jelodari Mamaghani, M. Molkara, A. Hoseini, B. khodabandeloo, S. Mohammadi "A Centralized RSSI-Based Localization Algorithm for Wireless sensor networks," In Proc. of 4th Natl Conference of Command, Control, Communications, Computers and Intelligence (IC4I), Tehran, Iran. November 2011

[3] A. Hoseini, B. khodabandeloo, **M.Jelodari Mamaghani**, S. Mohammadi "Hardware and Software Implementation of a Wireless Sensor Node (WSN) with High Flexibility," In Proc. of 4th National Conference of Command, Control, Communications, Computers and Intelligence (IC4I), Tehran, Iran. November 2011

[2] A. Hoseini, **M. Jelodari Mamaghani**, B. khodabandeloo, M. Molkara, N. Yazdani "WNA: Wireless Network Analyzer for High Throughput Wireless LANs," In Proc. of 5th Int'l Symp of Telecommunication (IST), Iran Telecommunication Research Center, Tehran, Iran. December 2010

[1] A. Hoseini, B. khodabandeloo, **M. Jelodari Mamaghani**, P. Teymoori, N. Yazdani "High Throughput Low Power CCMP Architecture for Very High Speed Wireless LANs," In Proc. of 15th CSI Int'l Symp. of Computer Architecture & Digital Systems (CADS), IPM, Tehran, Iran. September 2010