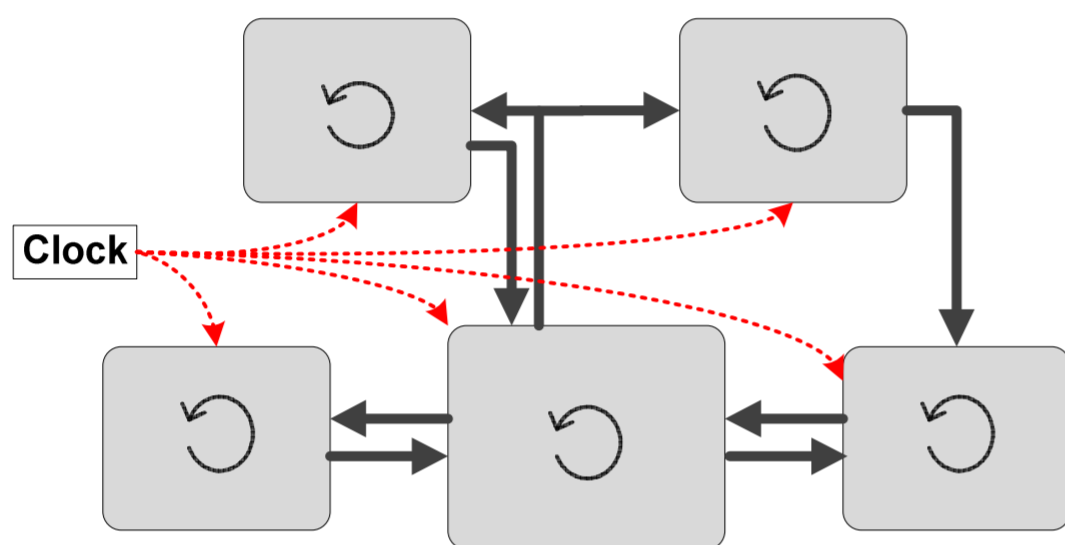


Introduction

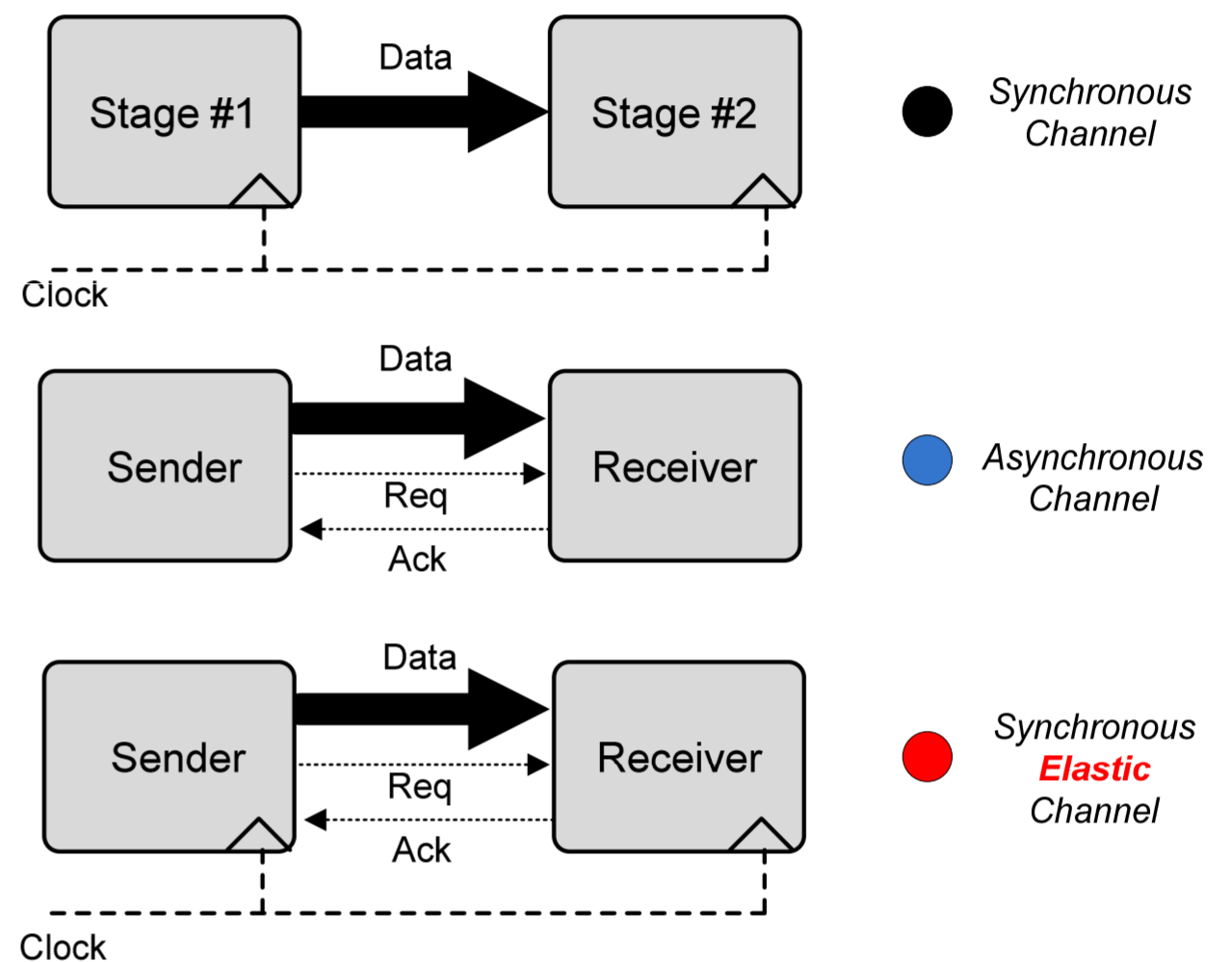
The forward-looking design trend in Very Large Scale Integrated (VLSI) is Systems-on-Chip (SoC). SoC aims to integrate multiple computation, communication and storage components into a single chip and targets high performance systems by elimination of most off-chip communication costs.

Aggressive technology scaling has brought up:

- Mismatch between gate and interconnect delays
- Variability in terms of power and clock speed
- Difficulties in power budget management
- Difficulties in clock distribution within a chip



How to address scaling issues?



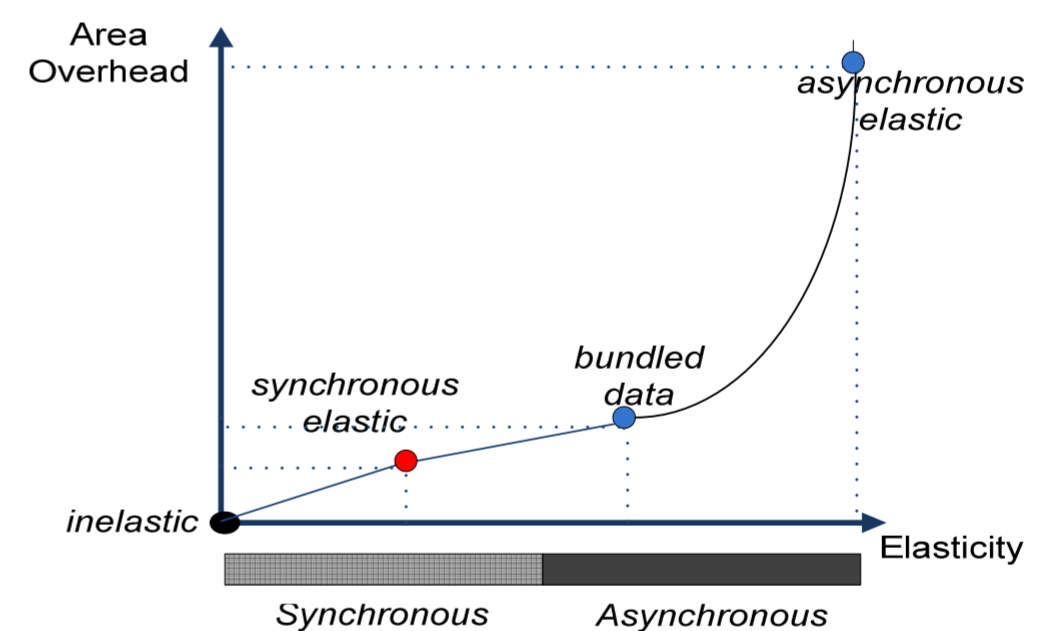
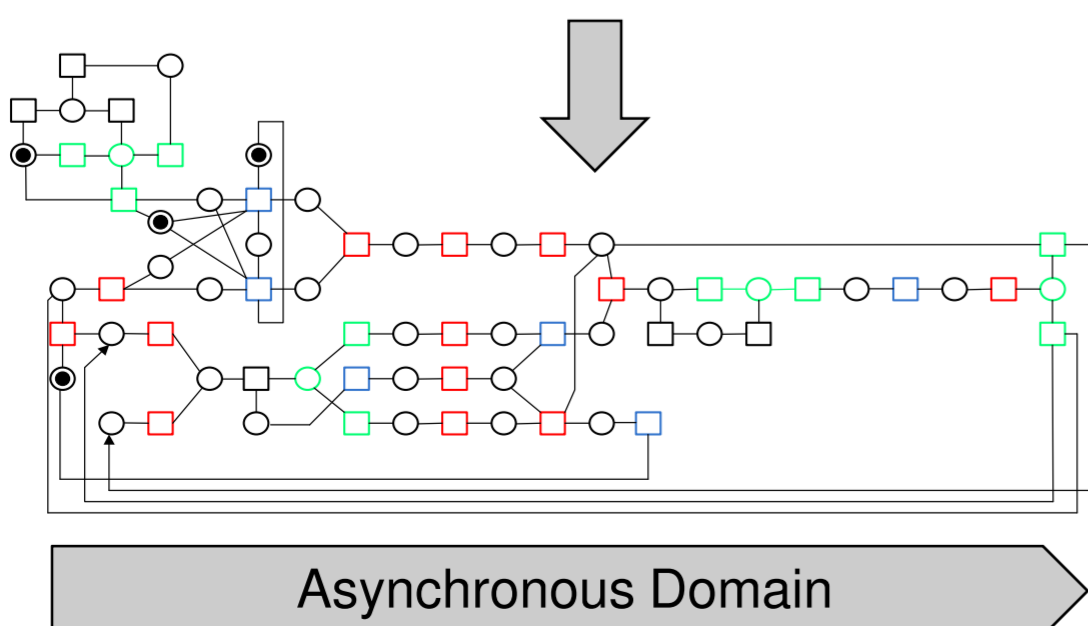
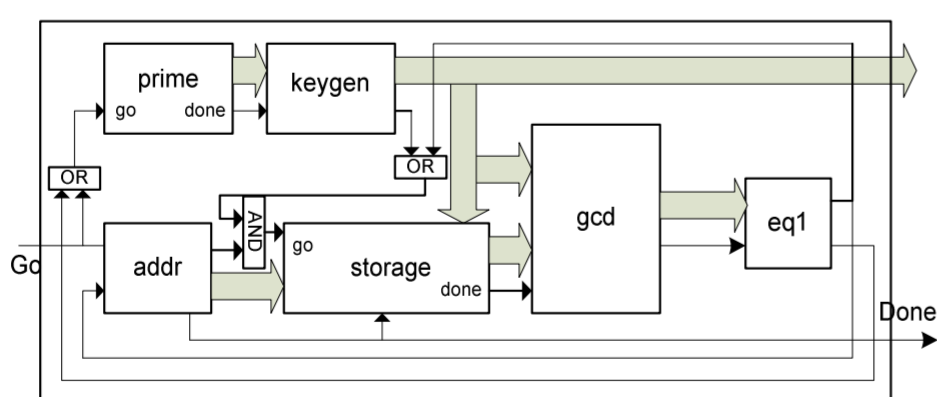
Methodology

Synchronous elasticity has emerged to exploit some of the advantages of asynchronous designs within synchronous systems to transform them into latency insensitive systems.

Synchronous elasticity provides a latency-insensitive framework which is synthesisable with commercial EDA tools.

High-Level Synthesis Flow

The flow starts off from a behavioural specification in *Balsa* language. At this level correct functionality is concerned and timing constraints are relaxed.



Synchronous Elasticity enables us to cross from the asynchronous domain to the synchronous domain and take advantage of mature synchronous tools for performance, power and area improvement.

Synchronous CAD tools will be used for:

- Circuit timing and power analysis
- Behavioural synthesis for optimisation purposes
- Identifying clock islands for multi-clock systems

