A Fault-tolerant Stochastic Network-on-chip Routing Algorithm

Wei Song
Supervised by Dr. Doug Edwards
Advanced Processor Group
What is Network-on-chip (NoC)?

Single Chip Single Processor

Single Board Multi Processor

Bus Based Multi Processor Chip

ProwerPC  DSP
IO  Decoder
ARM  Memory

NoC

ARM
DSP
Memory
Decoder
IO
ProwerPC
A NoC topology (4x4 mesh)

PE: processor element
R: router
Why fault-tolerant?

- Circuit in chip is not 100% reliable now!
  - Transient Error
    - Low thresh hold voltage causes the low noise tolerant level.
  - Permanent Error
    - Some cells are broken from the beginning and some will malfunction during the process.
Existed Routing Algorithm

- **Deterministic Routing**
  - According to address, single static route, no fault-tolerance; simple algorithm.

- **Adaptive Routing**
  - Multiple routes, and adaptive route selection, excellent fault-tolerance; complex algorithm.

- **Stochastic Routing**
  - Fully randomized route selection, the best fault-tolerance; simple algorithm.
Stochastic Routing
Our selected algorithm

- Function-oriented stochastic routing
  - No address requirement, adaptive configurable.
  - Stochastic routing, fault-tolerant.
  - Connection-oriented, guaranteed service.
  - Buffer-free, low area consumption.
Where is my contribution?

- **Throughput**
  - **Router algorithm**
    - Combine the adaptive routing into stochastic routing.
    - Improve throughput by sacrificing adaptation speed.

- **Power and area**
  - **Architecture**
    - Component sharing and architecture divide.
  - **Data Link**
    - Find the best power and area tradeoff point in speed and link width.
Conclusion

- **Project**: implement an asynchronous fault-tolerant network-on-chip chip.

- **Work**: routing algorithm and network implementation.

- **Research**: improve the routing algorithm and find the compromise between area, power and throughput.