Wei Song, PhD, Research Associate

CONTACT INFORMATION

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ACADEMIC EXPERIENCE

The University of Manchester, Manchester, UK, September 2007–Present

October 2011 to Present
Research Associate, School of Computer Science

- EPSRC Project EP/I038306/1: Globally Asynchronous Elastic Logic Synthesis
  - Implemented a RTL Verilog HDL parser using Bison and Flex.
  - Automatic finite state machine (FSM) detection using register relation graphs [18].
  - Automatic data-path extraction using signal-level data flow graphs [19].
  - Automatic data-path detection and system partition.
- Fault-tolerance techniques for asynchronous on-chip networks [17,20–22].
- Large-scale sorter on FPGA for database applications (FP7 Project AXLE).

September 2007 to September 2011
Ph.D. in Computer Science, School of Computer Science

- Supervisor: Dr. Doug Edwards
- EPSRC Doctoral Training Award EP/P503833/1 (10/2007–3/2011)
  EPSRC Project Grant EP/E06065X/1 (4/2008–7/2011)
  Bursary of the School of Computer Science, Univ. of Manchester (10/2007–3/2011)
- Thesis: *Spatial parallelism in the routers of asynchronous on-chip networks*
  - Designed and implemented asynchronous spatial division multiplexing (SDM) routers for asynchronous on-chip networks [13,15].
  - Designed and implemented a high-speed asynchronous wormhole router for asynchronous on-chip networks [9,11].
  - Designed and implemented the first asynchronous scheduler for three-stage S^3 Clos networks [12,14].
  - All designs are coded in synthesizable Verilog HDL (Faraday 130nm cell library), implemented by Synopsys DC-Topo, ICC, StarXRC, PrimeTime-PX, and simulated by SystemC/Verilog co-simulation using Cadence NC-Sim.

Beijing University of Technology, Beijing, P.R.China, September 2001–September 2008

September 2005 to September 2008
M.S.EE. in Automation, College of Electronic Information and Control Engineering

- Designed and implemented an ANSI C non-preemptive real-time scheduler [2,3,7,10] for the central controller of electrical vehicles. (supported by Beijing Sci. Foundation #KZ20041000501).

October 2004 to November 2006
Research Assistant, Beijing Embedded System Key Lab

- Implementing the ASIC prototypes into FPGA verification platforms for the final hardware test before tape out. FPGA platforms include Xilinx Virtex-4 and II. ASIC prototypes include the baseband for ATSC, DVB-T, DVB-C and WLAN 802.11g.

September 2001 to September 2005
B.S.EE. in Automation, College of Electronic Information and Control Engineering
Minor in Computer Science, College of Computer Science

2014

22 Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas and Zhiying Wang. **An asynchronous SDM network-on-chip tolerating permanent faults**. In submission to *Proc. of International Symposium on Asynchronous Circuits and Systems (ASYNC)*, 2014.

21 Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas and Zhiying Wang. **Protecting QDI interconnects from transient faults using delay-insensitive redundant check codes**. In submission to *Microprocessors and Microsystems*.

20 **Wei Song**, Guangda Zhang and Jim Garside. **On-line detection of the deadlocks caused by permanently faulty links in quasi-delay insensitive networks on chip**. In *Proc. of International Conference of the Great Lakes Symposium on VLSI (GLSVLSI)*, Houston, Texas, USA, May 2014.

19 **Wei Song**, Jim Garside and Doug Edwards. **Automatic data path extraction in large-scale register-transfer level designs**. In *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, June 2014.

2013

18 **Wei Song** and Jim Garside. **Automatic controller detection for large scale RTL designs**. In *Proc. of EUROMICRO Conference on Digital System Design (DSD)*, Santander, Spain, pp. 884–851, September 2013. (Rate: 49.0%)

17 Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas and Zhiying Wang. **Transient fault tolerant QDI interconnects using redundant check code**. In *Proc. of EUROMICRO Conference on Digital System Design (DSD)*, Santander, Spain, pp. 3–10, September 2013. (Rate: 49.0%)

2012

16 **Wei Song** and Doug Edwards. **Survey of asynchronous networks-on-chip**. *Journal of Computer-Aided Design & Computer Graphics*, Vol. 24, No. 6, pp. 11, 2012. (Chinese)

15 **Wei Song**, Doug Edwards, Jim Garside and William J. Bainbridge. **Area efficient asynchronous SDM routers using 2-stage Clos switches**. In *Proc. of Design, Automation & Test in Europe (DATE)*, Dresden, Germany, pp. 1495–1500, March 2012. (Rate: 16.0%)

2011

14 **Wei Song**, Doug Edwards, Zhenyu Liu and Sohini Dasgupta. **Routing of asynchronous Clos networks**. *IET Computers & Digital Techniques*, Vol. 5, No. 6, pp. 452–467, 2011.

13 **Wei Song** and Doug Edwards. **Asynchronous spatial division multiplexing router**. *Microprocessors and Microsystems*, Vol. 35, No. 2, pp. 85–97, 2011.

2010

12 **Wei Song** and Doug Edwards. **An asynchronous routing algorithm for Clos networks**. In *Proc. of International Conference on Application of Concurrency to System Design (ACSD)*, Braga, Portugal, pp. 67–76, June 2010. (Rate: 52.6%)

11 **Wei Song** and Doug Edwards. **A low latency wormhole router for asynchronous on-chip networks**. In *Proc. of Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, TAIWAN, pp. 437–443, January 2010. (Rate: 33.8%)

10 Zhe Xu, Shizhen Yan, **Wei Song**, Chunxuan Yu, Jianmin Duan, and Mingjie Zhang. ***A method to implement the CANopen master***. Chinese invention patent, Application No. CN200810056824.5, Grant No. CN101222510B, November 2010.

2009

9 **Wei Song** and Doug Edwards. **Building asynchronous routers with independent subchannels**. In *Proc. of International Symposium on SoC*, Tampere, Finland, pp. 48–51, October 2009. (Rate: 49.3%)

8 **Wei Song**, Doug Edwards, Jose Luis Nunez-Yanez, and Sohini Dasgupta. **Adaptive stochastic routing in fault-tolerant on-chip networks**. In *Proc. of ACM/IEEE International Symposium on Networks-on-Chip (NoCS)*, San Diego, CA, USA, pp. 32–37, May 2009. (Rate: 23.0%)

7 Zhe Xu, Shizhen Yan, **Wei Song**, and Zhuo Zhang. **Development of the CANopen master based on MC9S12DP512 and μC/OS-II**. *Computer Engineering and Science*, Vol. 31, No.

5, pp. 118–120, 2009. (Chinese)

6 Zhe Xu, Shizhen Yan, and **Wei Song**. **Object dictionary design of CANopen based on hash table**. *Computer Engineering*, Vol. 35, No. 8, pp. 44–46, 2009 (Chinese).

Earlier

5 **Wei Song**, Suiming Fang, Dan Yao, Lichao Zhang, and Cheng Qian. Clock synchronization in multi-FPGA designs. *Computer Engineering*, Vol. 34, No. 7, pp. 245–247, 2008 (Chinese).

4 **Wei Song**, Suiming Fang, Mingjie Zhang, and Zhe Xu. **Task scheduler in the design of CANopen master**. *Computer Measurement & Control*, Vol. 16, No. 4, pp. 558–560, 2008 (Chinese).

3 **Wei Song**, Shizhen Yan, Zhe Xu, and Suiming Fang. **Transplantable CANopen master based on non-preemptive task scheduler**. In *Proc. of IEEE International Conference on Automation and Logistics (ICAL)*, Jinan, P.R.China, pp. 557–562, August 2007.

2 **Wei Song** and Suiming Fang. Clock circuit design in FPGA based on BUFGMUX and DCM. *Modern Electronic Technique*, Vol. 29, No. 2, pp. 141–143, 2006. (Chinese)

1 **Wei Song**. **The method of using m-files of MATLAB6.5 in C language**. *Computer and Information Technology*, Vol. 7, No. 12, pp. 57–58, 2004. (Chinese)

OPENSOURCE PROJECTS

Asynchronous Verilog Synthesiser, ongoing

Generate elastic or asynchronous circuits from synchronous RTL designs written in Verilog HDL.

https://github.com/wsong83/Asynchronous-Verilog-Synthesiser

C++/Tcl, stable

A C++ library for interoperability between C++ and Tcl.

Adopted from the original C++/Tcl designed by Maciej Sobczak.

https://github.com/wsong83/cpptcl

Asynchronous Spatial Division Multiplexing (SDM) Router, stable

Hardware designs of asynchronous SDM routers using Nangate 45nm cell library. Gate-level, synthesisable netlist written in Verilog HDL. SystemC testbenches and synthesis scripts for Synopsys DC provided.

http://opencores.org/project,async_sdm_noc

ACADEMIC ACTIVITIES

IEEE Member

Reviewer for:

IET Computer and Digital Techniques
Microprocessors and Microsystems
Journal of Computers

TECHNICAL SKILLS

Hardware implementation flow

TLM/RTL/Gate hardware design
SystemC/Verilog/VHDL mixed simulation
ASIC and FPGA: synthesis, place and routing

Languages

Verilog/VHDL, C/C++, SystemC, System Verilog, Petrify, Balsa, MATLAB, HSpice, ARM ASM, JAVA, Haskell, Perl

Operation Systems

Windows/MS-DOS, Linux, Unix

Tools

Cadence: NC-Sim, SoC encounter, Virtuoso
Synopsys: Design Compiler, IC Compiler, VCS, Hspice, Nanosim
Mentor: ModelSim, Calibre xRC/LVS
FPGA: Xilinx ISE, Synpicity Synplify, Altera Quartus II
Other: Microsoft Visual C++/GNU GCC, ARM ADS, Word/LaTex, Emacs