An Adiabatic Power-Supply Controller For Asynchronous Logic Circuits

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Abstract—**Adiabatic logic can offer significant power reductions in comparison to conventional CMOS circuits ([1], [2]). Although numerous architectures have been proposed in the literature for synchronous circuit implementations, not much work has been done on asynchronous logic due to the difficulties of such implementations. This paper presents a new adiabatic power supply controller for asynchronous circuits which attempts to improve on previous asynchronous adiabatic approaches.**

I. INTRODUCTION

IN conventional CMOS circuits (Figure 1), when the pull-up network is switched on a certain amount of charge $Q = CV_{DD}$ is pulled out of the positive power supply rail to charge the load capacitance C up to V_{DD}. At a subsequent clock cycle, when the pull-down network switches on the load capacitor is discharged and the charge is transferred to the ground terminal of the power supply. Over a complete charge/discharge cycle the energy transferred by the power supply to the circuit is $E = QV_{DD} = CV_{DD}^2$, which is dissipated on the pull-up and pull-down transistors during the charge/discharge phases. Ideally the dissipated energy will be evenly distributed amongst the pull-up/pull-down networks and thus, $E_{charge} = E_{discharge} = \frac{1}{2}CV_{DD}^2$.
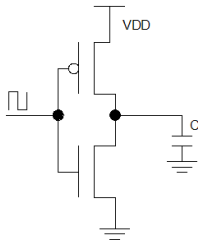

Figure 1. A CMOS Inverter.

It can be easily derived from the above equations that to reduce the energy consumption in conventional CMOS, either the supply voltage V_{DD} has to be reduced or the load capacitance C. If the main concern is the power consumption of the circuit ($P = \frac{dE}{dt}$), then the switching activity can be reduced as well.

Adiabatic logic follows a different approach to minimize the energy loss during the charge/discharge phases by attempting to recover the charge back to the power supply, instead of dissipating it as heat and by charging/discharging all nodes at constant current levels to minimize energy dissipation [1]. This

is accomplished by using AC power supplies which charge the circuit during specific adiabatic phases and subsequently discharge it to recover the supplied charge. Constant current flow is achieved at all times by making ramp-like transitions between high-low and low-high voltage levels.

II. PREVIOUS WORK

Various circuit architectures have been proposed in the literature that are able to take advantage of adiabatic charging principles. A typical configuration is the 2N-2P family of logic circuits [2], which is based on the DCVSL logic (Figure 2).
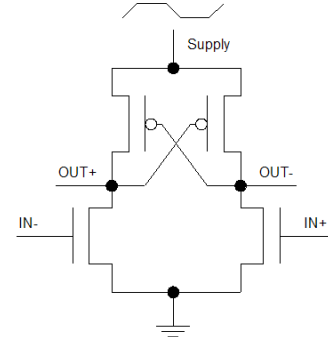

Figure 2. Basic 2N-2P Adiabatic Circuit.

The timing diagram of the circuit can be seen in Figure 3. Initially, the adiabatic supply is in the WAIT phase and the supply voltage is LOW maintaining at the same time the outputs in the LOW state. Then the inputs are set (one goes LOW the other HIGH) and the supply voltage ramps-up. As the inputs are evaluated, the outputs change complementary to each other and the one that goes HIGH, follows the power supply until it reaches V_{DD}. At that moment the inputs are returned to the LOW state and after a certain period of time in the HOLD "1" phase, the supply ramps down with the outputs following until the LOW state is reached again.

The charge recovery by the power supply occurs during the RESET phase and the adiabatic charging/discharging takes place during the ramping-up/-down in the EVALUATE/RESET phases. As the supply gradually changes from LOW to HIGH and vice versa, the charge transfer to the load capacitance of the circuit is performed in constant current mode and thus energy dissipated by the transistor switches is minimized. This is in contrast to conventional CMOS where the voltage
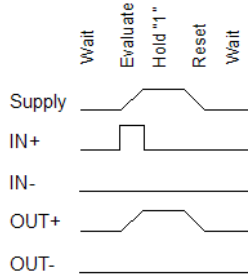
Figure 3.   2N-2P Timing.

levels change almost instantaneously and the charge transfer is performed in constant voltage mode, with high levels of current passing through the transistor switches.

An additional benefit of adiabatic logic is that the power supply also contains the circuit clock, therefore separate clocking signals are not required for the proper operation of adiabatic circuits. This is a distinct advantage for synchronous circuits and various circuit architectures have been proposed in the literature on synchronous adiabatic logic.

On the contrary not much work has been presented on asynchronous adiabatic implementations. The main reason is that it is necessary for adiabatic logic to have global power-supply clocks for charging/discharging all circuits at specific periods, whilst in asynchronous logic a global clock is undesirable and each logic block has to be clocked separately by making use of handshake signals. Therefore, an asynchronous adiabatic implementation would normally require a separate power-supply clock generator for each asynchronous logic block, which may not be practically feasible since the generators are typically based on externally placed inductor circuits [3]. Thus resolving this issue is a major challenge for asynchronous adiabatic design.

An alternative method for generating the adiabatic power-supply clock for asynchronous circuits was proposed in [4], which makes use of a controller to operate a tank capacitor stepwise charging circuit based on the Request/Acknowledge signals of the asynchronous handshake. While this implementation conserves space by replacing the power-clock generator inductors with capacitors, the supply voltage output does not produce a ramp-like waveform, unless the circuit is composed of a very large number of capacitors, ideally infinite. So in practice the charging/discharging of the circuit does not follow adiabatic principles and a percentage of the energy that could be recovered is lost. Furthermore, the stepwise charging circuit has to be implemented for every single asynchronous logic block which requires separate handshaking, possibly making this implementation very space consuming, especially if some of the tank capacitors are to be placed externally of the chip.

III. CIRCUIT

The circuit proposed in this paper attempts to overcome some of the limitations of asynchronous adiabatic logic designs. It utilizes a just single inductor-based sine wave power supply for all the asynchronous logic blocks on the chip,

combined with independent CMOS adiabatic supply controllers for generating the individual ramp-like power supply waveforms for each adiabatic asynchronous logic block. The block diagram of the circuit along with the control signals for the four adiabatic phases (EVALUATE, HOLD "1", RESET, WAIT) can be seen in Figure 4.
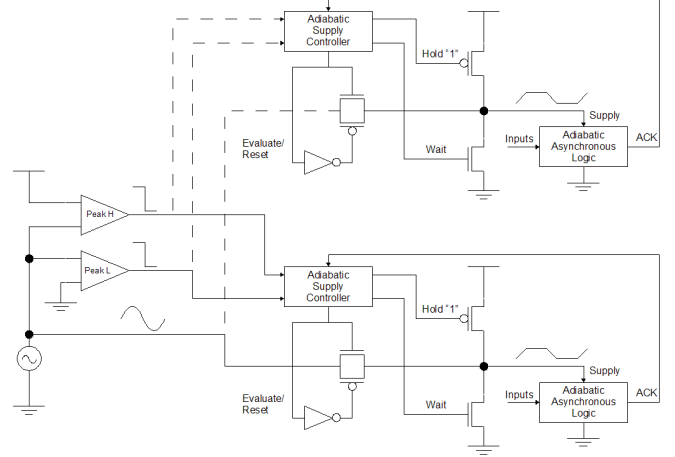

Figure 4.   Proposed circuit configuration for Asynchronous Adiabatic Logic.

The adiabatic supply controller sets the asynchronous circuit in one of the adiabatic phases, based on the status of the asynchronous Acknowledge signal and the global sine-wave supply (HIGH peak or LOW peak). In summary, the operation principle is as follows: Each time the Acknowledge signal goes HIGH, the controller generates an EVALUATE signal and the asynchronous logic block is supplied with the first half of the sine-wave period, going from the LOW peak to the HIGH peak. When the sine-wave reaches its HIGH peak (V_{DD}), the EVALUATE signal goes LOW and a HOLD "1" signal is generated (which signals LOW) and is kept LOW until the Acknowledge signal goes LOW again. Then the HOLD "1" signal goes HIGH and a RESET signal is generated which supplies this time the asynchronous logic block with the second half of the sine wave period, going from the HIGH peak to the LOW peak, effectively discharging the circuit. When the sine-wave reaches its LOW peak (thus the circuit is fully discharged) the RESET signal goes LOW and a WAIT signal is generated, ending the adiabatic charge/discharge cycle. The transitions of the sine wave from the LOW peak to the HIGH peak and vice versa, are detected by using two comparator circuits. The timing diagram of the described operation principle can be seen in Figure 5.

Using the fore-mentioned method a fully-adiabatic charging/discharging and charge recovery can be achieved. The main limitation is that the global sine-wave supply has to be clocked at a higher frequency than the asynchronous logic blocks. Assuming that in the worst case the Acknowledge signal goes HIGH exactly after a LOW peak is detected, the controller must wait for 1 sine-wave period until the next LOW peak to begin the EVALUATE phase. The EVALUATE phase requires itself $\frac{1}{2}$ period to charge the asynchronous circuit. Assuming that the HOLD "1" phase will not be very short,
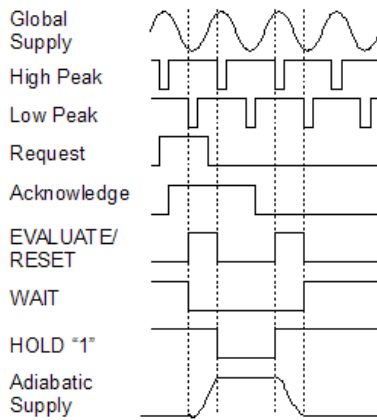
Figure 5.   Adiabatic Supply Controller Timing Diagram.

Figure 6.   Adiabatic Supply Controller.

the controller has to wait for another 1 period until the next HIGH peak to begin the RESET phase, which will last for $\frac{1}{2}$ period to discharge the circuit. So in the worst case the circuit will require $1 + \frac{1}{2} + 1 + \frac{1}{2} = 3$ sine-wave periods to complete all 4 adiabatic phases. Of course, if the controller begins the EVALUATE phase at the first LOW peak and ends the RESET phase at the subsequent LOW peak, the 4 adiabatic phases are completed in just 1 sine wave, but this is the best possible case and in practice to assure correct operation of the circuit at all times, the sine-wave supply must be set at 3 times the operating frequency of the fastest asynchronous logic block in the chip.

The logic implementation of the Adiabatic Supply Controller can be seen in Figure 6. Since the controller inputs (Acknowledge, Peak detectors) come from two different time domains, there is a possibility for the set-up and hold conditions of the input gates to be violated and thus metastability to occur [5]. No action was taken to prevent this, but since the frequencies of the inputs for this circuit are several times slower than the speed of the gates, it can be assumed for the purposes of this analysis that there will be enough time for any metastability to be resolved and thus keep the chances of circuit failure to acceptable levels.

Furthermore the sine-wave generator supply and the two comparators, seen in Figure 4, were not implemented on the transistor level as their design is considered out of scope of this work. In their place ideal circuits were used providing with the same functionality. As a result the power consumption of these components could not be taken into account during simulations, but although these circuits have to be as energy efficient as possible, their impact to each individual asynchronous logic block is minimal since they are shared amongst all logic blocks in the chip. An example of a peak detector implementation is presented in [6] and examples of sine wave power supplies in [3] and [7].

IV. COMPARISON RESULTS

To evaluate the performance of the proposed circuit, a dual-rail 1-bit half adder function block was designed and implemented in both conventional CMOS and adiabatic asynchronous logic. For the adiabatic implementation a modified
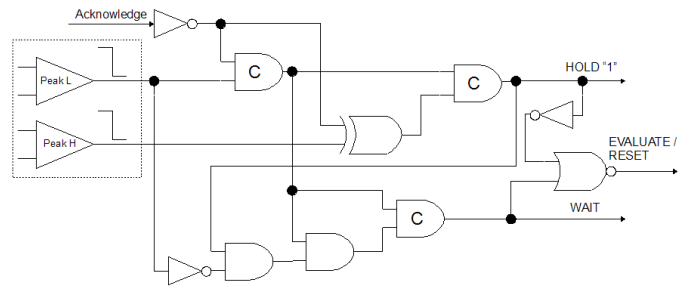
2N-2P structure was used [8] (Figure 7), so as to allow for full charge recovery during the RESET phase. The PULSE signal is activated during the RESET phase and it is easily generated from the adiabatic controller outputs.
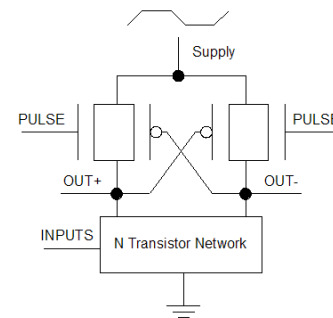

Figure 7.   Modified 2N-2P.

For the conventional asynchronous implementation a precharged differential CMOS combinatorial circuit [9] was designed (Figure 8). This design is very similar to the one used for the adiabatic logic since they are both based on DCVSL. The handshaking for both implementations is handled by a 2-bit dual-rail pipeline [9]. As it can be observed in Figure 9, the dual-rail pipeline is implemented in conventional CMOS, so only the asynchronous function block can actually benefit from the adiabatic power supply. Therefore if we consider that adiabatic asynchronous logic induces a power overhead, because of the required adiabatic power supply controller, it is evident that the asynchronous function block must have a much higher power consumption than the handshaking part of the circuit, so as to gain any benefits from an adiabatic logic implementation.
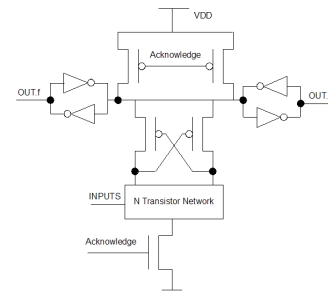

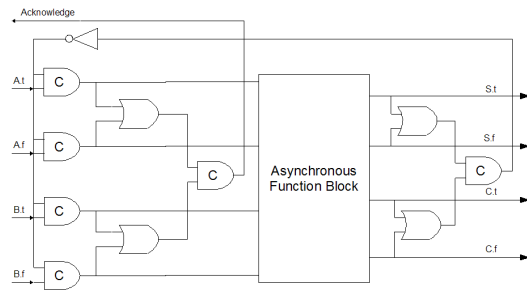Figure 8.   Precharged Differential CMOS combinatorial circuit.

Figure 9.   2-bit Dual-Rail Pipeline.

Simulation results can be seen in Figure 10 and an implementation comparison in Table I. The simulations were carried on for frequencies in the range of 2-100MHz using transistor models for the UMC 90nm process technology. The power consumption of the asynchronous function blocks was gradually increased by inserting additional copies of the half-adder function blocks in the circuit, but without concurrently increasing the width of the pipeline.

Table I
POWER REDUCTIONS OF THE ADIABATIC IMPLEMENTATION COMPARED
TO THE NON-ADIABATIC.

Frequency (MHz)	Power Impr/ment 8-HAs (%)	Power Impr/ment 4-HAs (%)	Power Impr/ment 2-HAs (%)
100	79	52	15
50	77	49	8
20	73	38	-12
10	64	20	-42
2	14	-67	-49

V.   CONCLUSIONS

The simulations demonstrated that considerable power consumption savings up to 79% can be achieved when asynchronous logic is implemented adiabatically. The advantage of this approach compared to other approached is that only a single AC power supply is required for all logic blocks in the chip. The main weaknesses are, the reduced maximum speed of the logic circuits and the power consumption overhead of the adiabatic supply controller. Therefore this design approach is more appropriately suited and could considerably benefit applications that require low-to-medium speed performances and implement medium-to-high complexity logic functions.
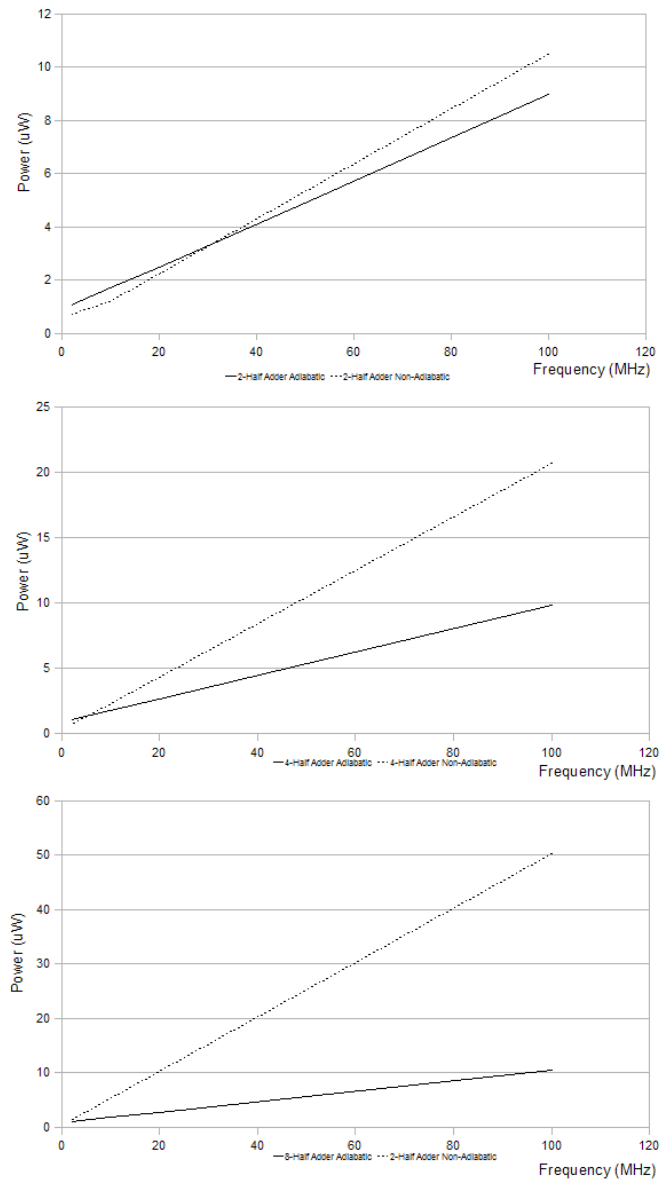

Figure 10.   Adiabatic/Non-Adiabatic Power Consumption Simulations.

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