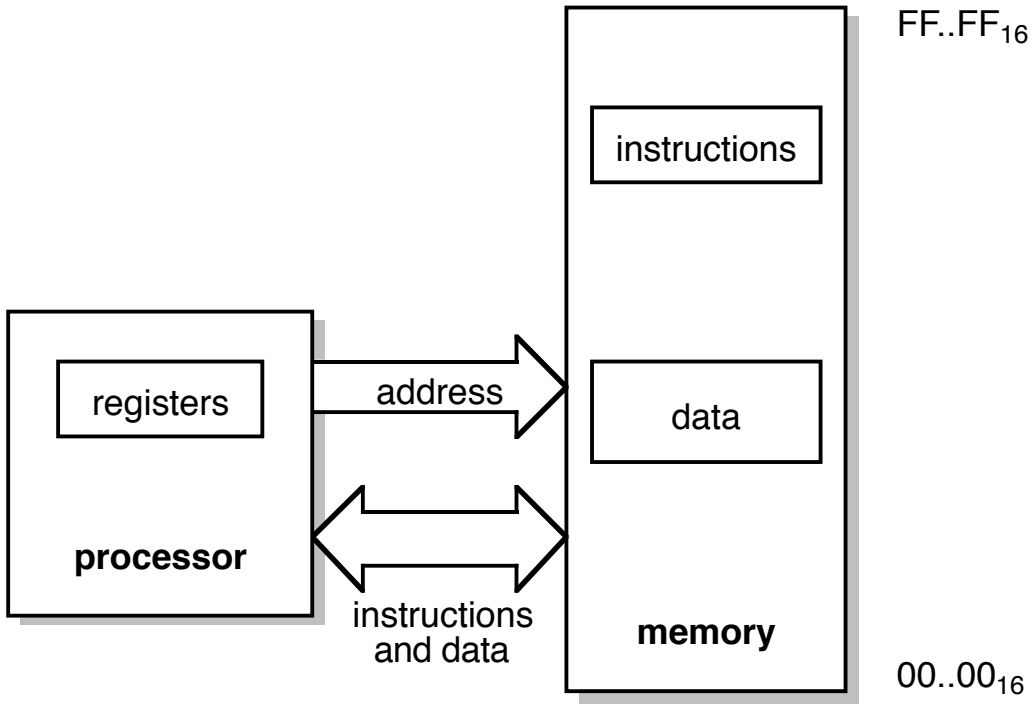
The state in a stored-program digital computer



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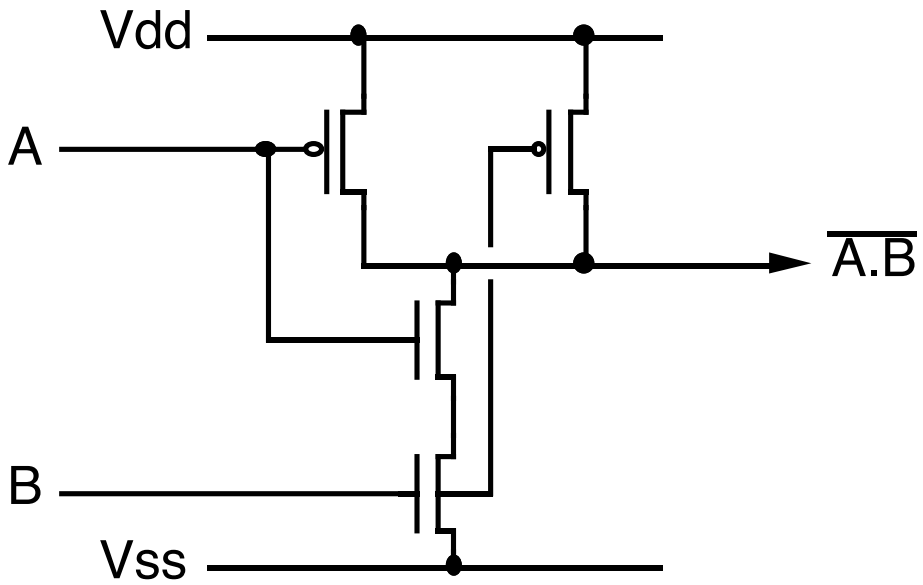
The transistor circuit of a static 2-input CMOS NAND gate



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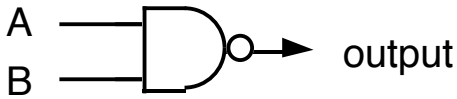
The logic symbol and truth table for a NAND gate



Logic symbol

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Truth table

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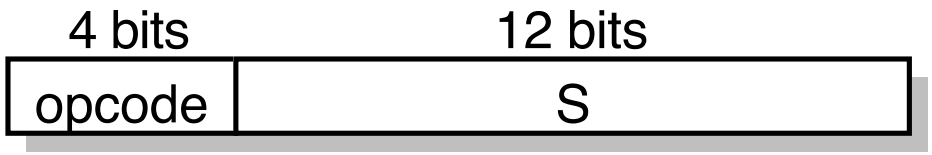
The MU0 instruction format



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The MU0 instruction set

Instruction	Opcode	Effect
LDA S	0000	ACC := mem_{16}[S]
STO S	0001	mem_{16}[S] := ACC
ADD S	0010	ACC := ACC + mem_{16}[S]
SUB S	0011	ACC := ACC - mem_{16}[S]
JMP S	0100	PC := S
JGE S	0101	if PC := S
JNE S	0110	if PC := S
STP	0111	stop

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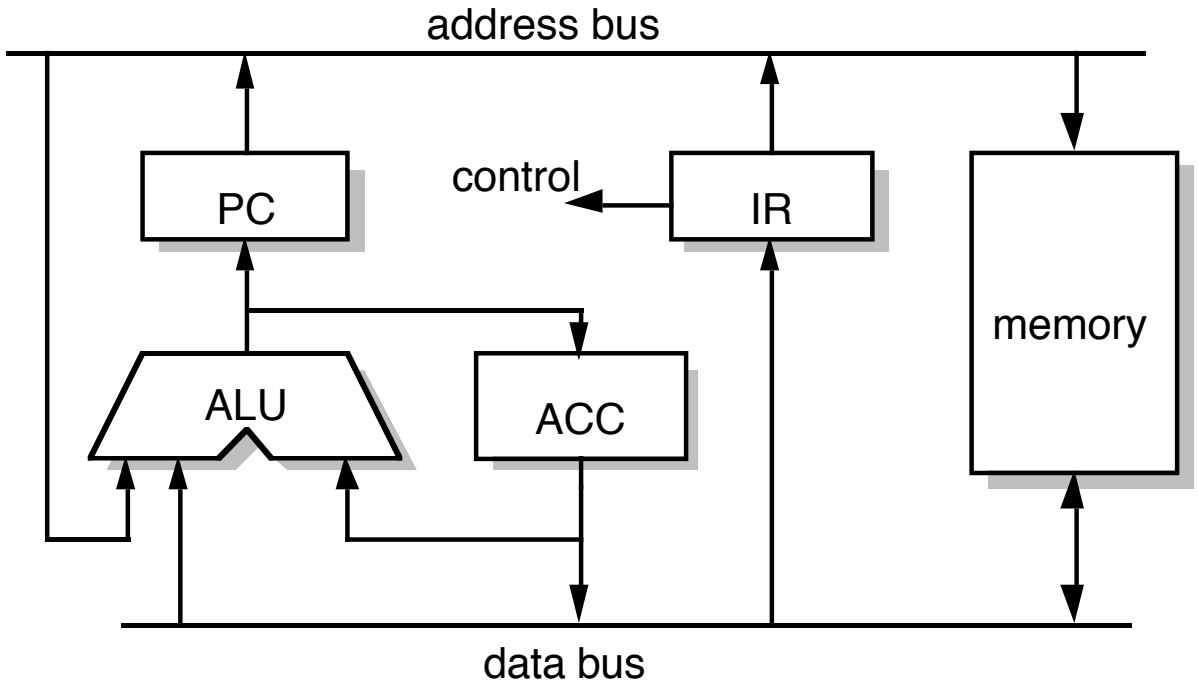
MU0 datapath example



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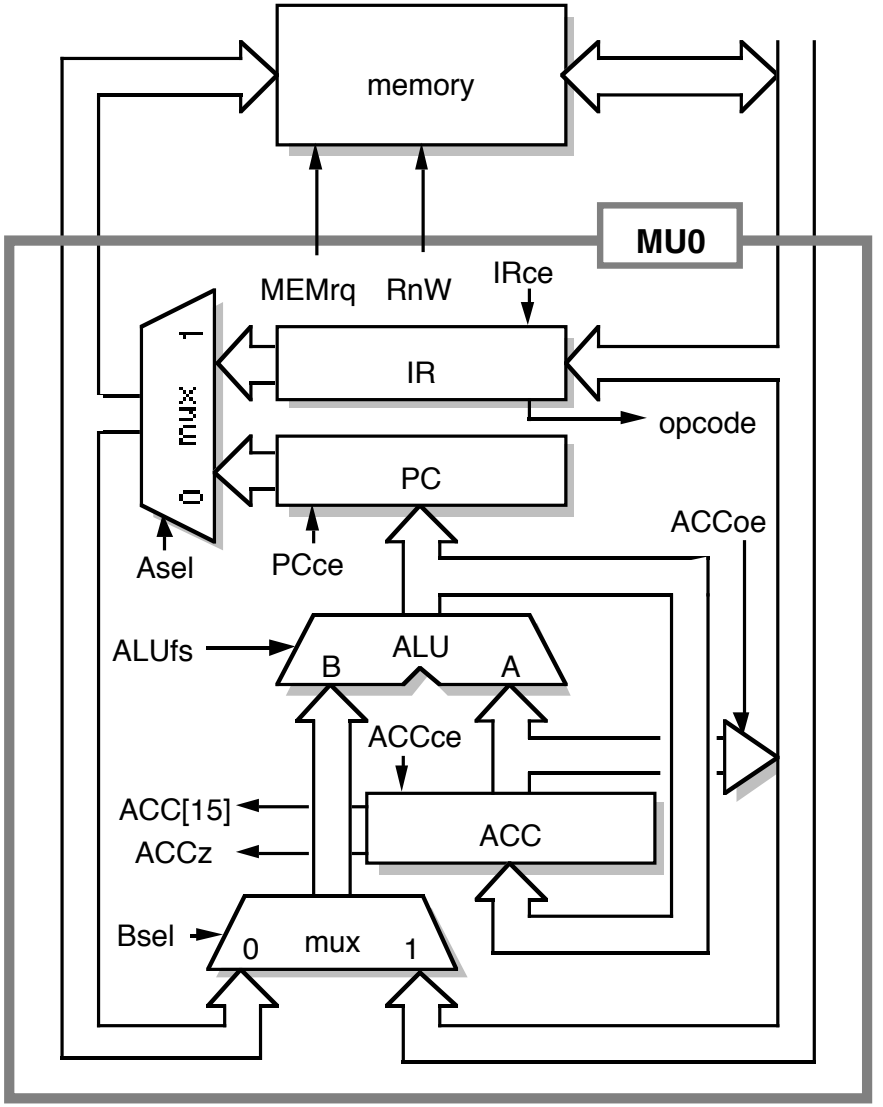
MU0 register transfer level organization



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MU0 control logic

Inputs						Outputs									
	Opcode	Ex/ft		ACC15			Bsel		PCce	ACCoe		MEMrq	Ex/ft		
Instruction		Reset		ACCz		Asel	ACCce		IRce		ALUfs		RnW		
Reset	xxxx	1	x	x	x	0	0	1	1	1	0	=0	1	1	0
LDA S	0000	0	0	x	x	1	1	1	0	0	0	=B	1	1	1
	0000	0	1	x	x	0	0	0	1	1	0	B+1	1	1	0
STO S	0001	0	0	x	x	1	x	0	0	0	1	x	1	0	1
	0001	0	1	x	x	0	0	0	1	1	0	B+1	1	1	0
ADD S	0010	0	0	x	x	1	1	1	0	0	0	A+B	1	1	1
	0010	0	1	x	x	0	0	0	1	1	0	B+1	1	1	0
SUB S	0011	0	0	x	x	1	1	1	0	0	0	A-B	1	1	1
	0011	0	1	x	x	0	0	0	1	1	0	B+1	1	1	0
JMP S	0100	0	x	x	x	1	0	0	1	1	0	B+1	1	1	0
JGE S	0101	0	x	x	0	1	0	0	1	1	0	B+1	1	1	0
	0101	0	x	x	1	0	0	0	1	1	0	B+1	1	1	0
JNE S	0110	0	x	0	x	1	0	0	1	1	0	B+1	1	1	0
	0110	0	x	1	x	0	0	0	1	1	0	B+1	1	1	0
STOP	0111	0	x	x	x	1	x	0	0	0	0	x	0	1	0

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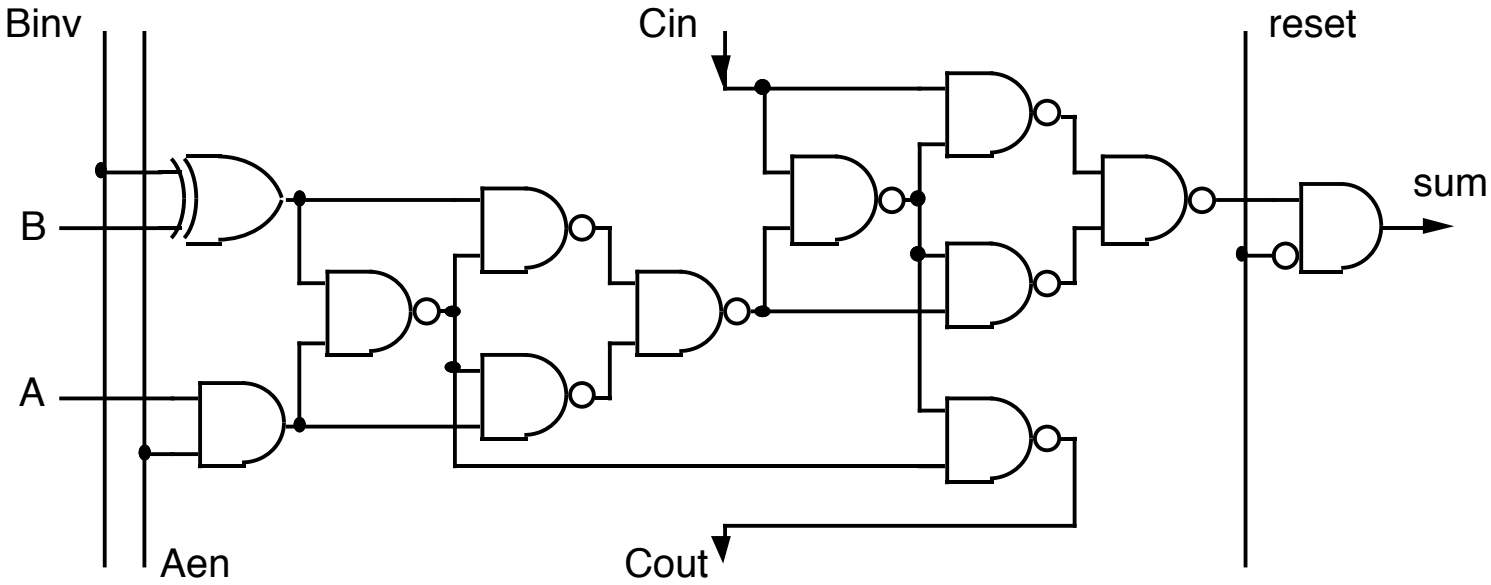
MU0 ALU logic for one bit



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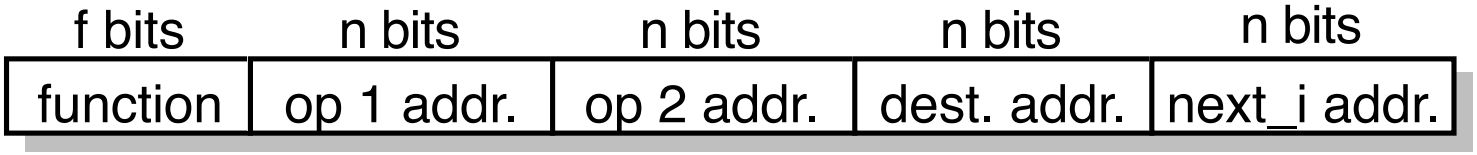
A 4-address instruction format



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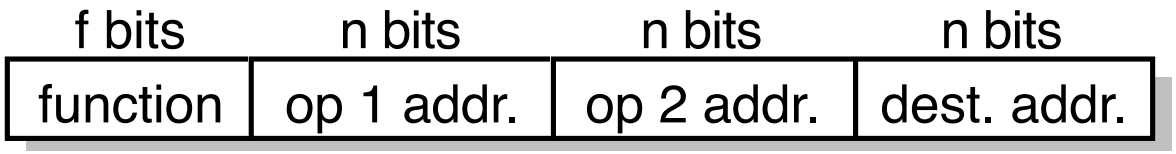
A 3-address instruction format



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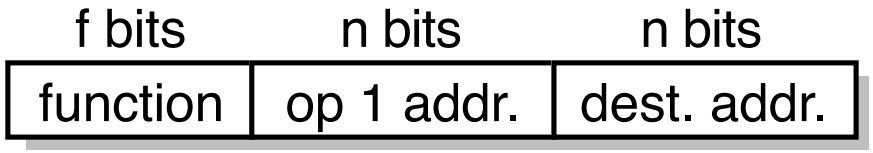
A 2-address instruction format



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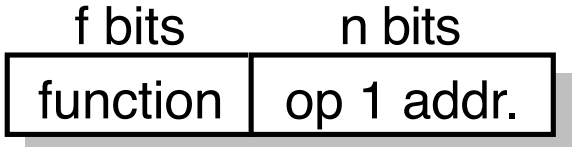
A 1-address (accumulator) instruction format



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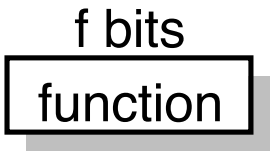
A 0-address instruction format



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Typical dynamic instruction usage

Instruction type	Dynamic usage
Data movement	43%
Control flow	23%
Arithmetic operations	15%
Comparisons	13%
Logical operations	5%
Other	1%

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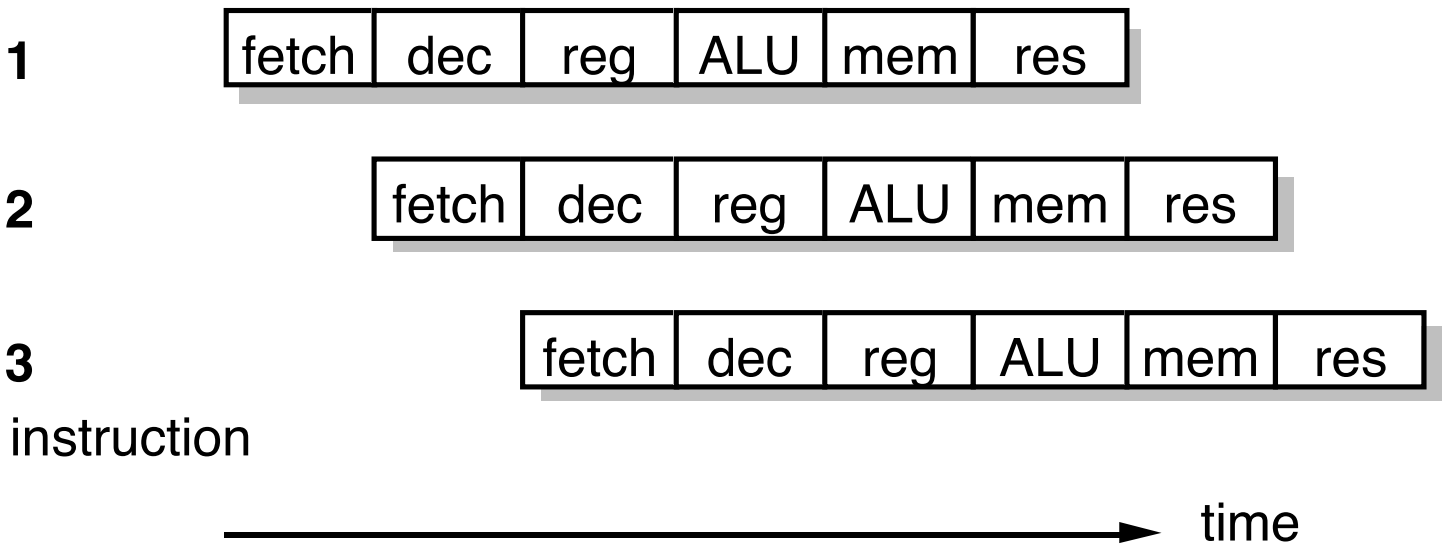
Pipelined instruction execution



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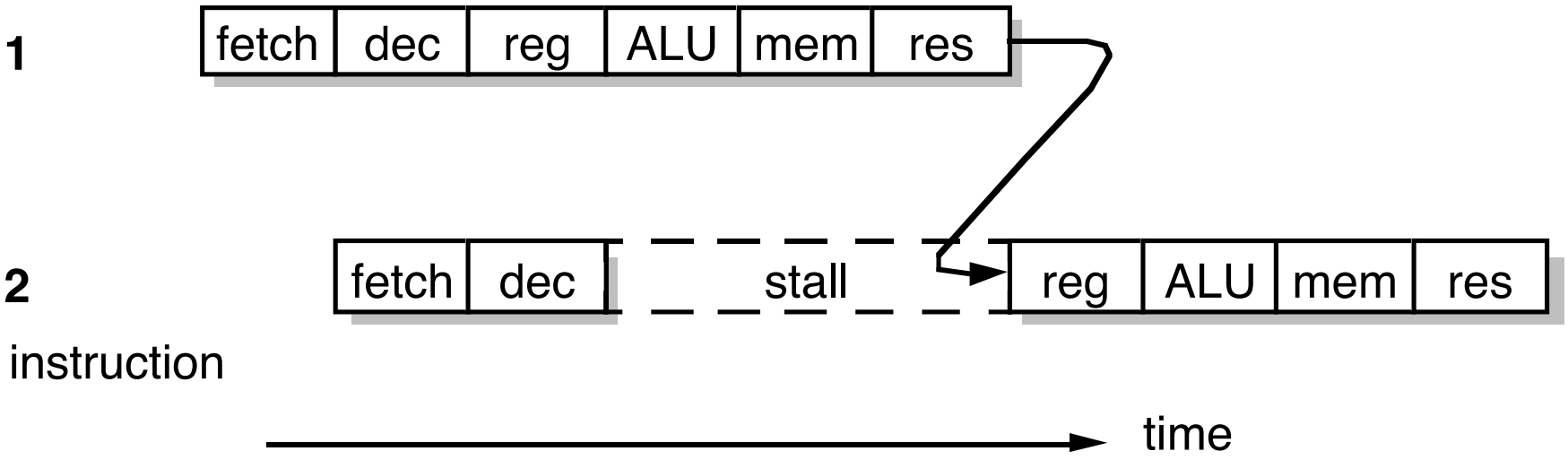
Read-after-write pipeline hazard



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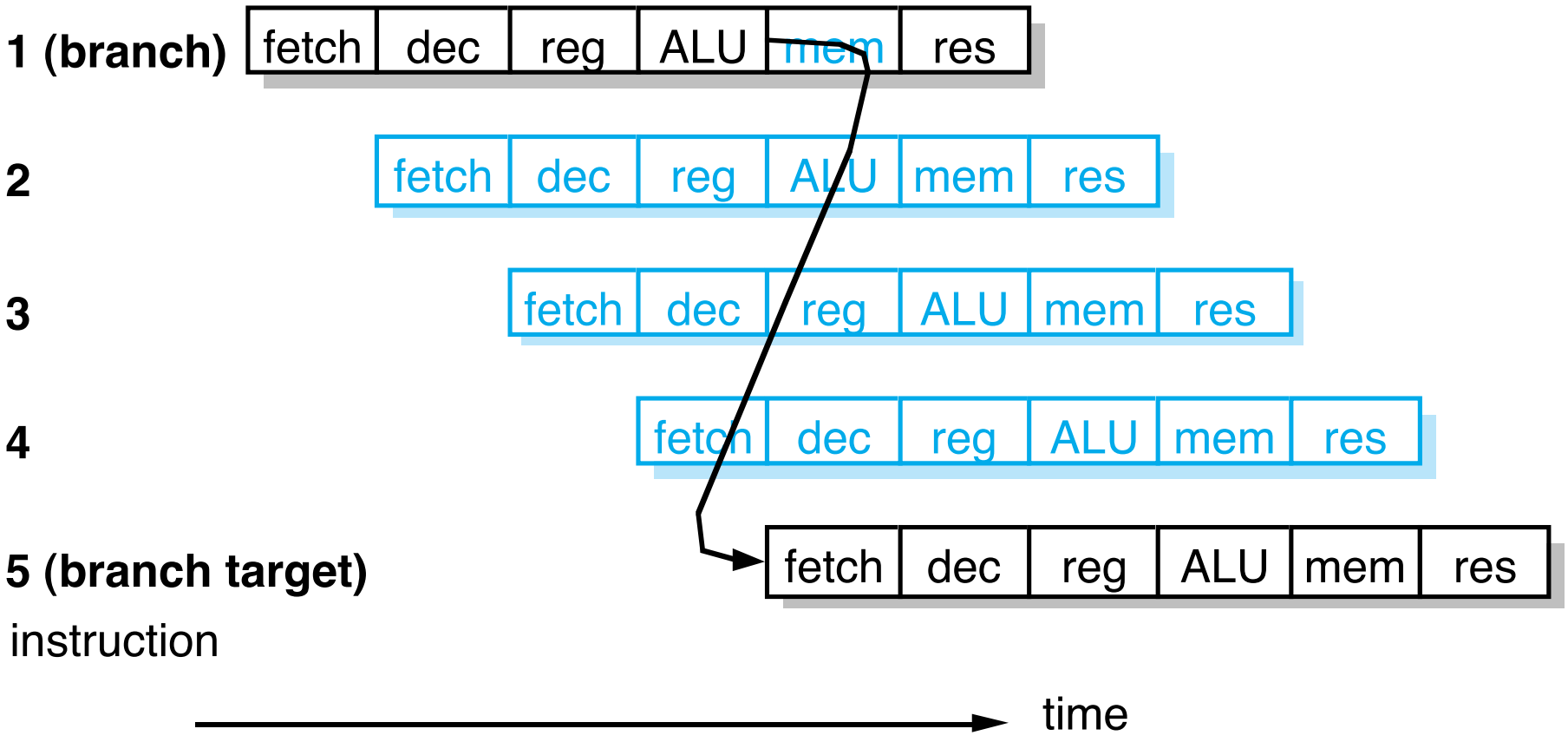
Pipelined branch behaviour



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