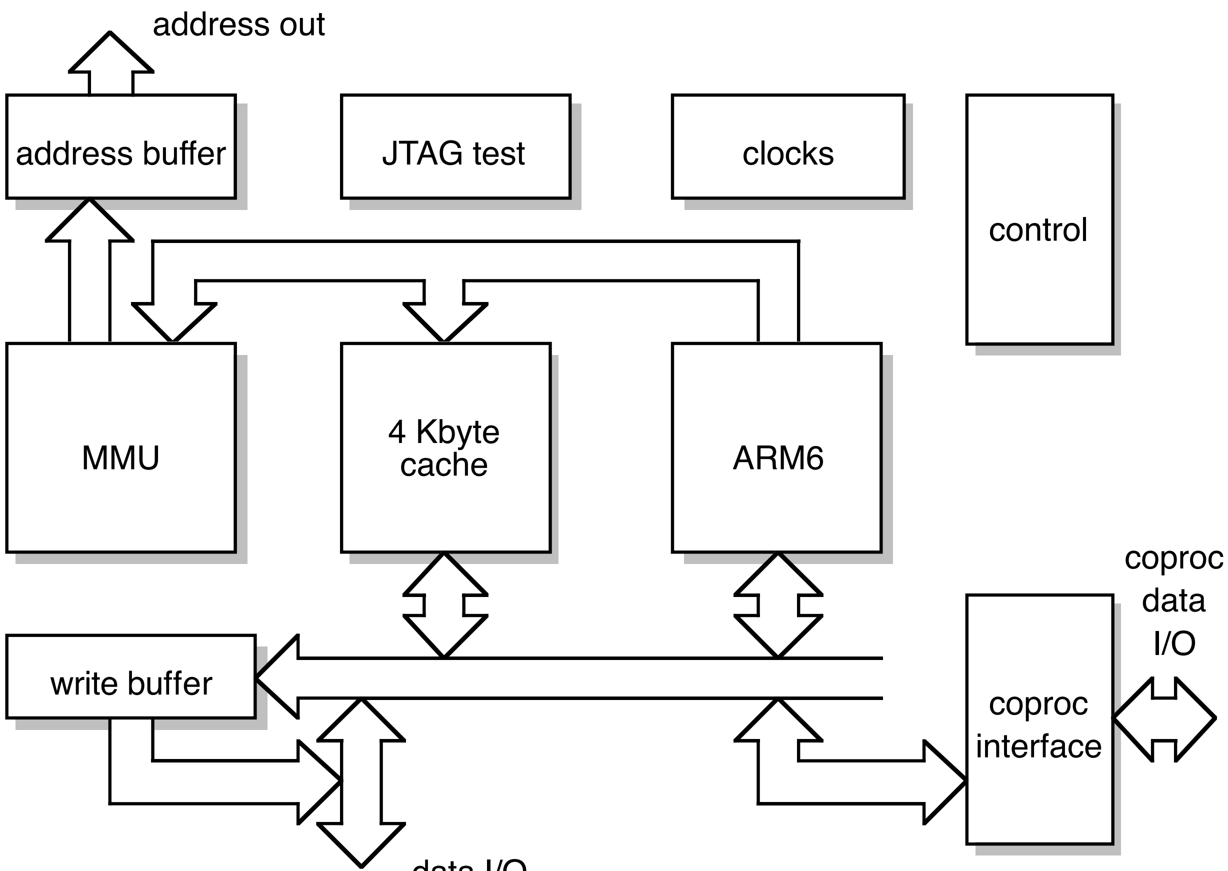
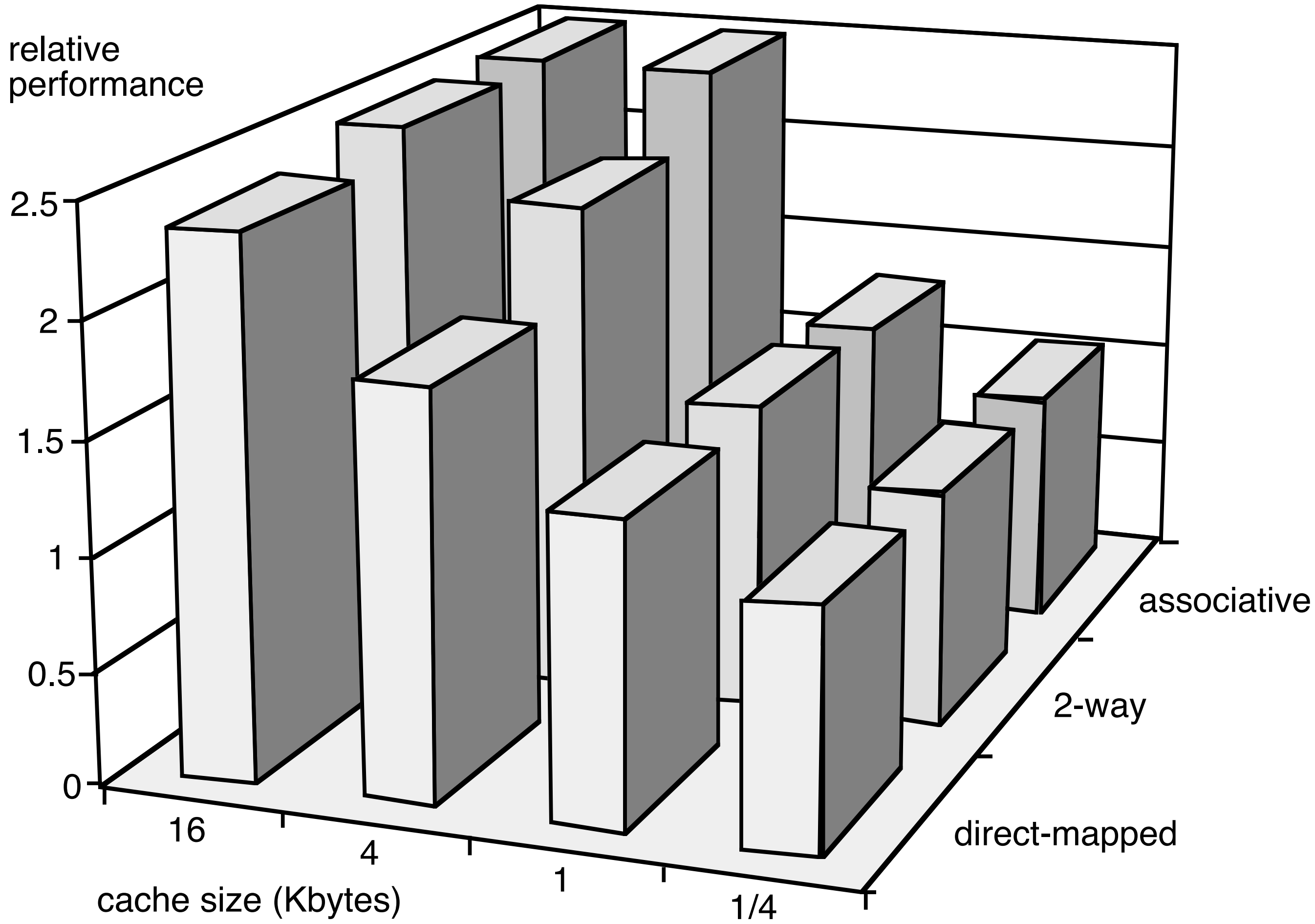
The ARM600 organization



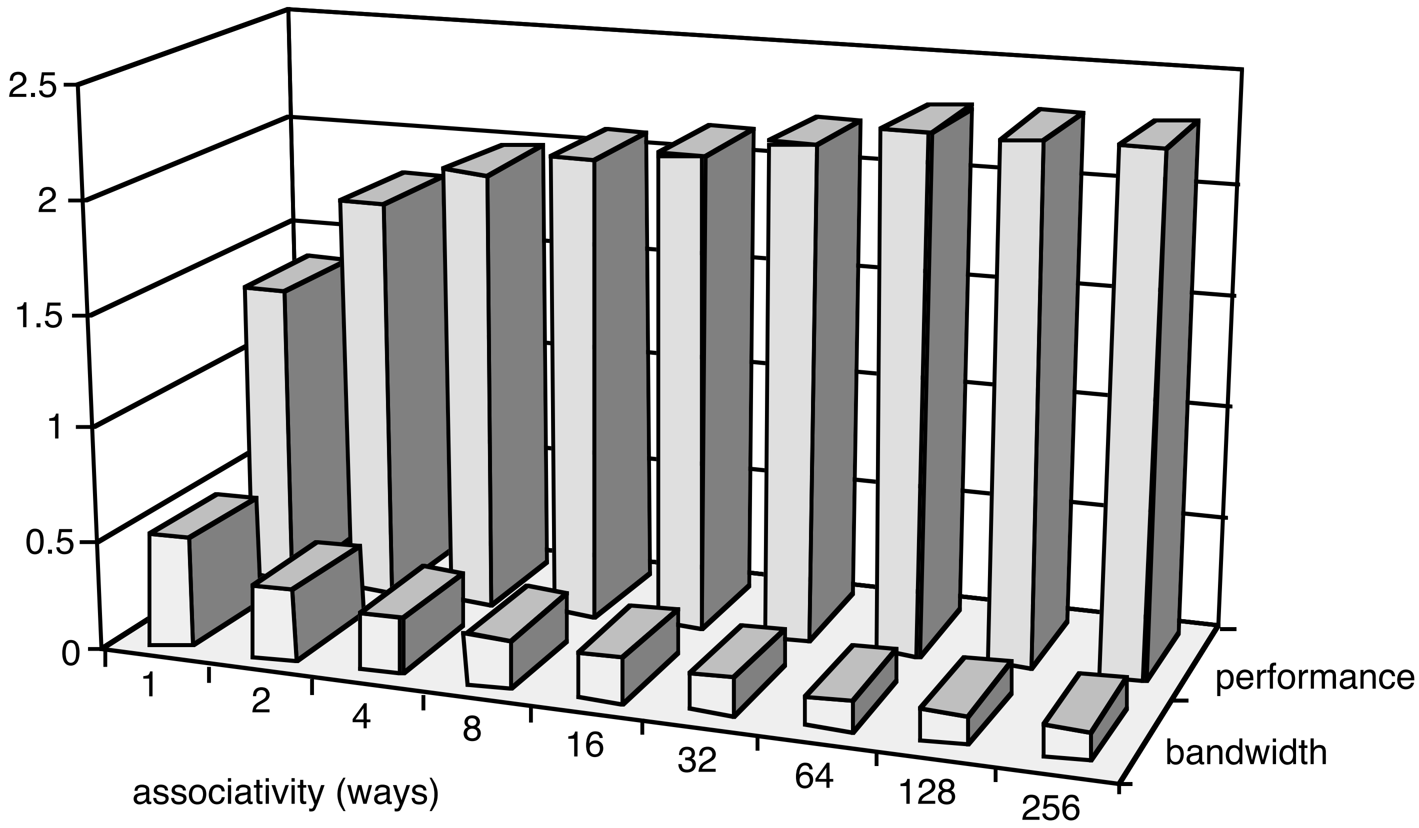
'Perfect' cache performance

Cache form	**Performance**
No cache	1
Instruction-only cache	1.95
Instruction and data cache	2.5
Data-only cache	1.13

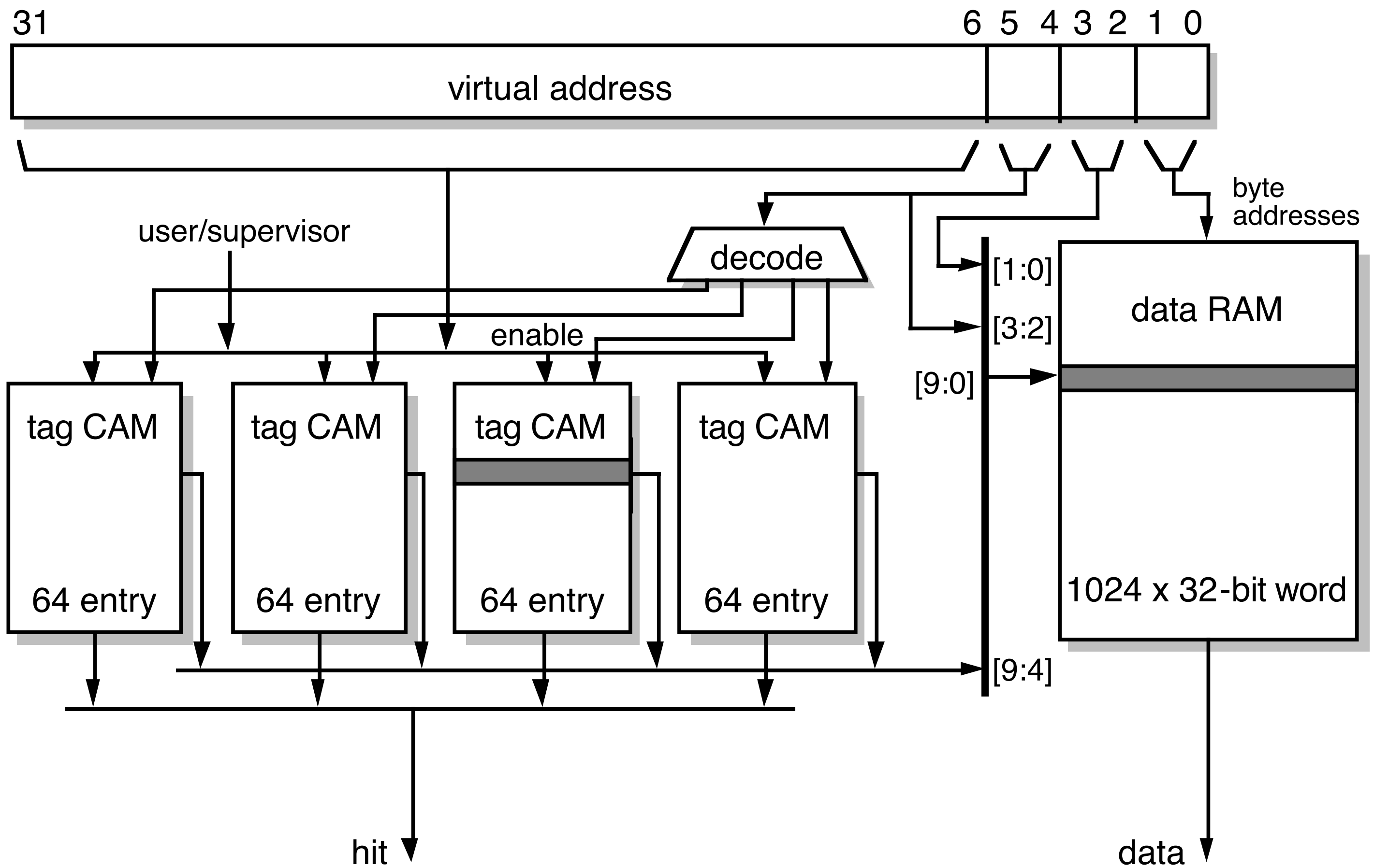
Unified cache performance as a function of size and organization



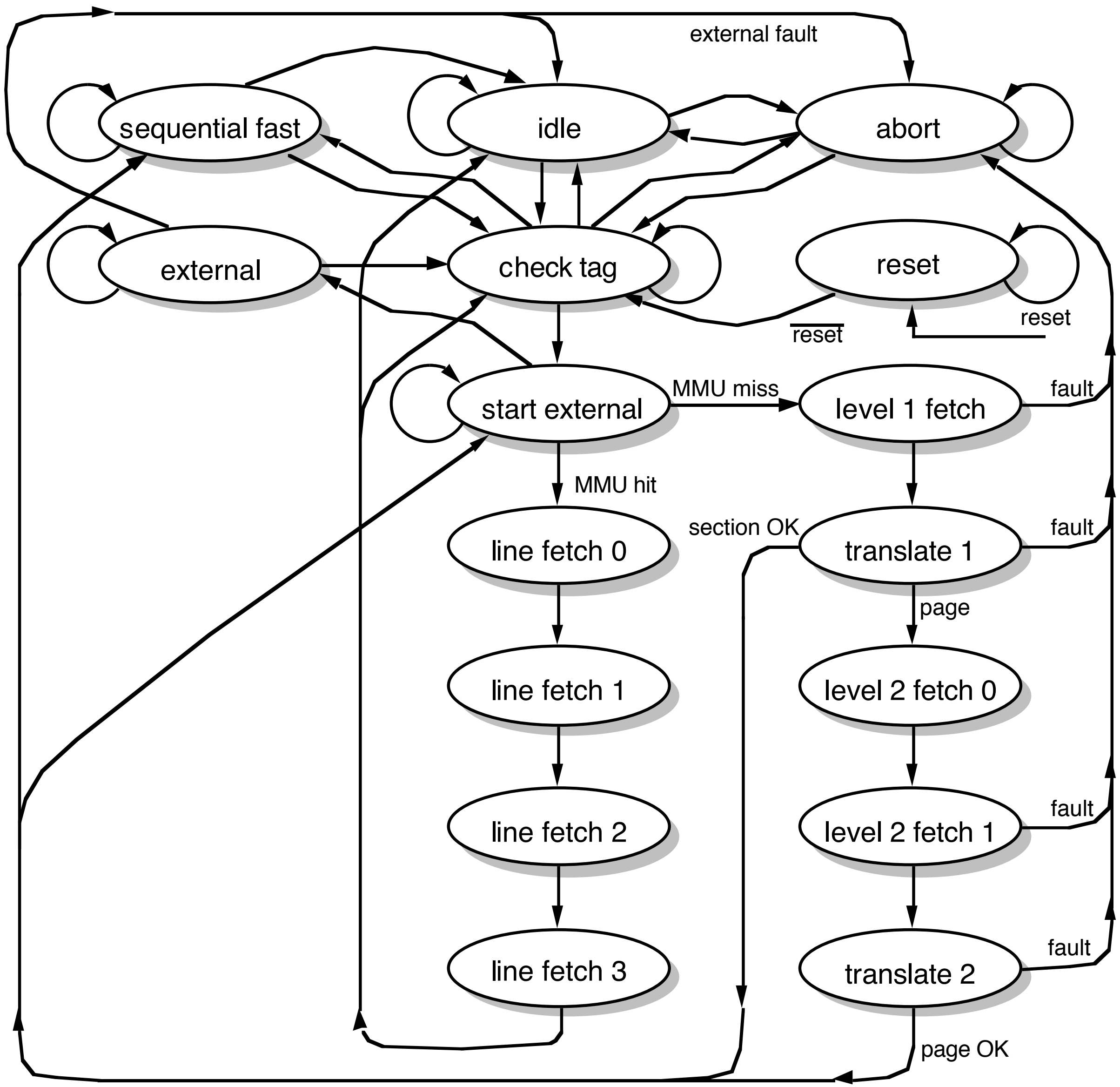
The effect of associativity on performance and bandwidth requirement



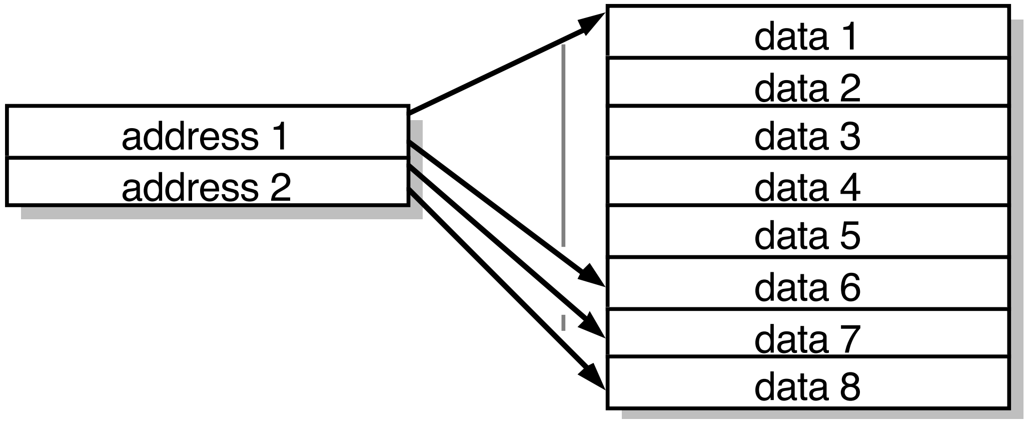
ARM600 cache organization



ARM600 cache control state machine



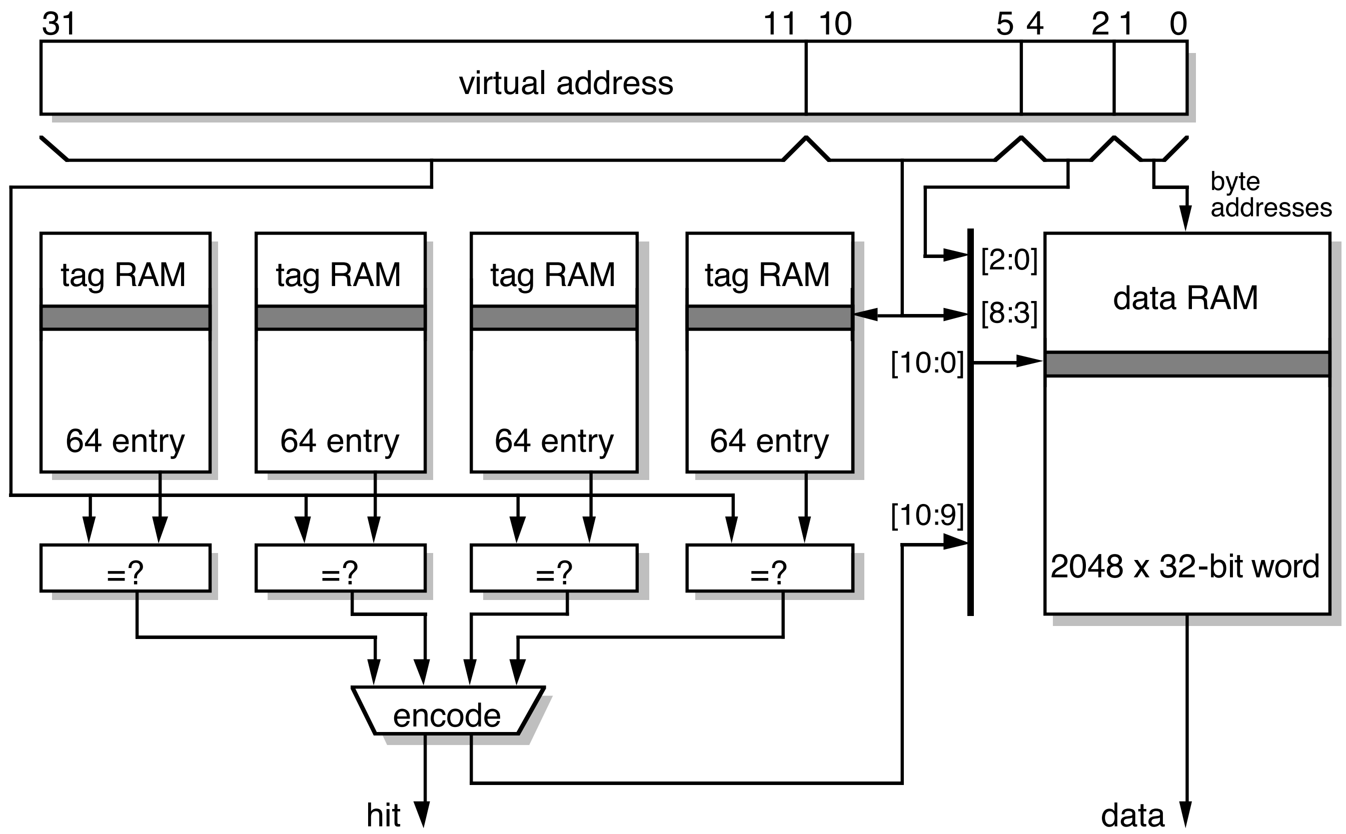
Write buffer mapping example



ARM610 characteristics

Process	0.6 µm	**Transistors**	358,931	**MIPS**	30
Metal layers	2	**Die area**	26 mm^2	**Power**	500 mW
Vdd	5 V	**Clock**	0 to 33 MHz	**MIPS/W**	60

The ARM700 cache organization



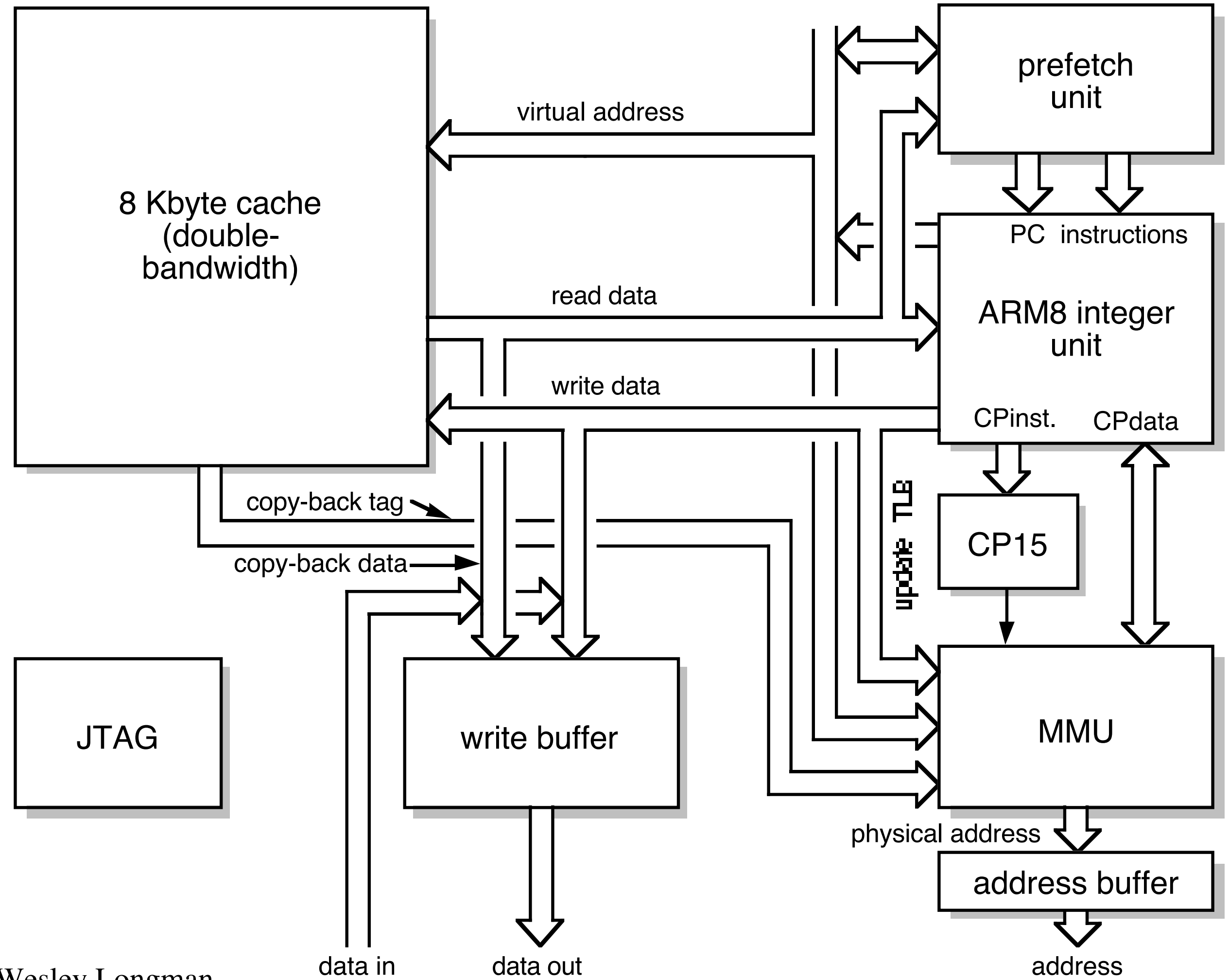
ARM700 characteristics

Process	0.8 µm	**Transistors**	578,977	**MIPS**	18/30
Metal layers	2	**Die area**	68 mm^2	**Power**	118/611 mW
Vdd	3.3/5 V	**Clock**	0 to 20/33 MHz	**MIPS/W**	152/49

ARM710 characteristics

Process	0.6 μm	**Transistors**	570,295	**MIPS**	23/36
Metal layers	2	**Die area**	34 mm^2	**Power**	120/500 mW
Vdd	3.3/5 V	**Clock**	0 to 25/40 MHz	**MIPS/W**	192/72

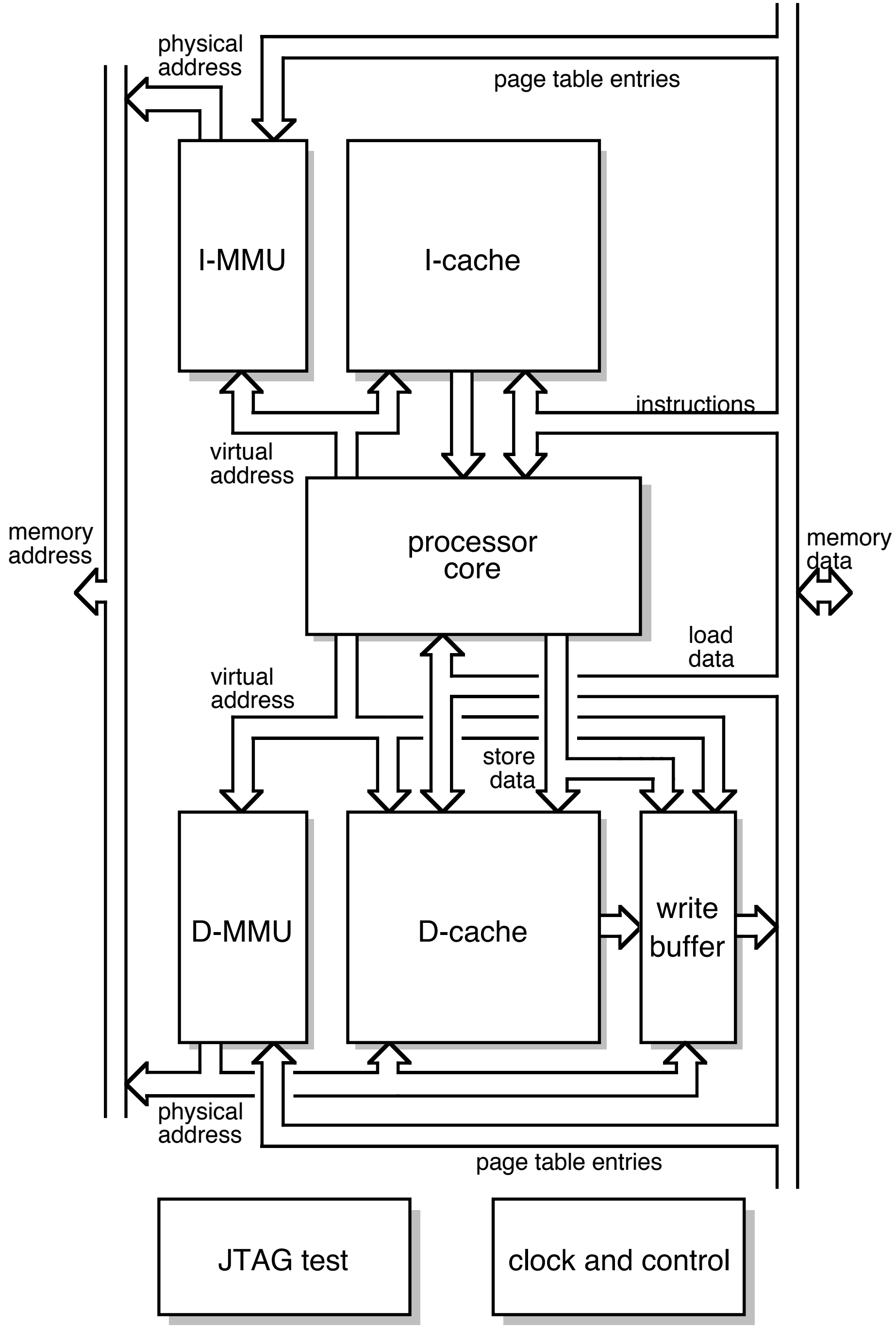
ARM810 organization



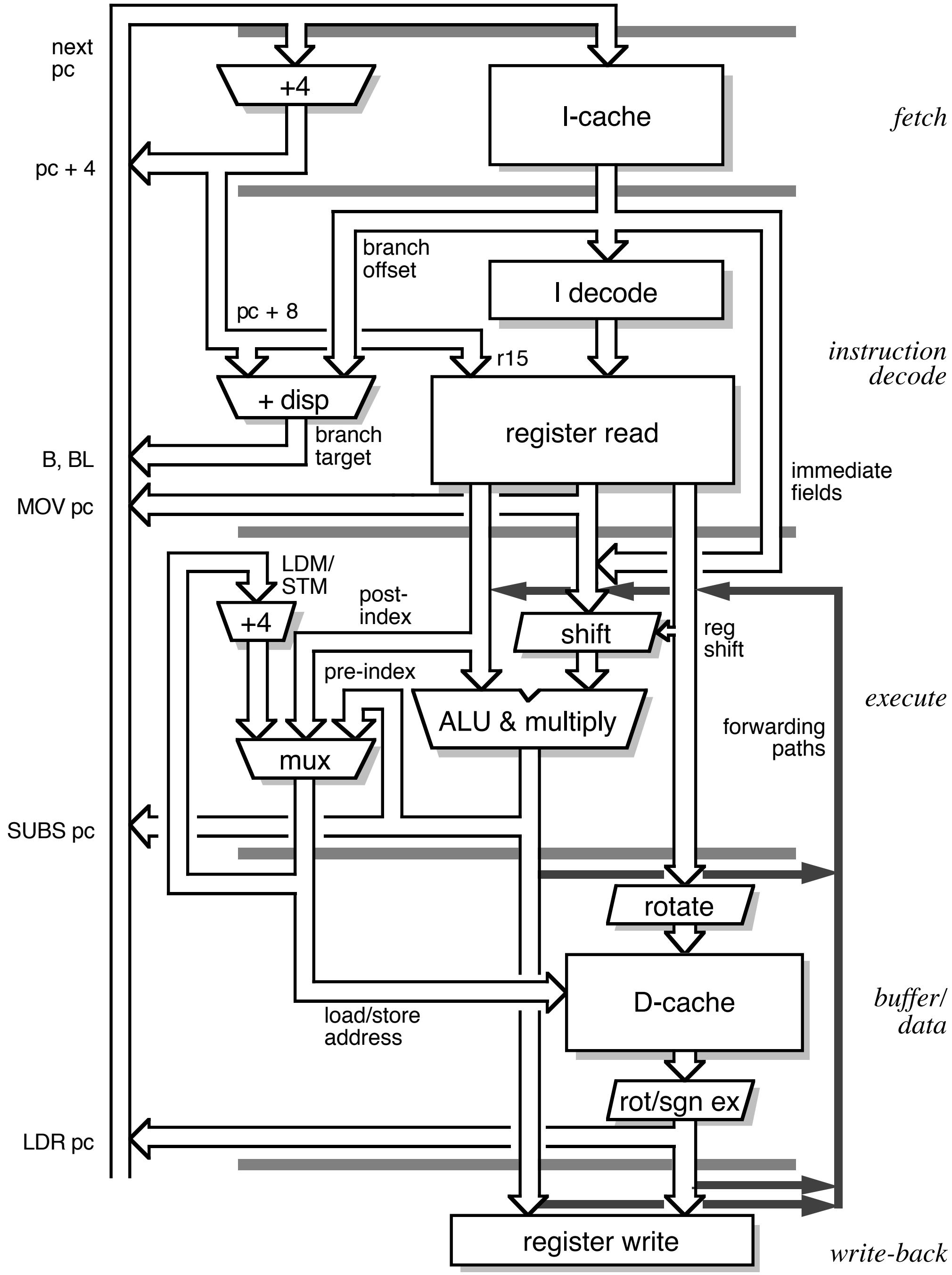
ARM810 characteristics

Process	0.5 μm	**Transistors**	836,022	**MIPS**	86
Metal layers	3	**Die area**	76 mm^2	**Power**	500 mW
Vdd	3.3 V	**Clock**	0 to 72 MHz	**MIPS/W**	172

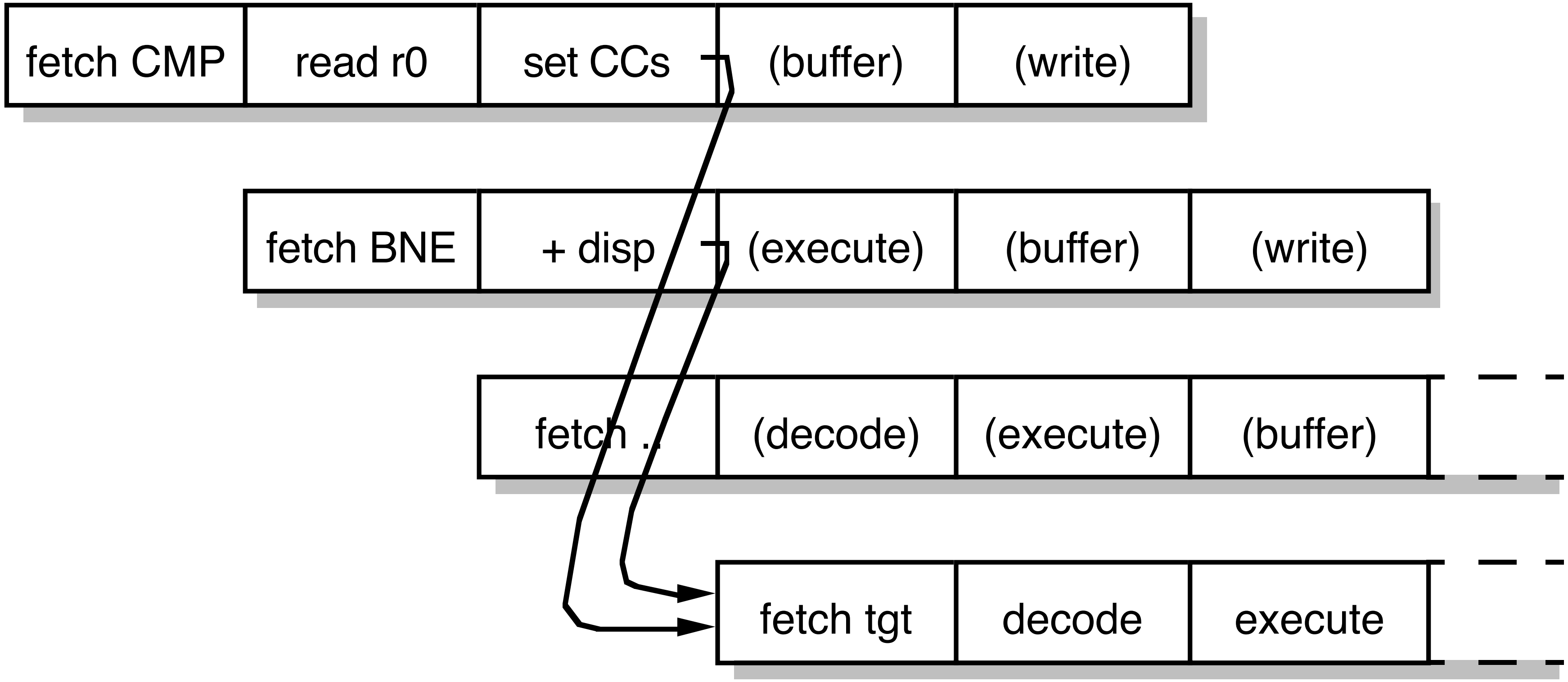
StrongARM organization



StrongARM core pipeline organization



StrongARM loop test pipeline behaviour



StrongARM characteristics

Process	0.35 µm	**Transistors**	2,500,000	**MIPS**	201/251
Metal layers	3	**Die area**	50 mm^2	**Power**	450/900 mW
Vdd	1.65/2 V	**Clock**	160/200 MHz	**MIPS/W**	448/279