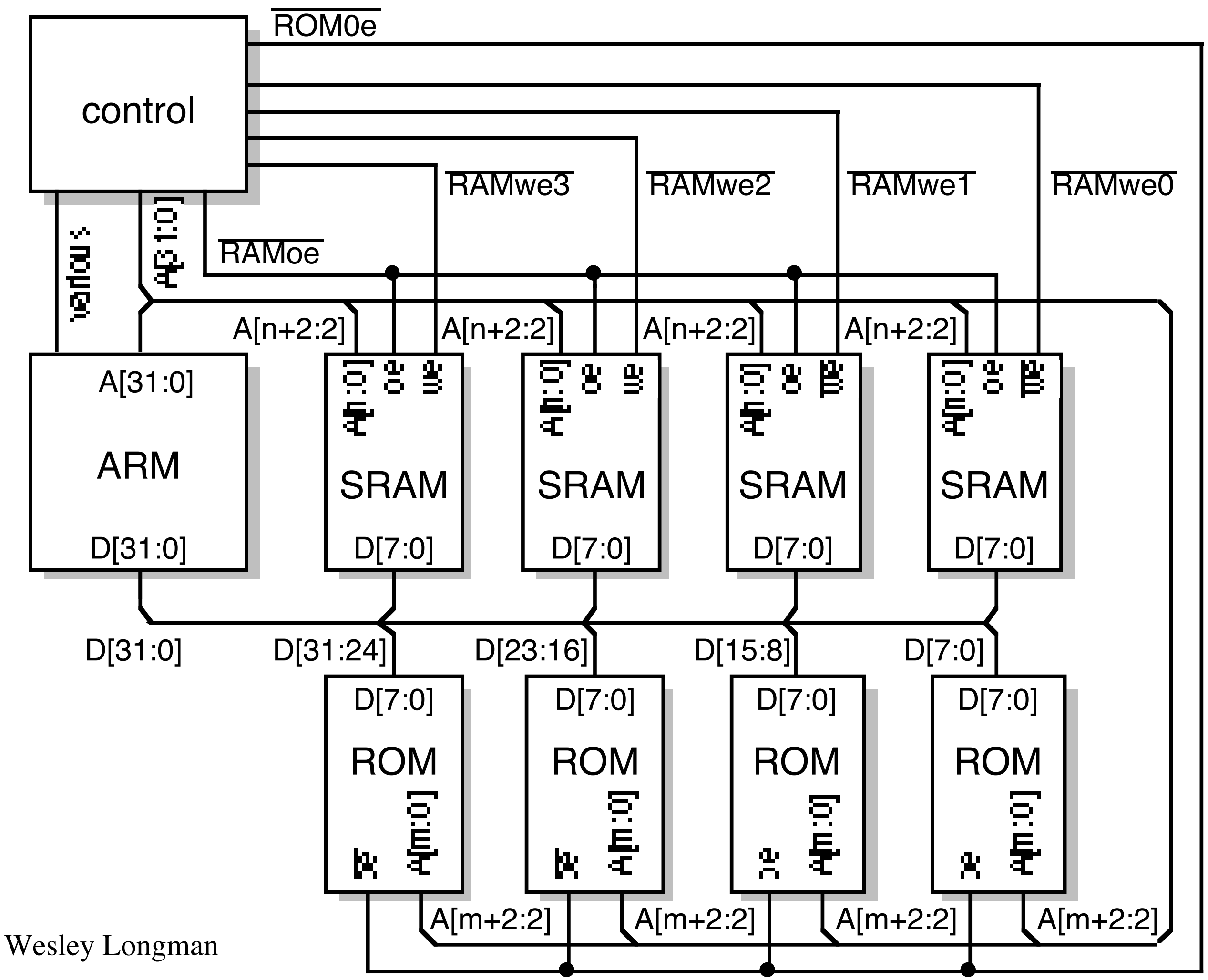
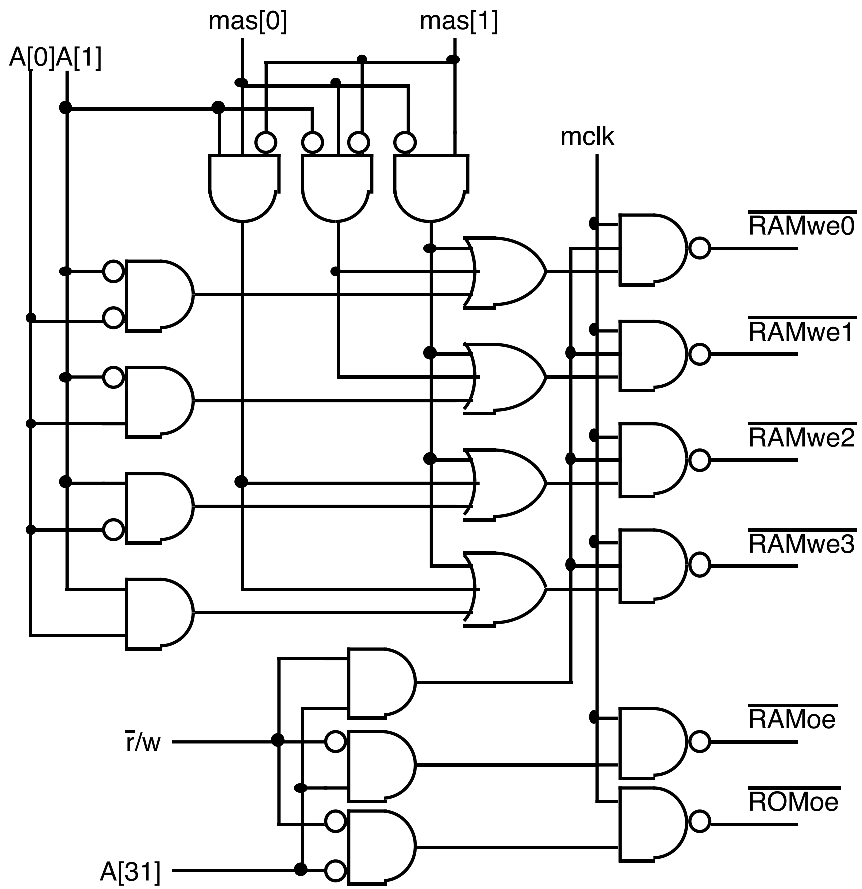
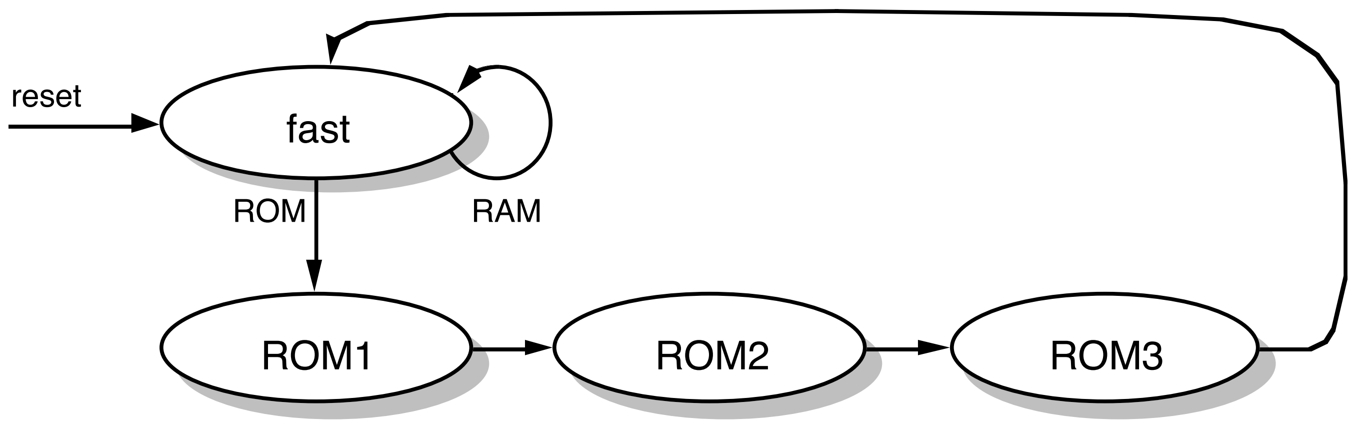
A basic ARM memory system



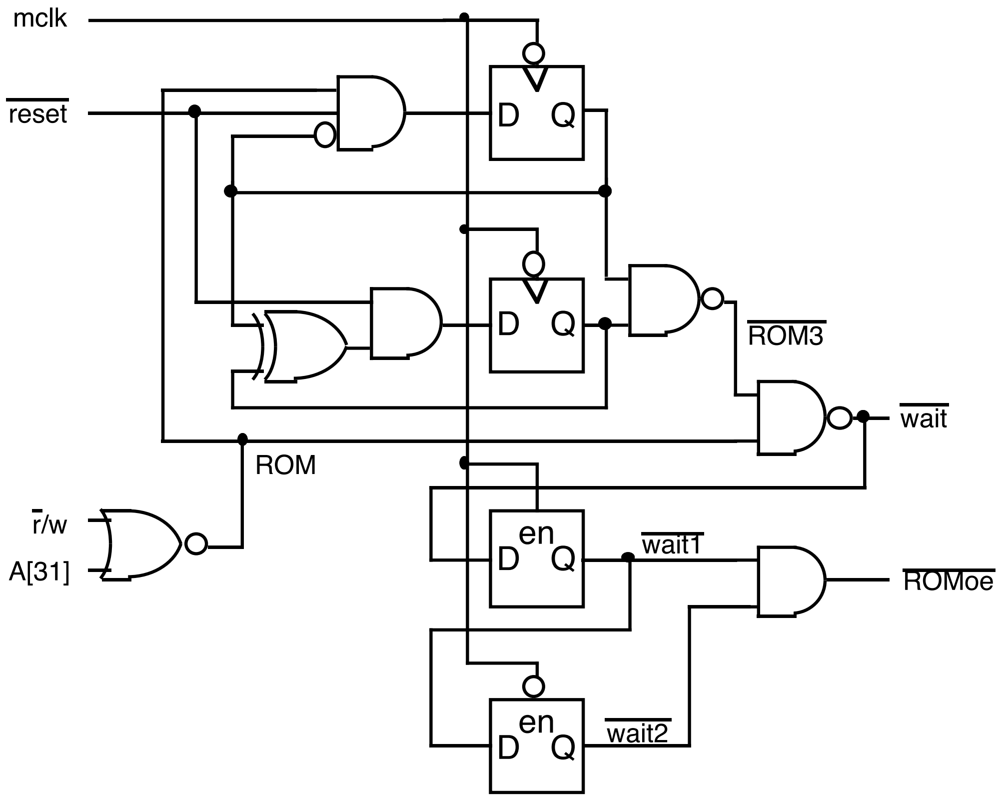
Simple ARM memory system control logic



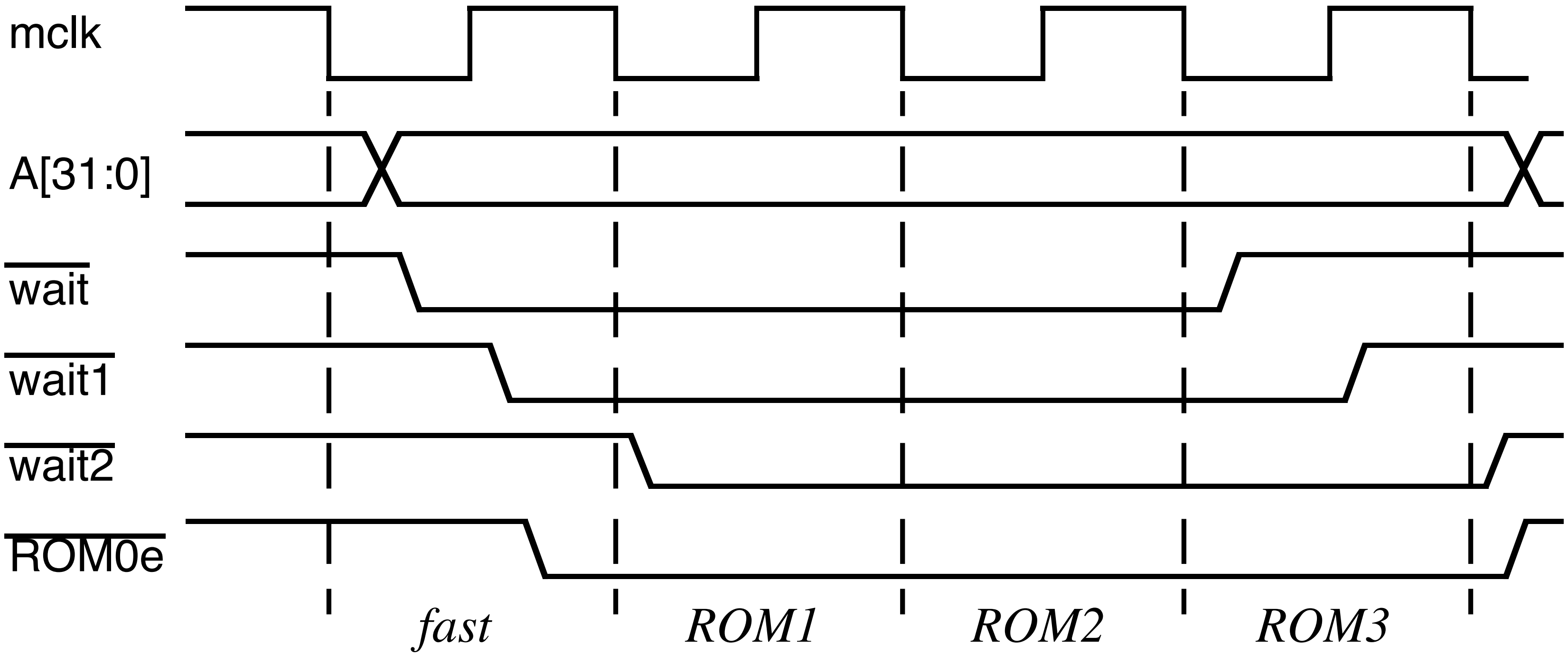
ROM wait control state transition diagram



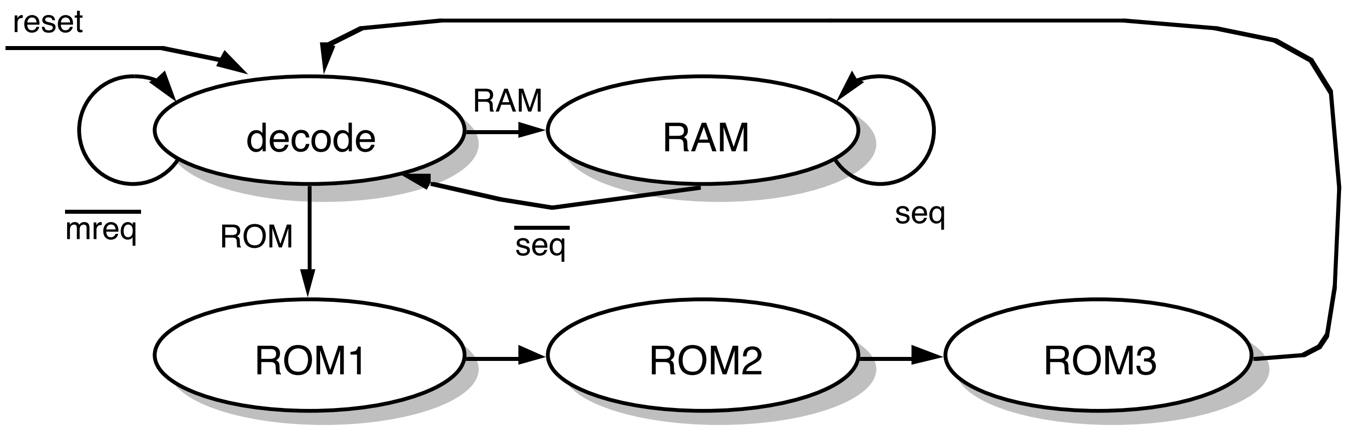
ROM wait state generator circuit



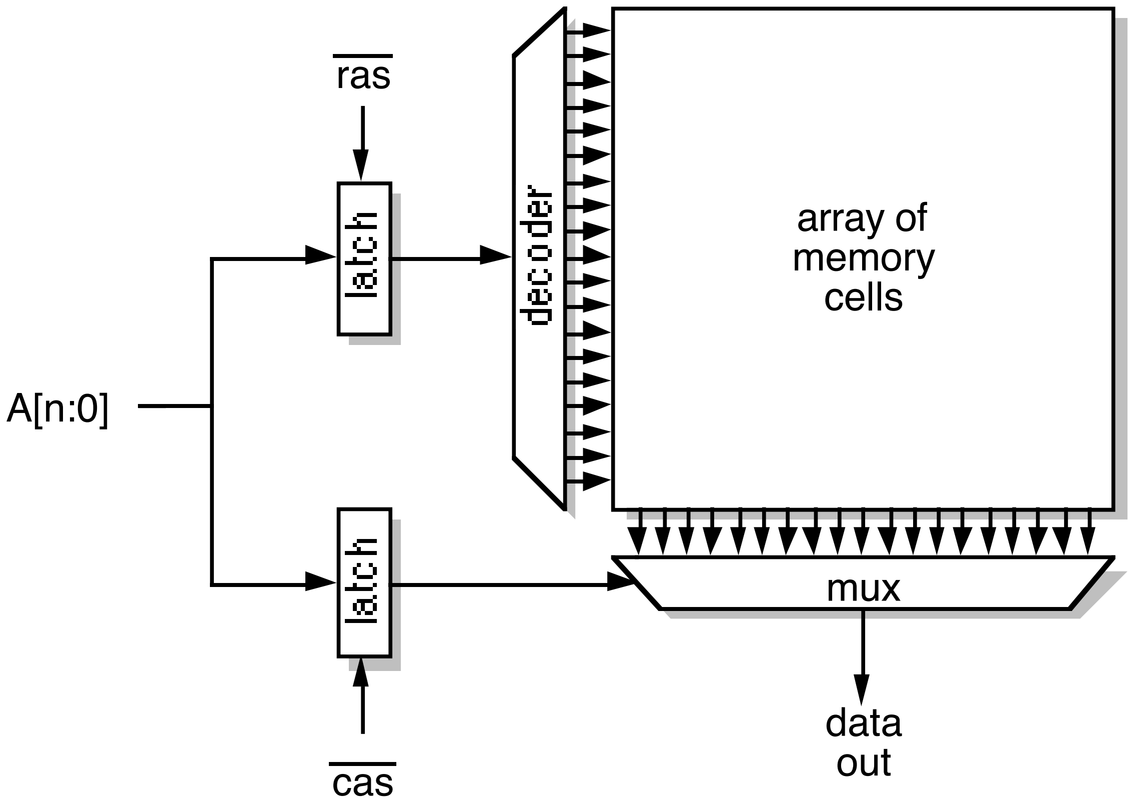
The timing diagram for the ROM wait state logic



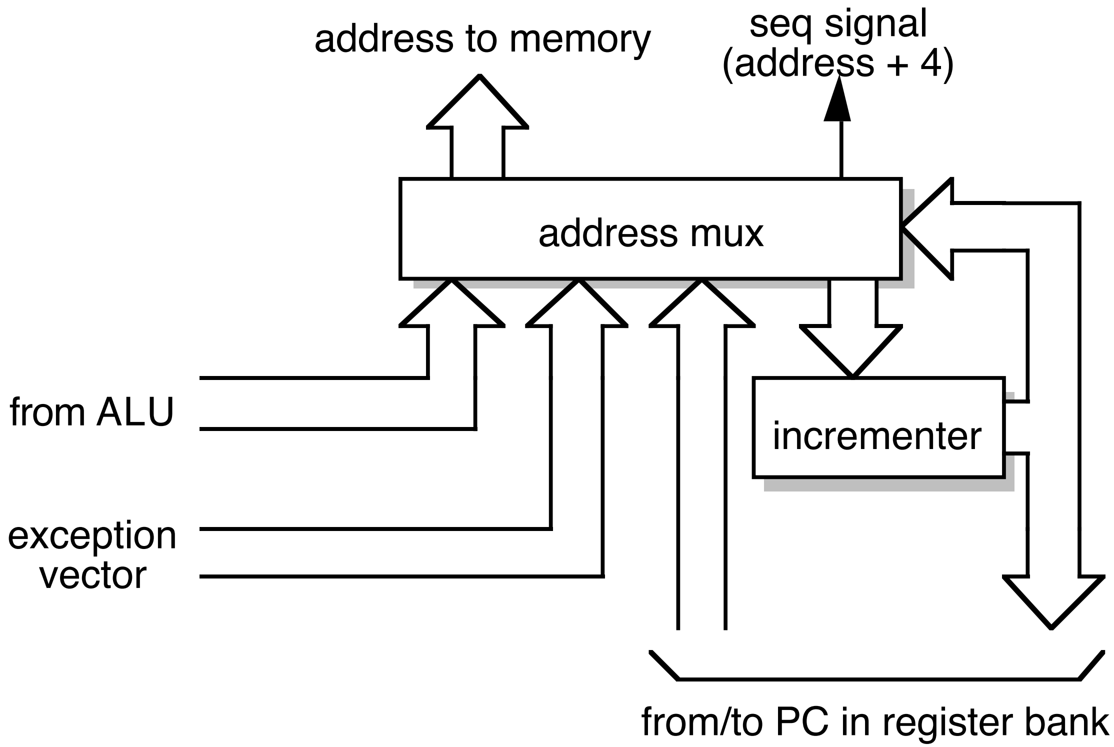
State transition diagram with a wait state for address decoding



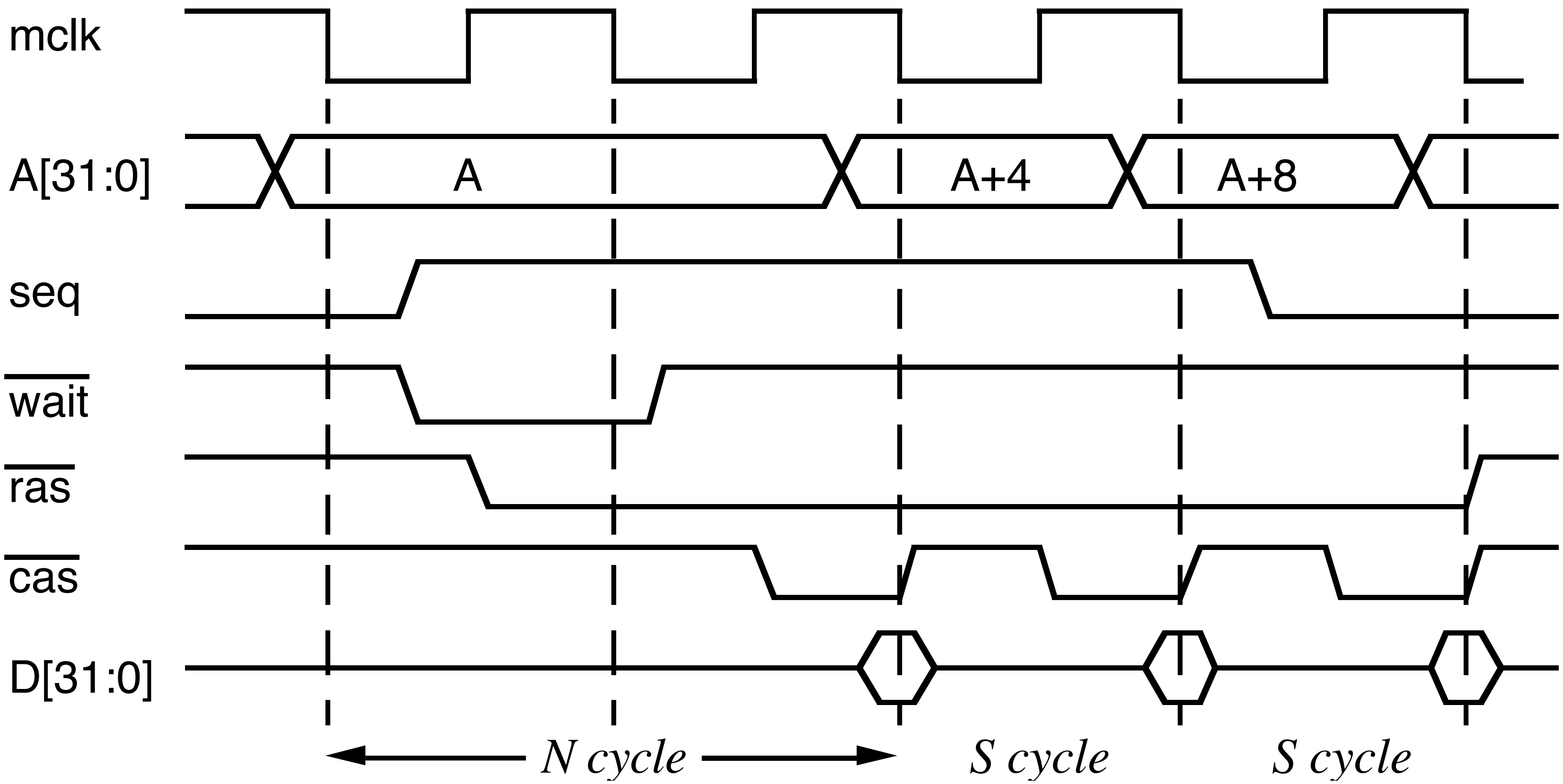
DRAM memory organization



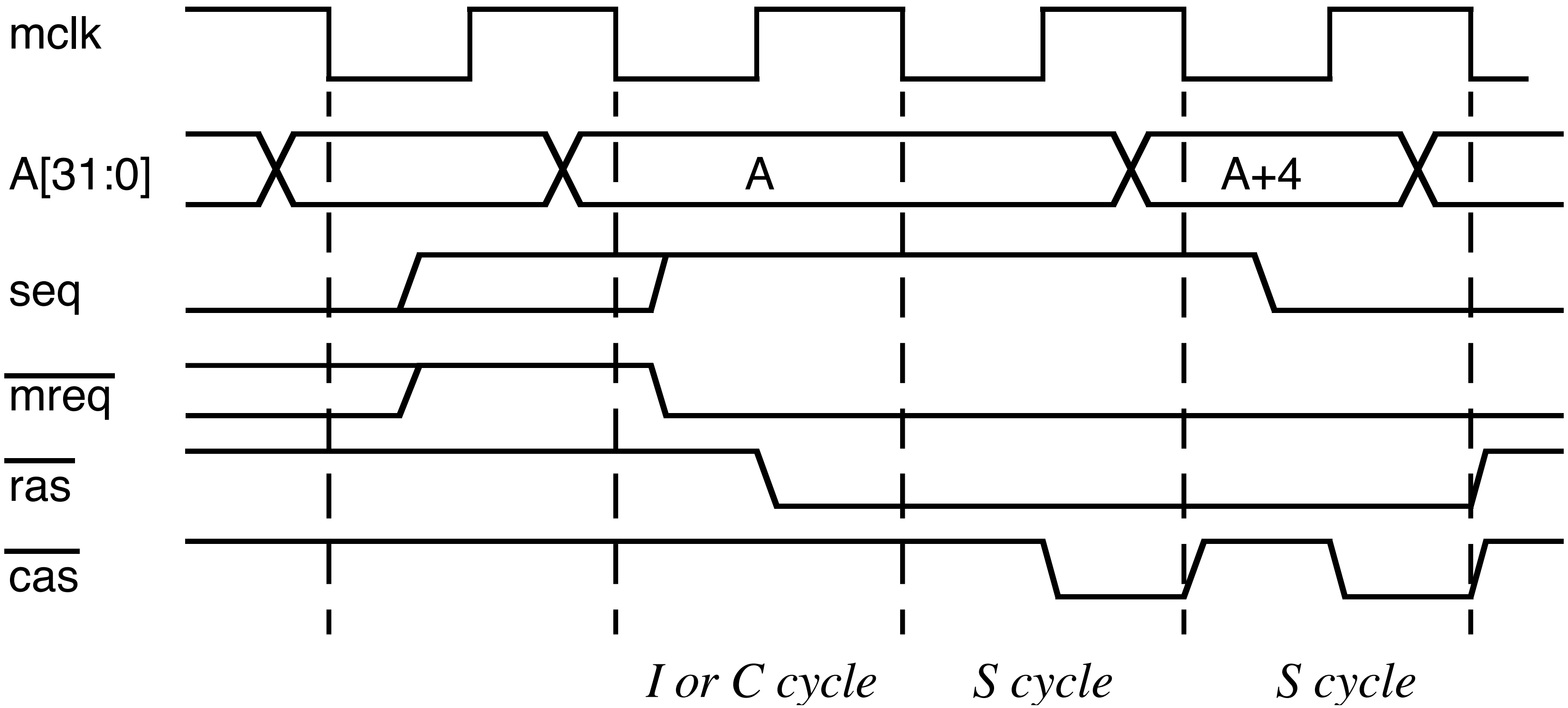
ARM address register structure



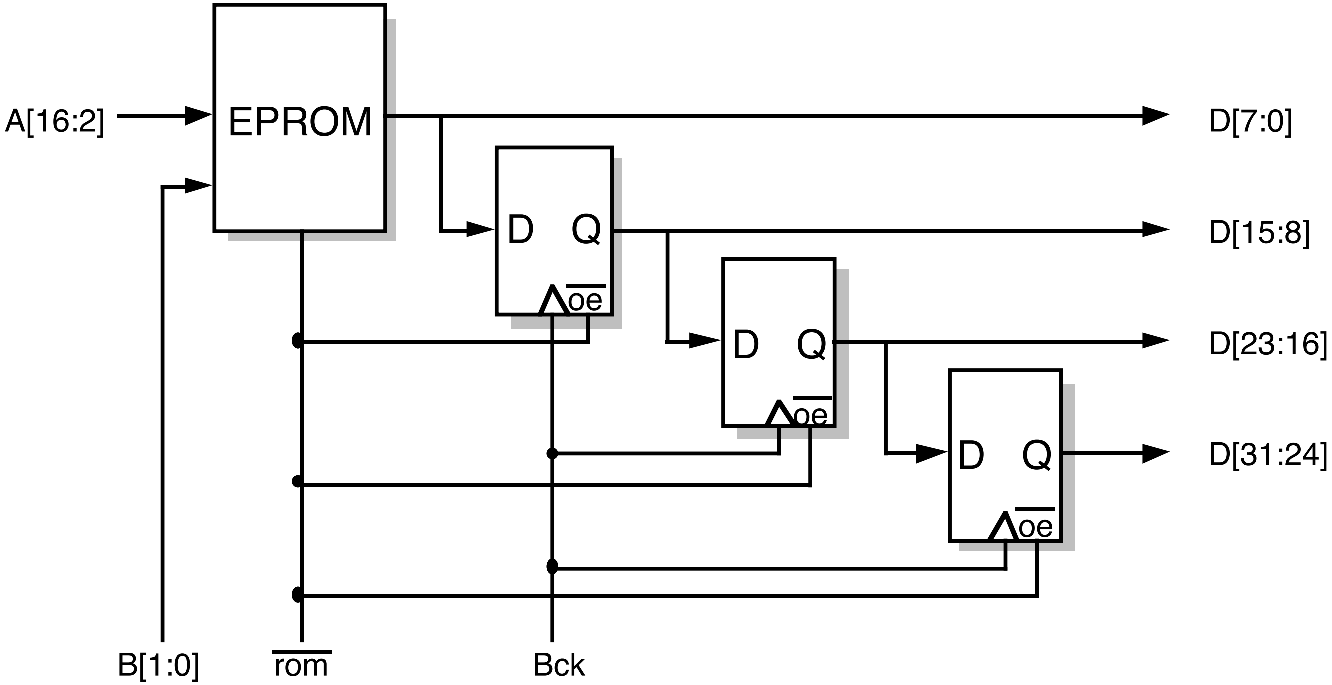
DRAM timing illustration



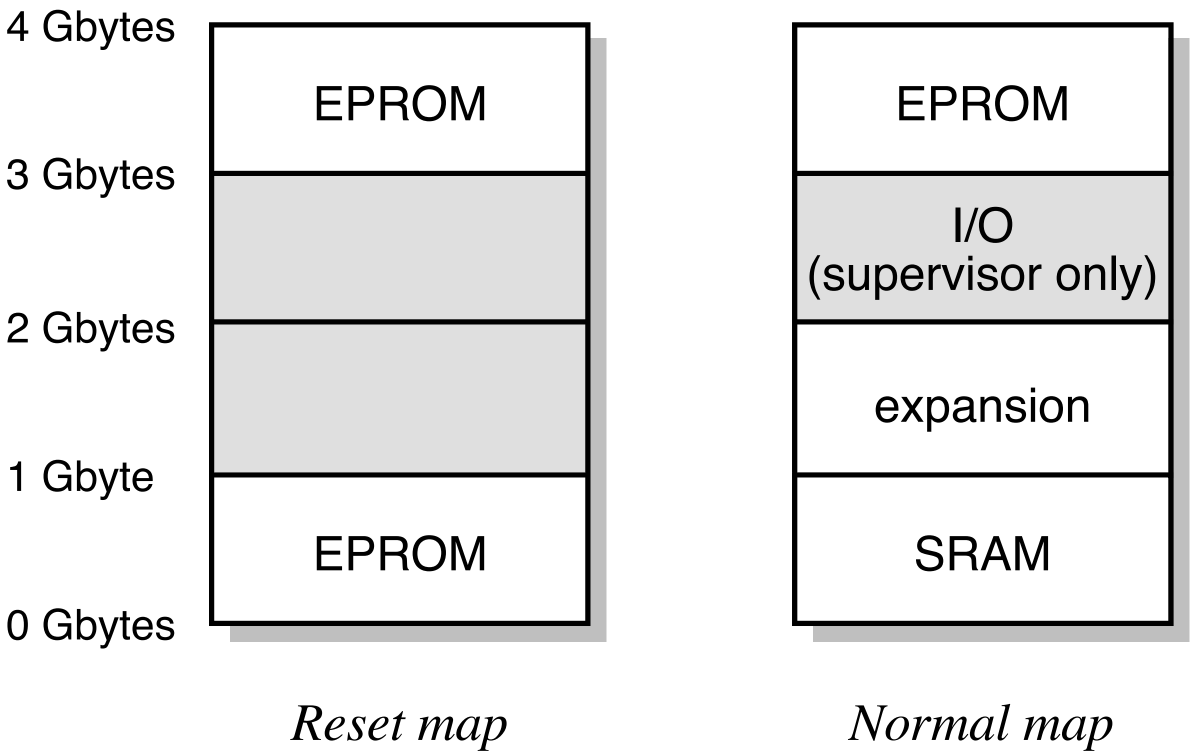
DRAM timing after an internal cycle



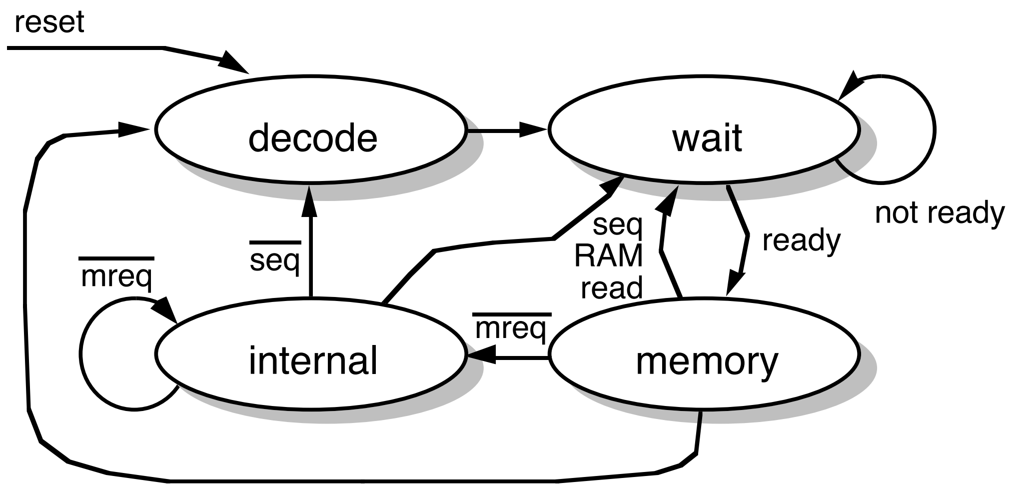
The PIE card EPROM pipeline



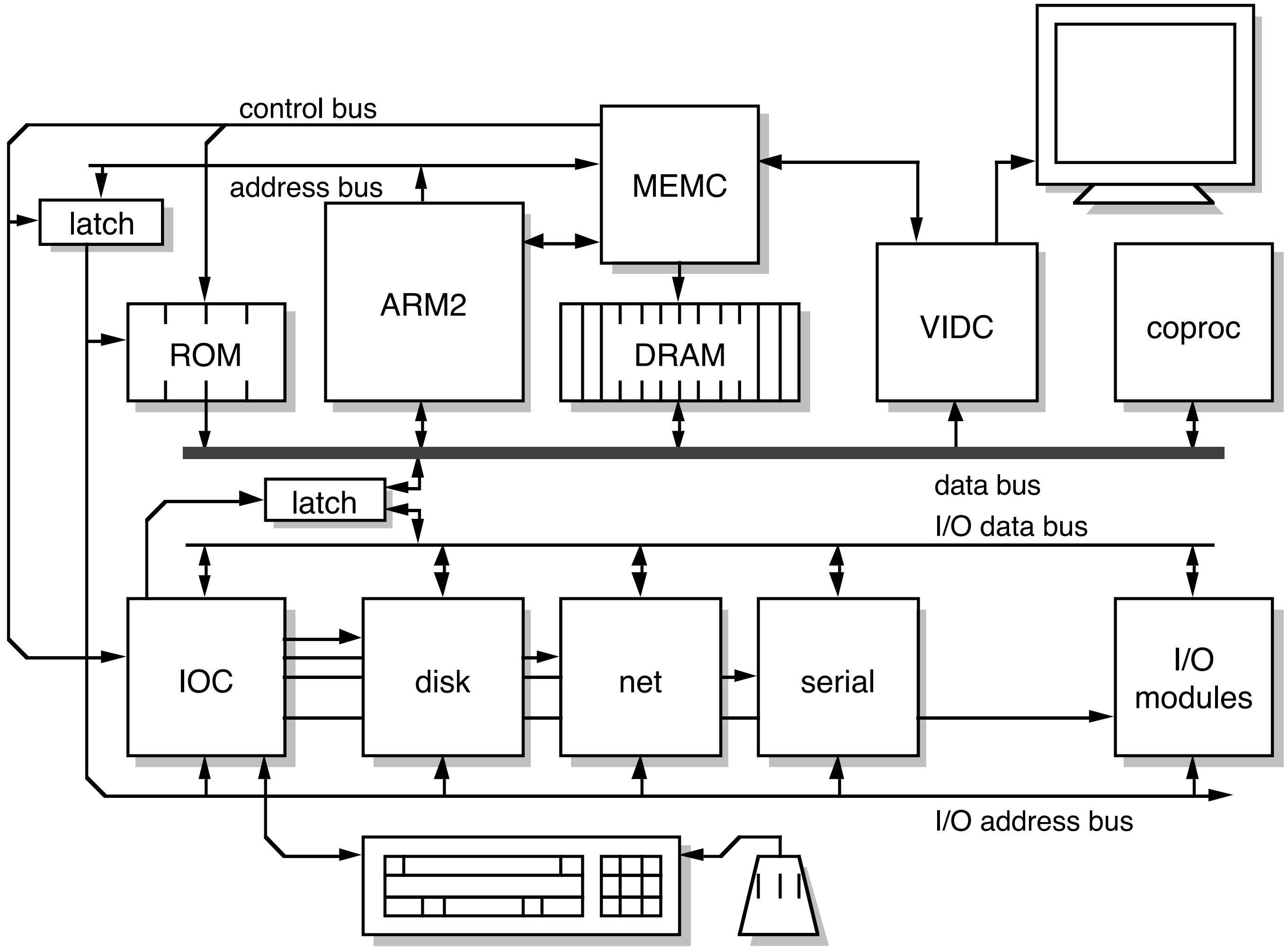
PIE card memory maps



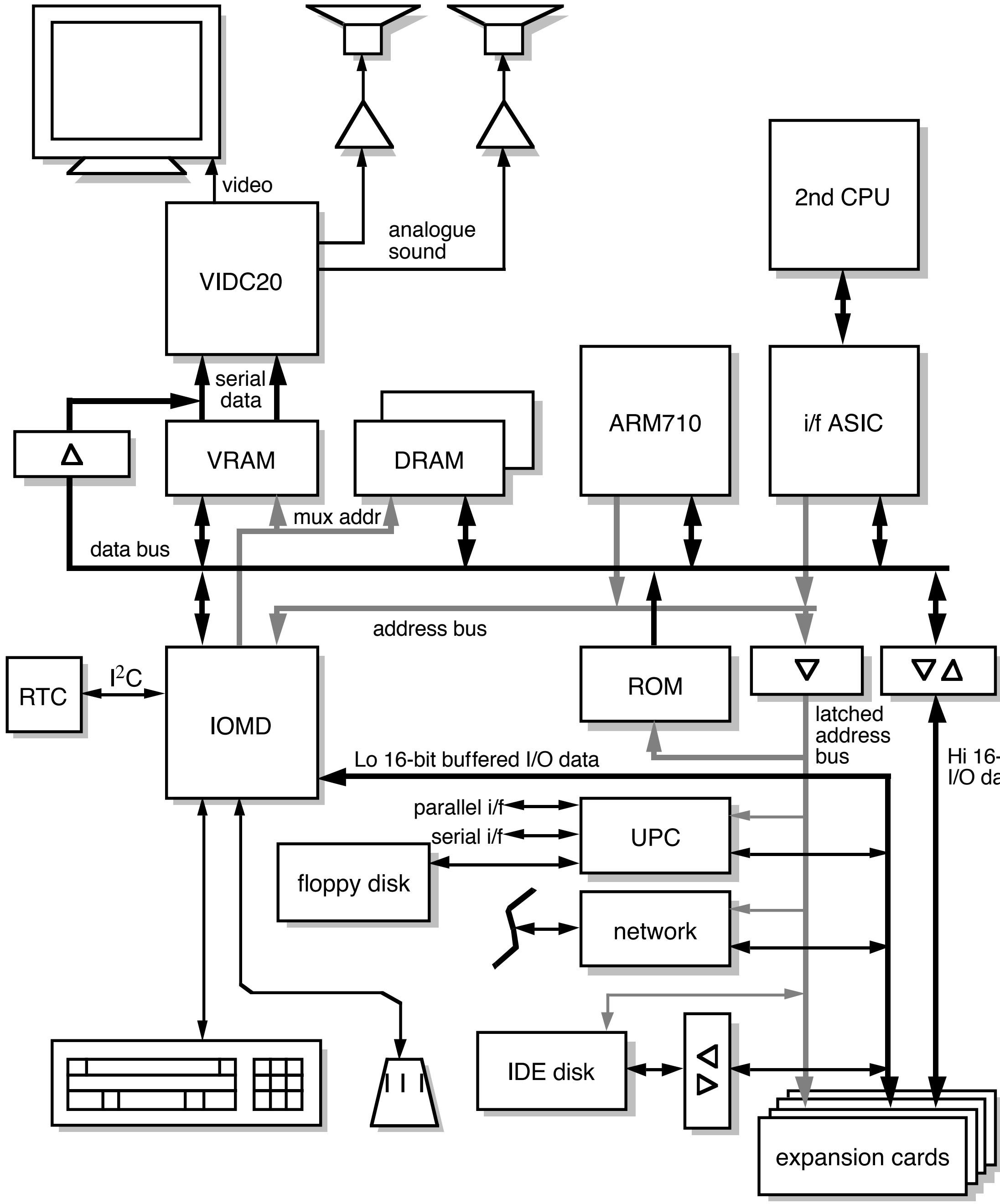
PIE card memory access state transition diagram



Archimedes system organization



Risc PC system organization



The Newton MessagePad hardware organization