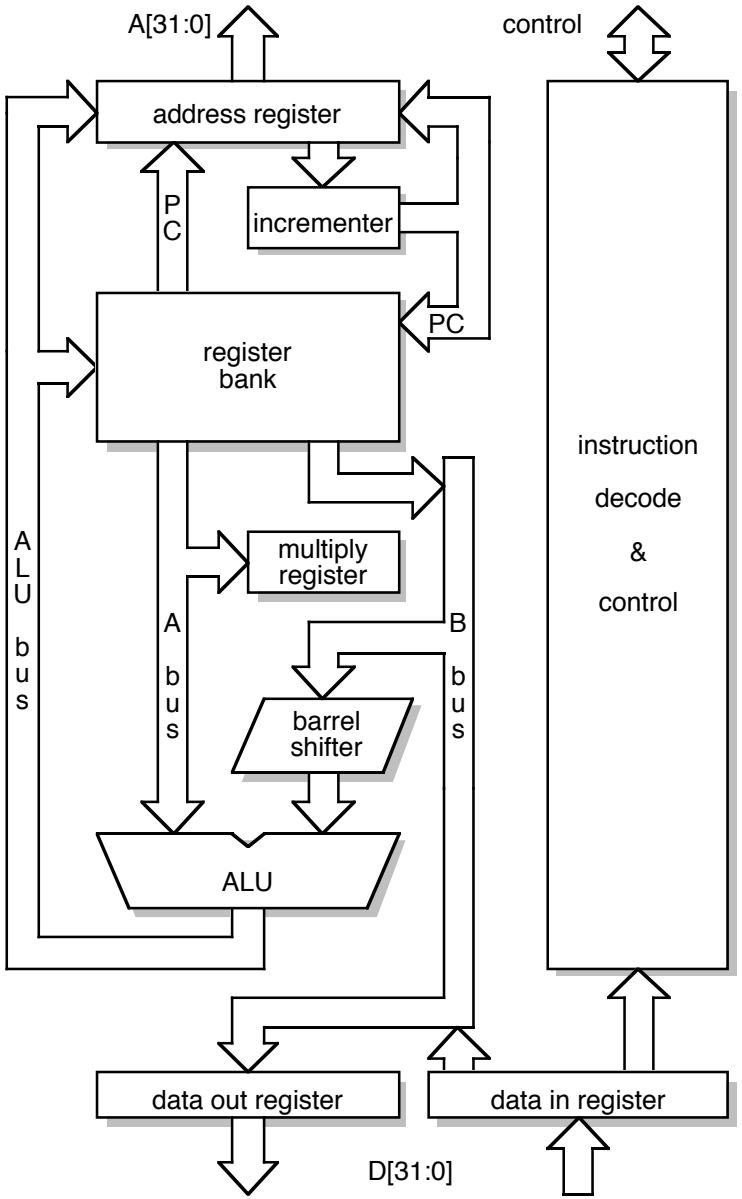
ARM organization



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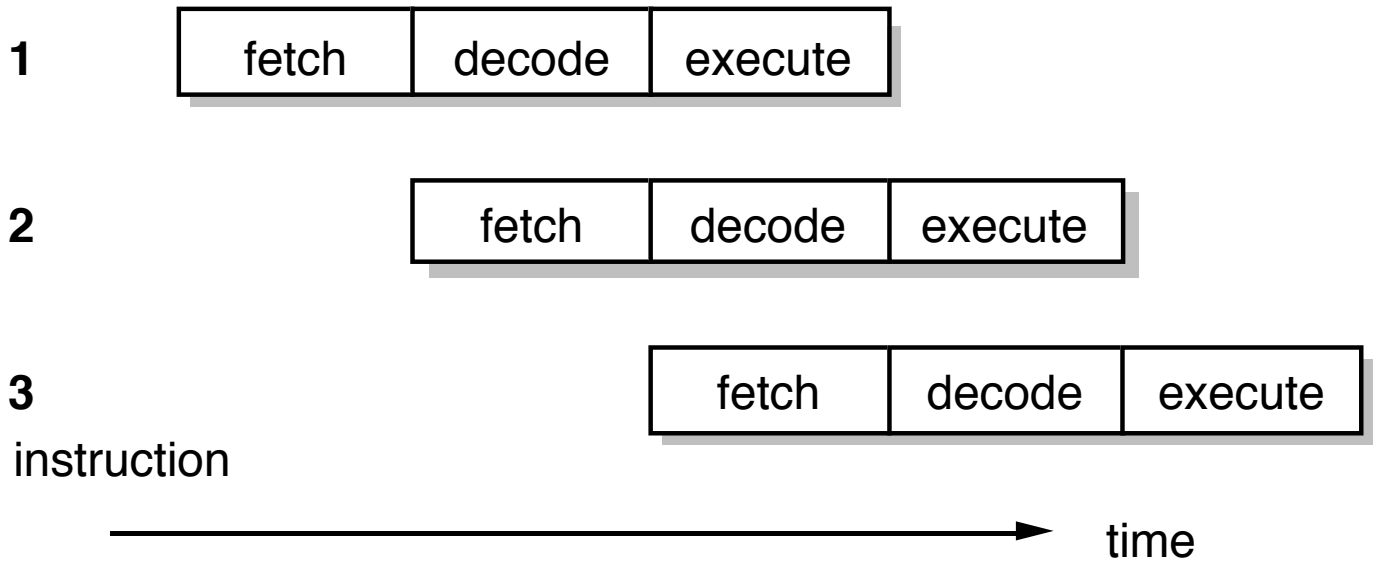
ARM single-cycle instruction pipeline operation



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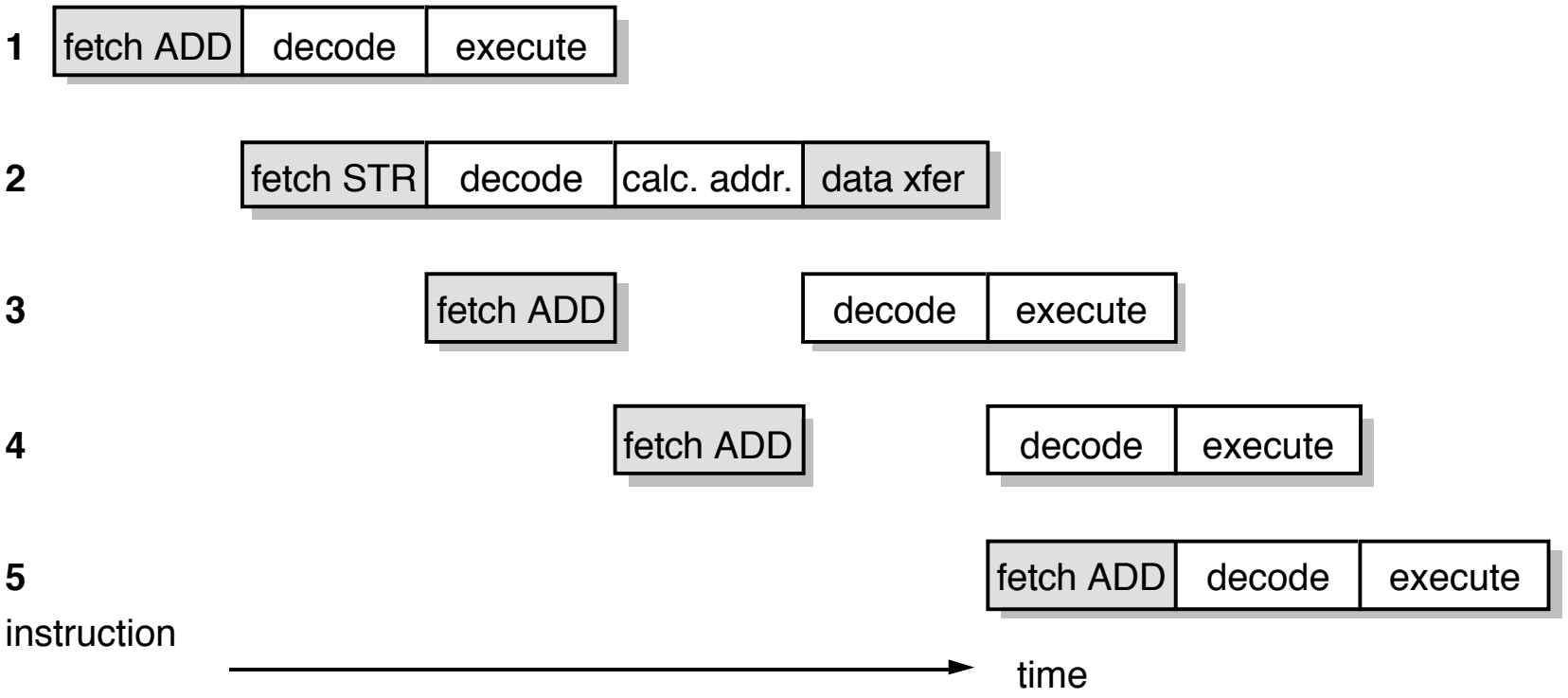
ARM multi-cycle instruction pipeline operation



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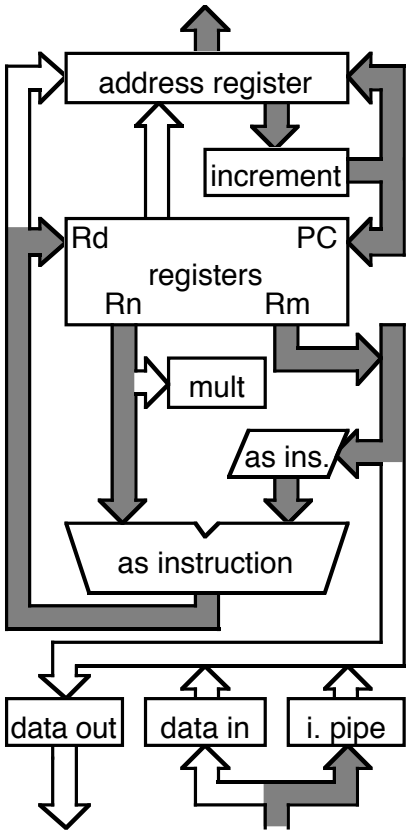
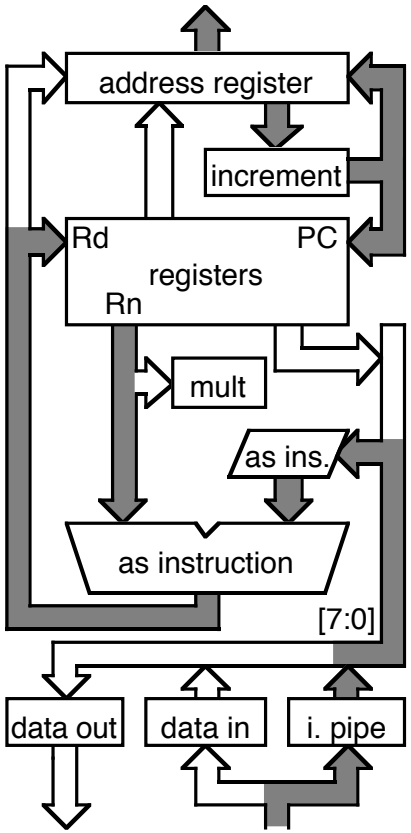
Data processing instruction datapath activity



(a) register - register operations



(b) register - immediate operations

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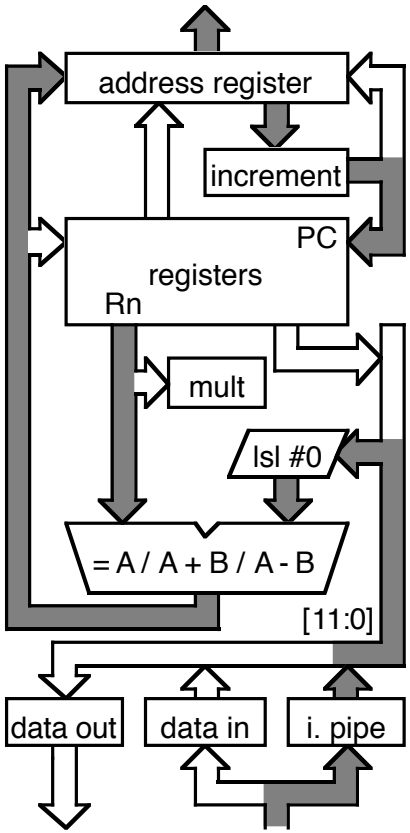
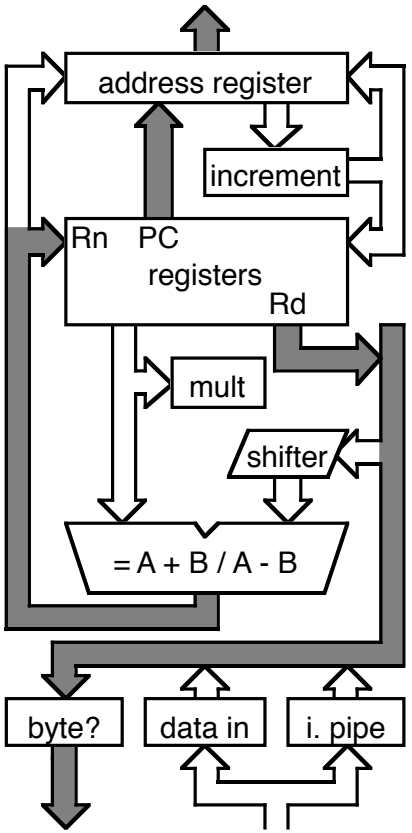
STR (store register) datapath activity



(a) 1st cycle - compute address



(b) 2nd cycle - store data & auto-index

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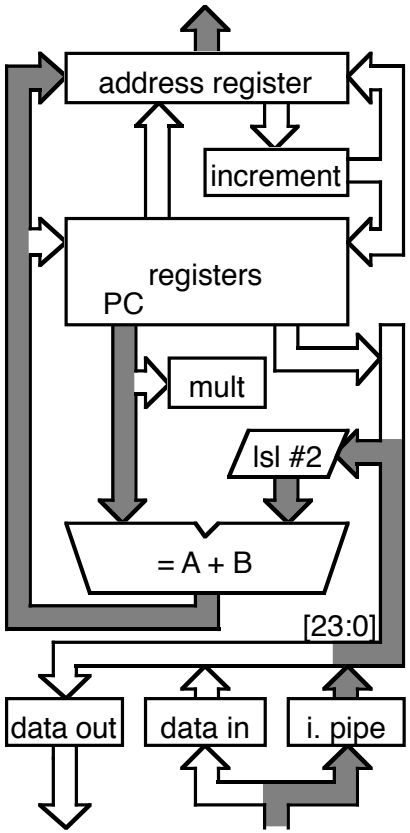
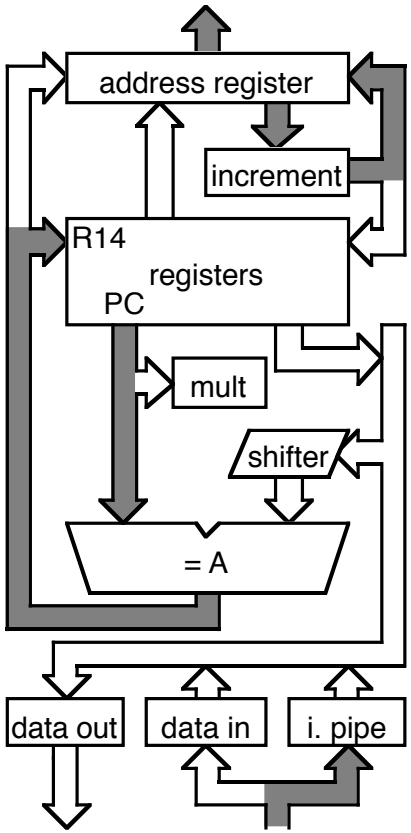
The first two (of three) cycles of a branch instruction



(a) 1st cycle - compute branch target



(b) 2nd cycle - save return address

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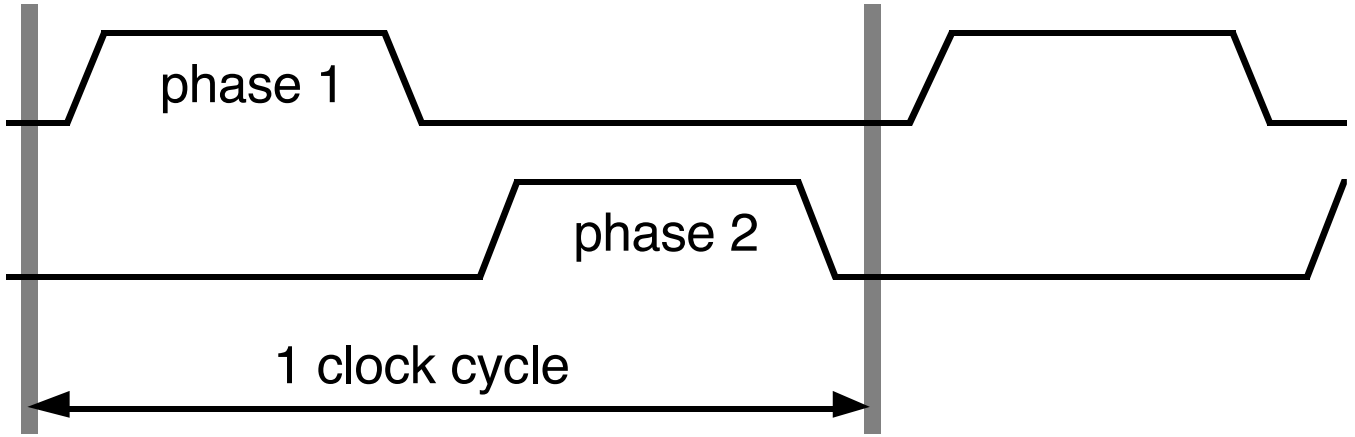
2-phase non-overlapping clock scheme



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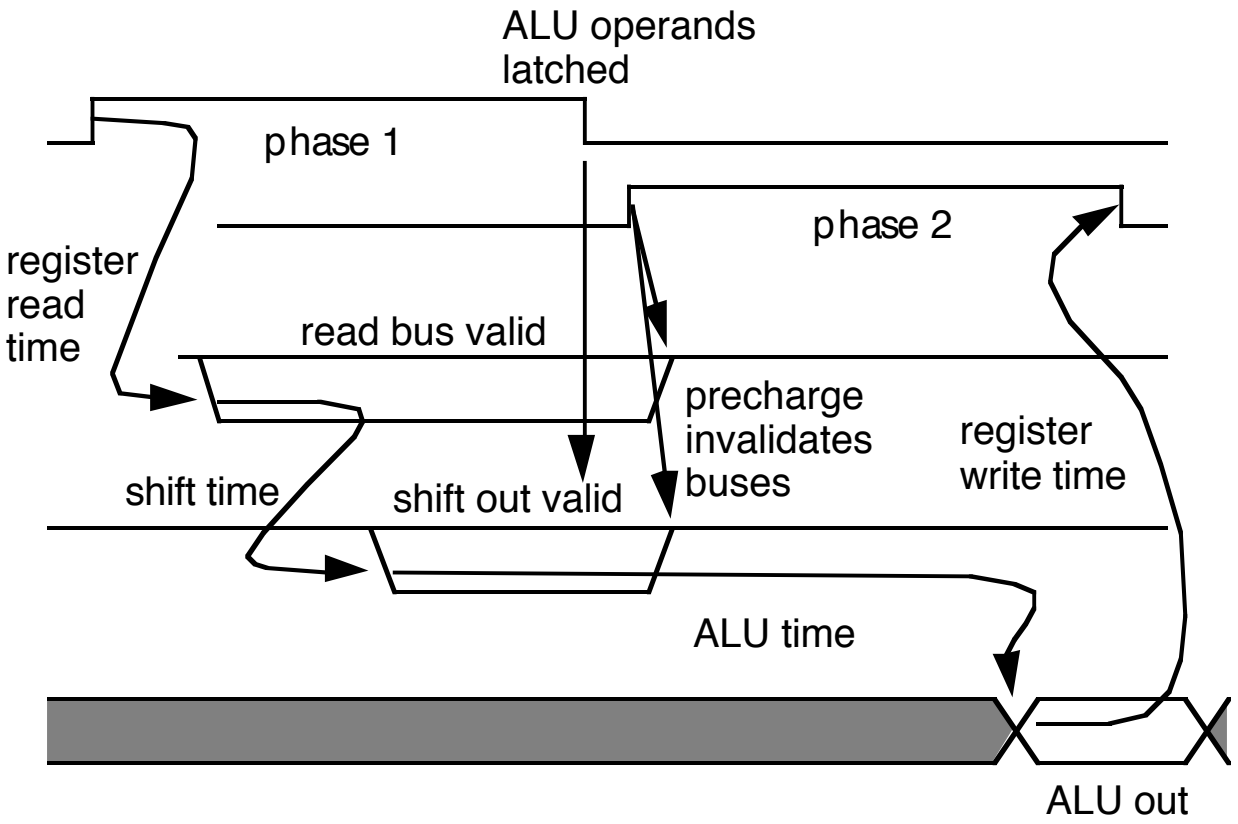
ARM datapath timing



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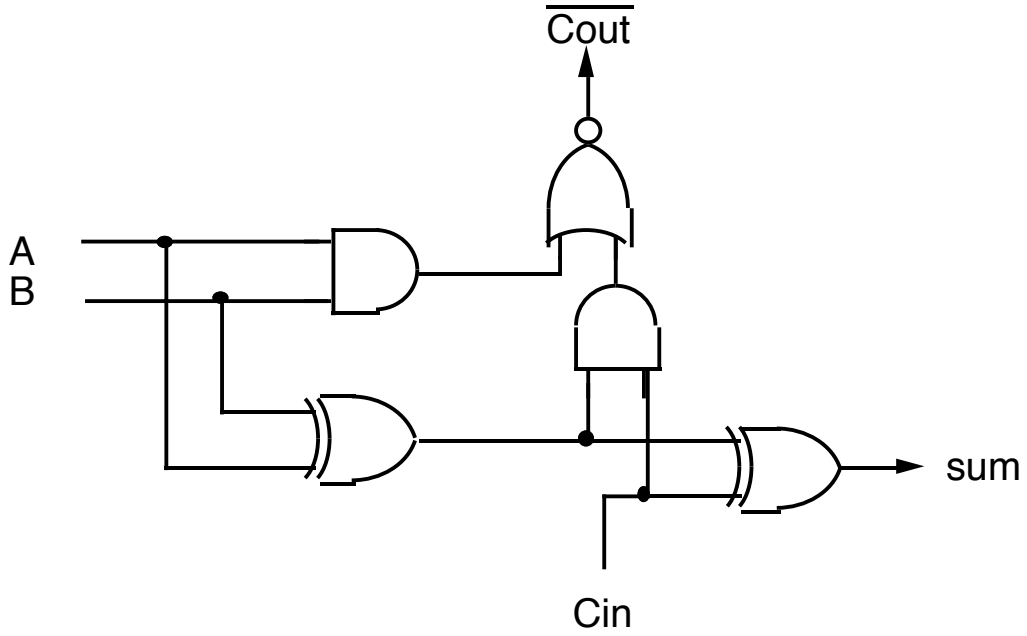
The original ARM1 ripple-carry adder circuit



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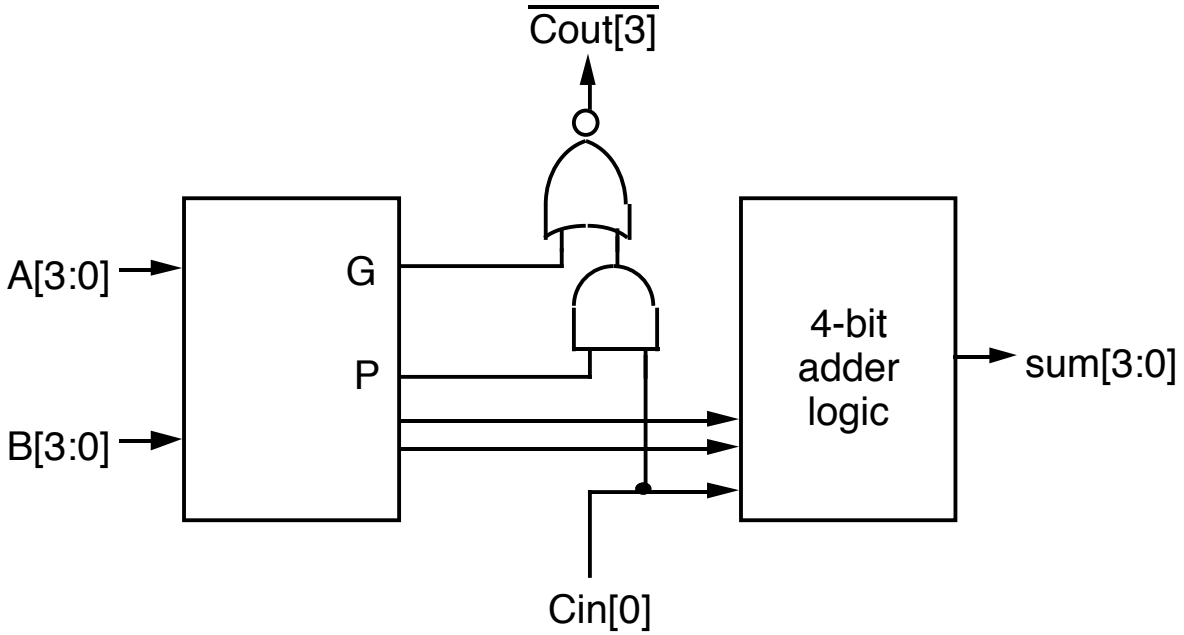
The ARM2 4-bit carry look-ahead scheme



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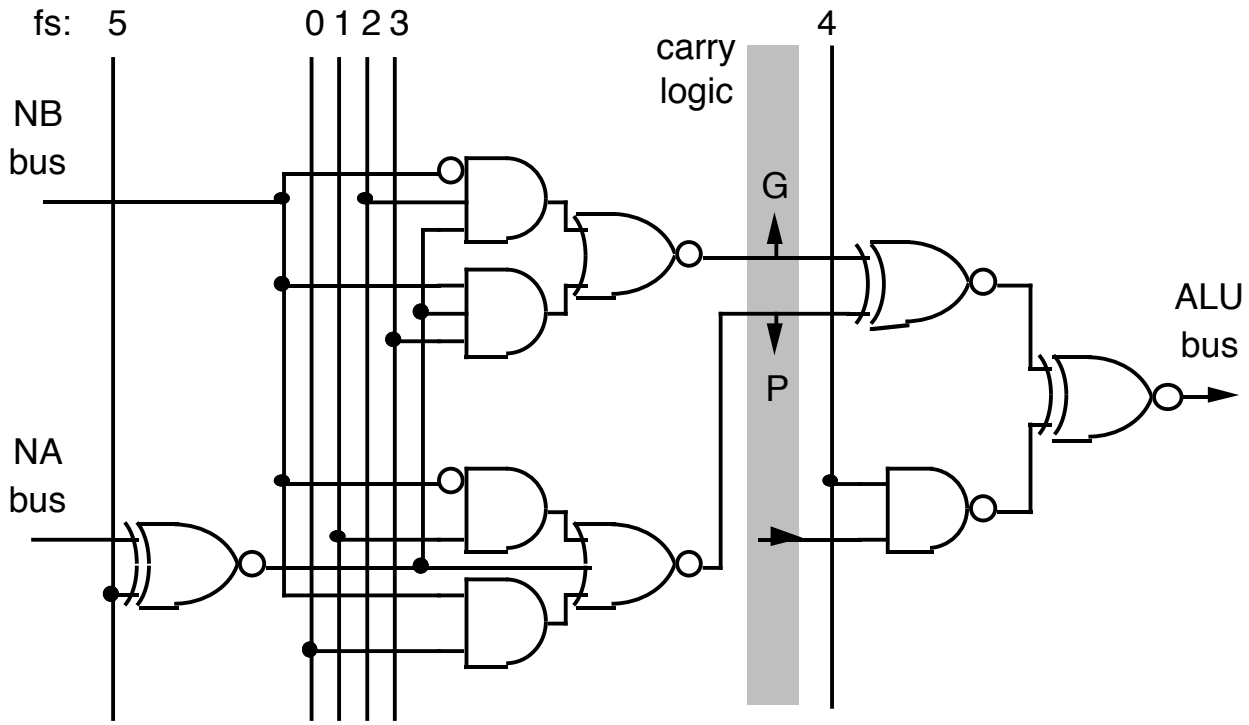
The ARM2 ALU logic for one result bit



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ARM2 ALU function codes

fs5	fs4	fs3	fs2	fs1	fs0	ALU output
0	0	0	1	0	0	A and B
0	0	1	0	0	0	A and not B
0	0	1	0	0	1	A xor B
0	1	1	0	0	1	A plus not B plus carry
0	1	0	1	1	0	A plus B plus carry
1	1	0	1	1	0	not A plus B plus carry
0	0	0	0	0	0	A
0	0	0	0	0	1	A or B
0	0	0	1	0	1	B
0	0	1	0	1	0	not B
0	0	1	1	0	0	zero

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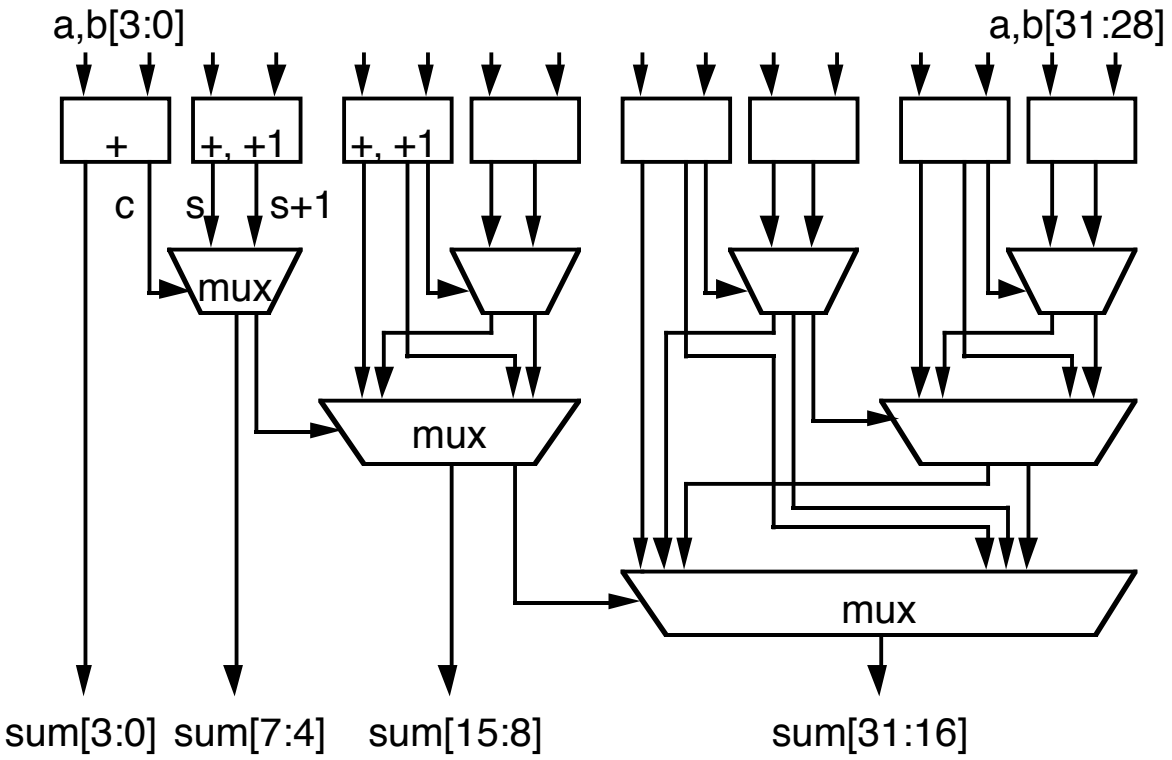
The ARM6 carry-select adder scheme



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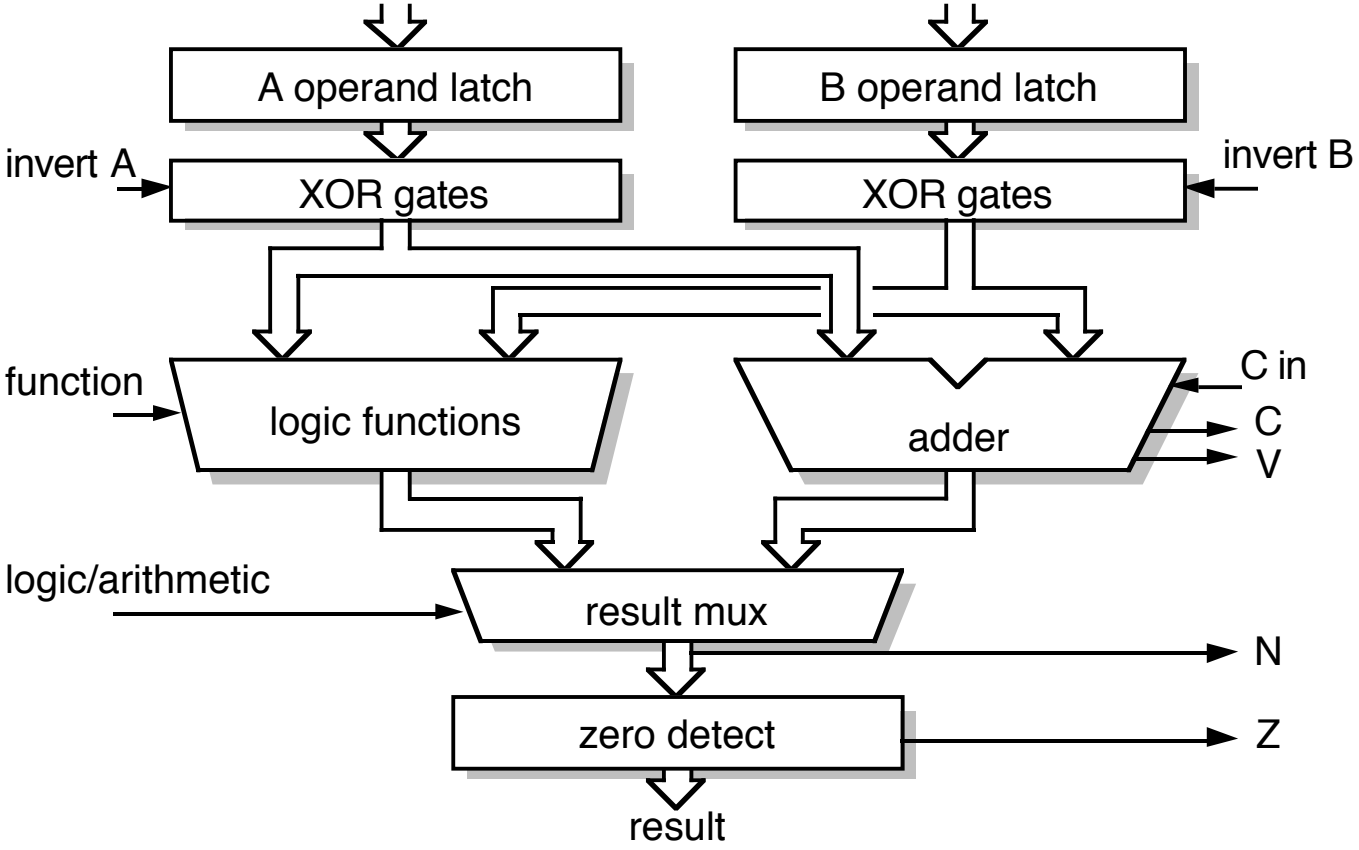
The ARM6 ALU organization



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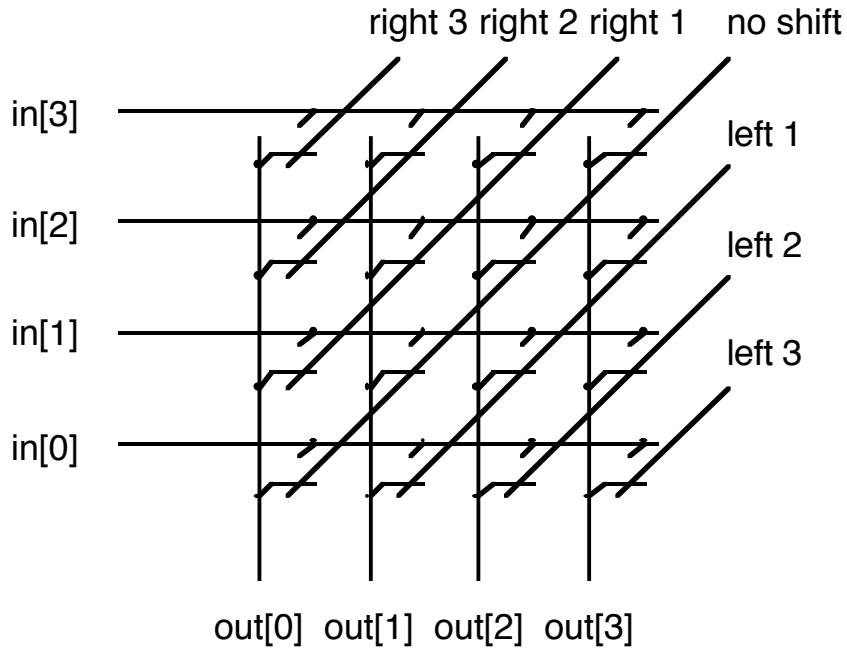
The cross-bar switch barrel shifter principle



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The 2-bit multiplication algorithm, Nth cycle

Carry-in	Multiplier	Shift	ALU	Carry-out
0	x 0	LSL #2N	A + 0	0
	x 1	LSL #2N	A + B	0
	x 2	LSL #(2N + 1)	A – B	1
	x 3	LSL #2N	A – B	1
1	x 0	LSL #2N	A + B	0
	x 1	LSL #(2N + 1)	A + B	0
	x 2	LSL #2N	A – B	1
	x 3	LSL #2N	A + 0	1

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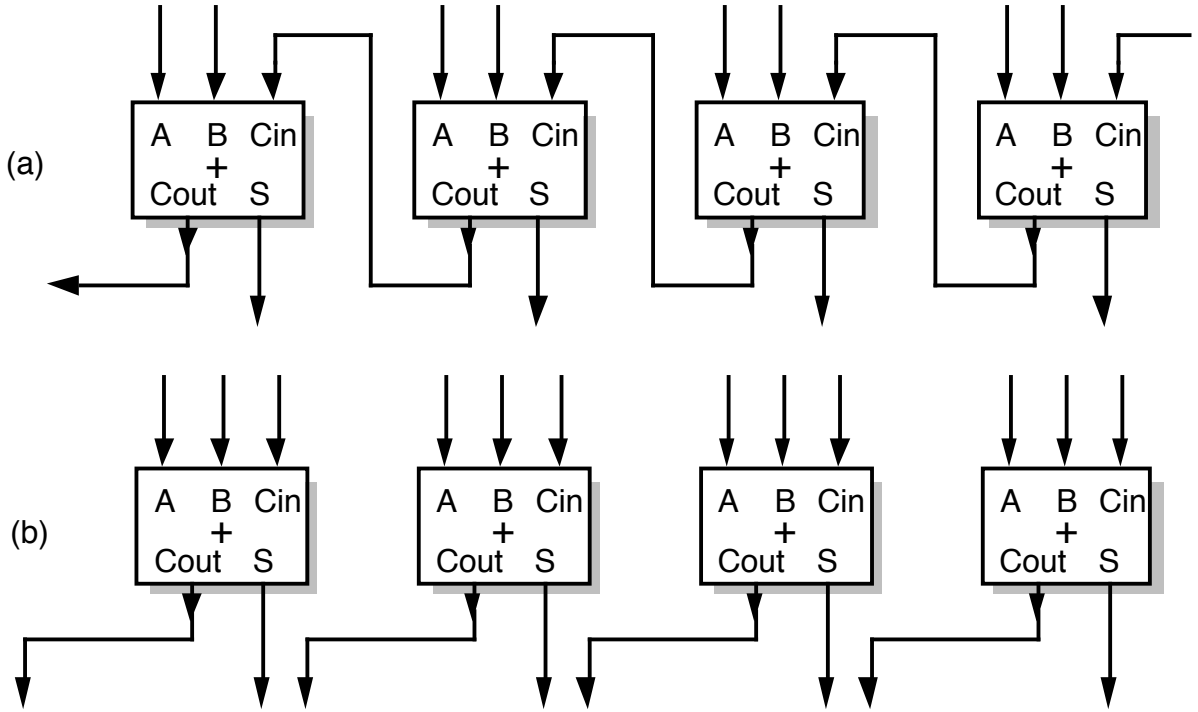
Carry-propagate (a) and carry-save (b) adder structures



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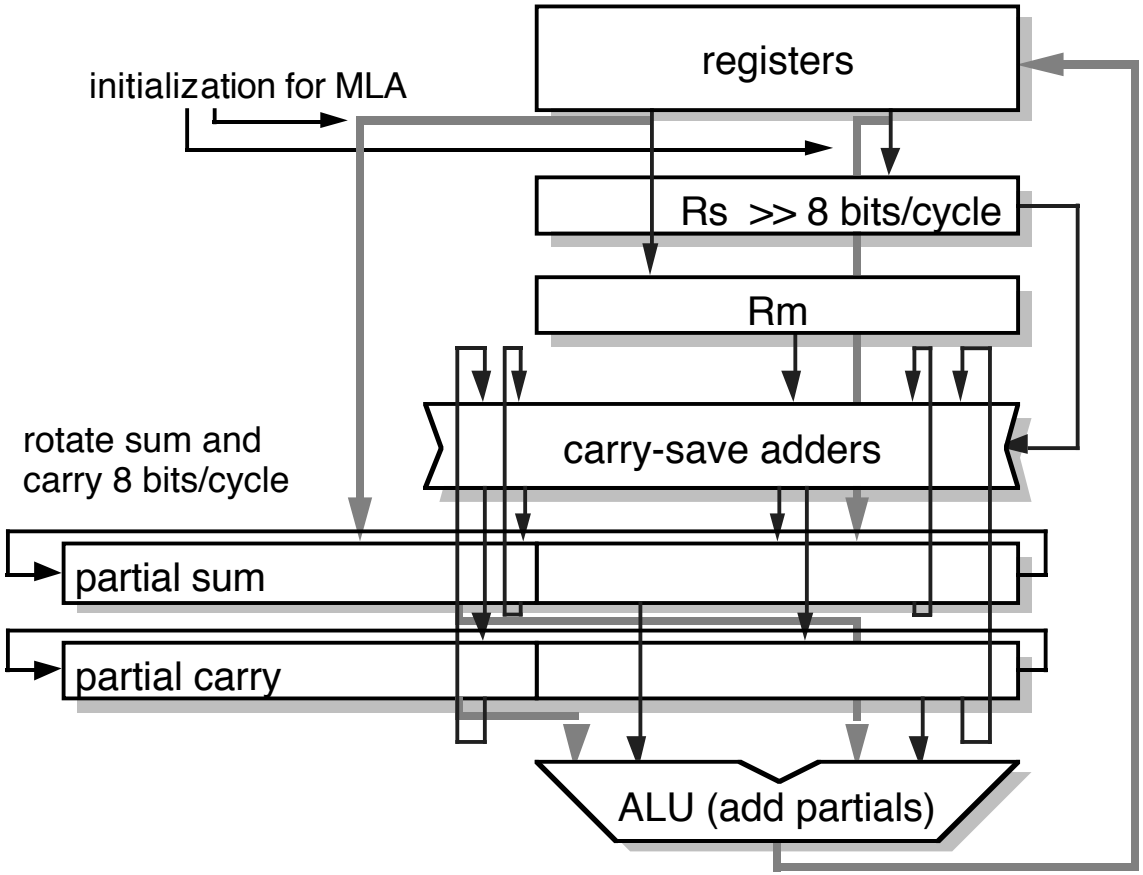
ARM high-speed multiplier organization



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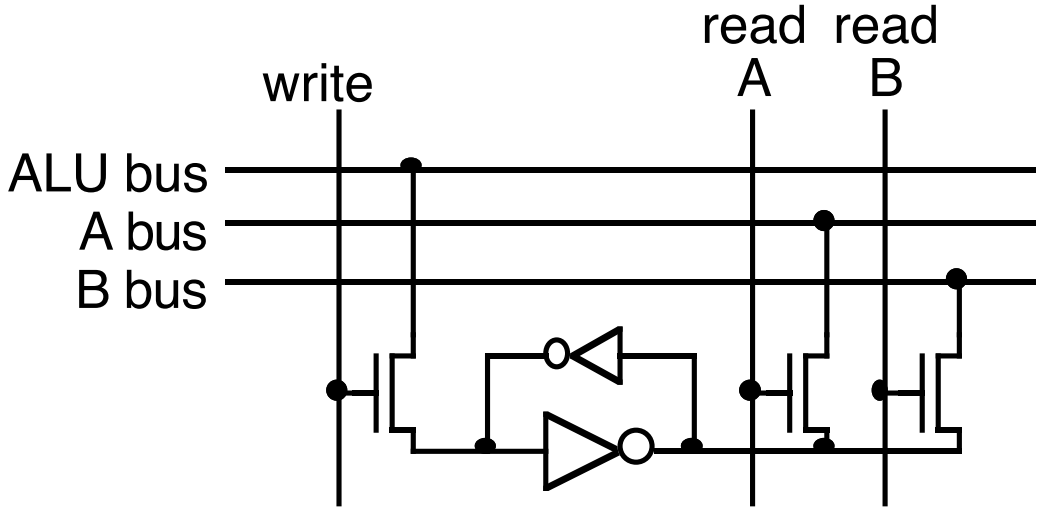
ARM2 register cell circuit



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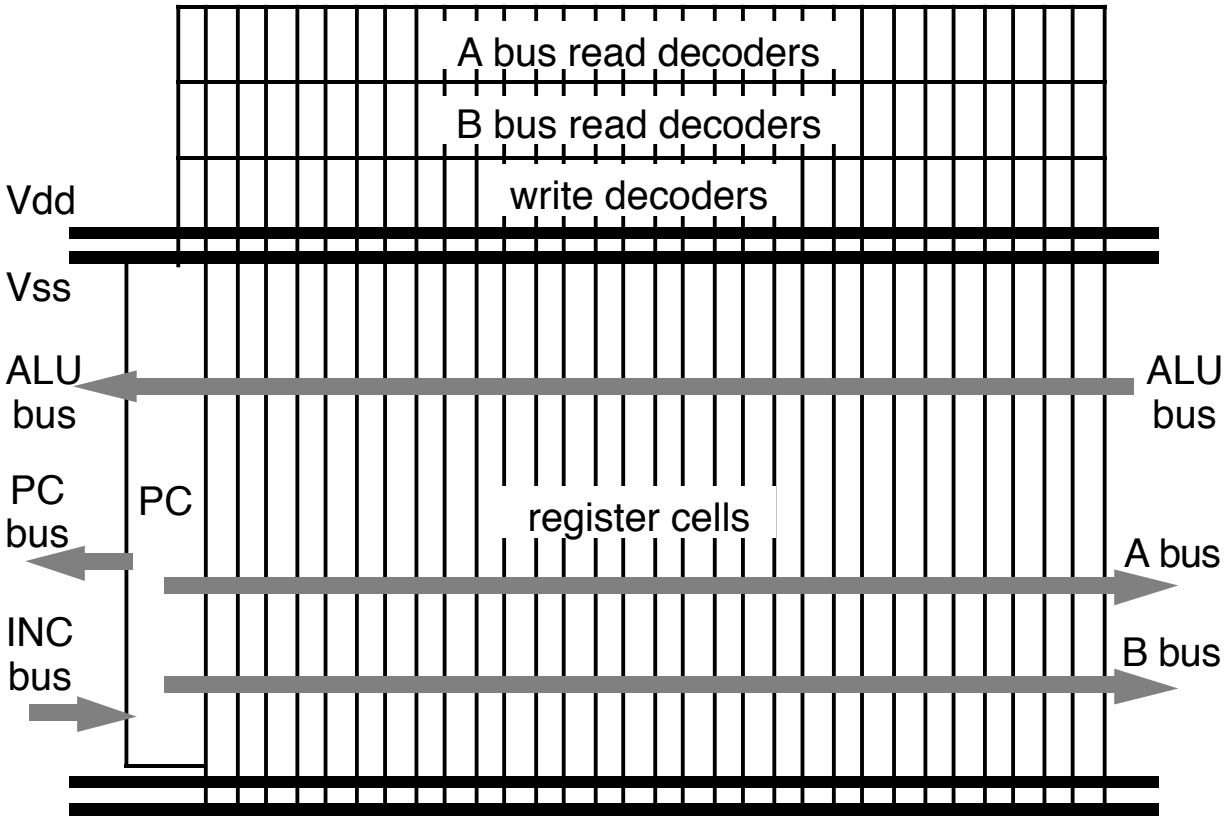
ARM register bank floorplan



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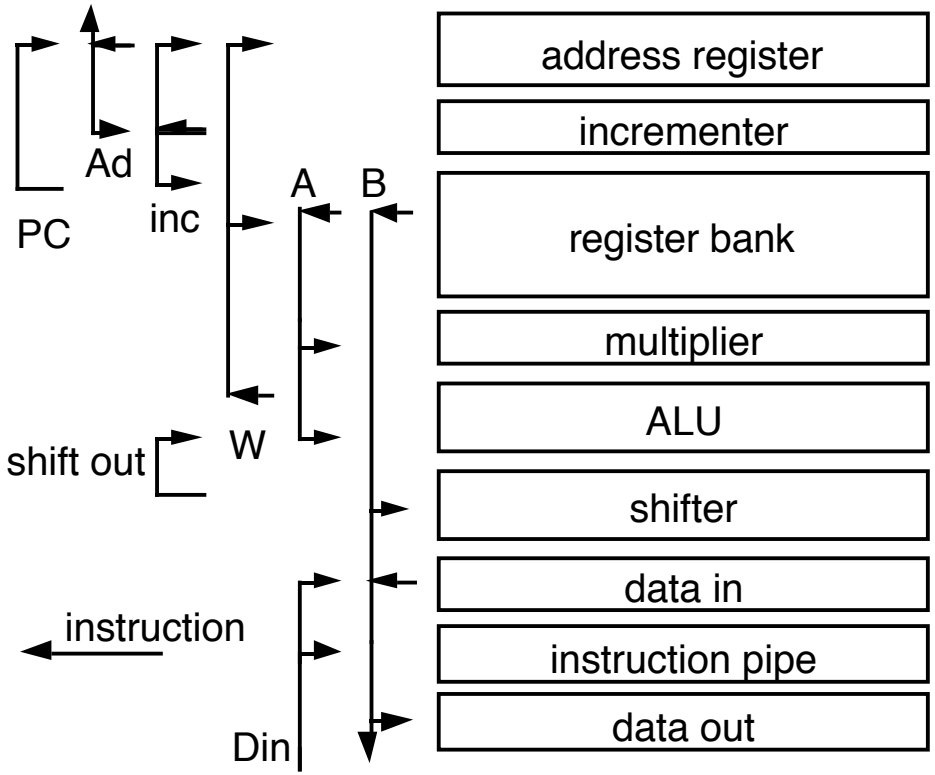
ARM core datapath buses



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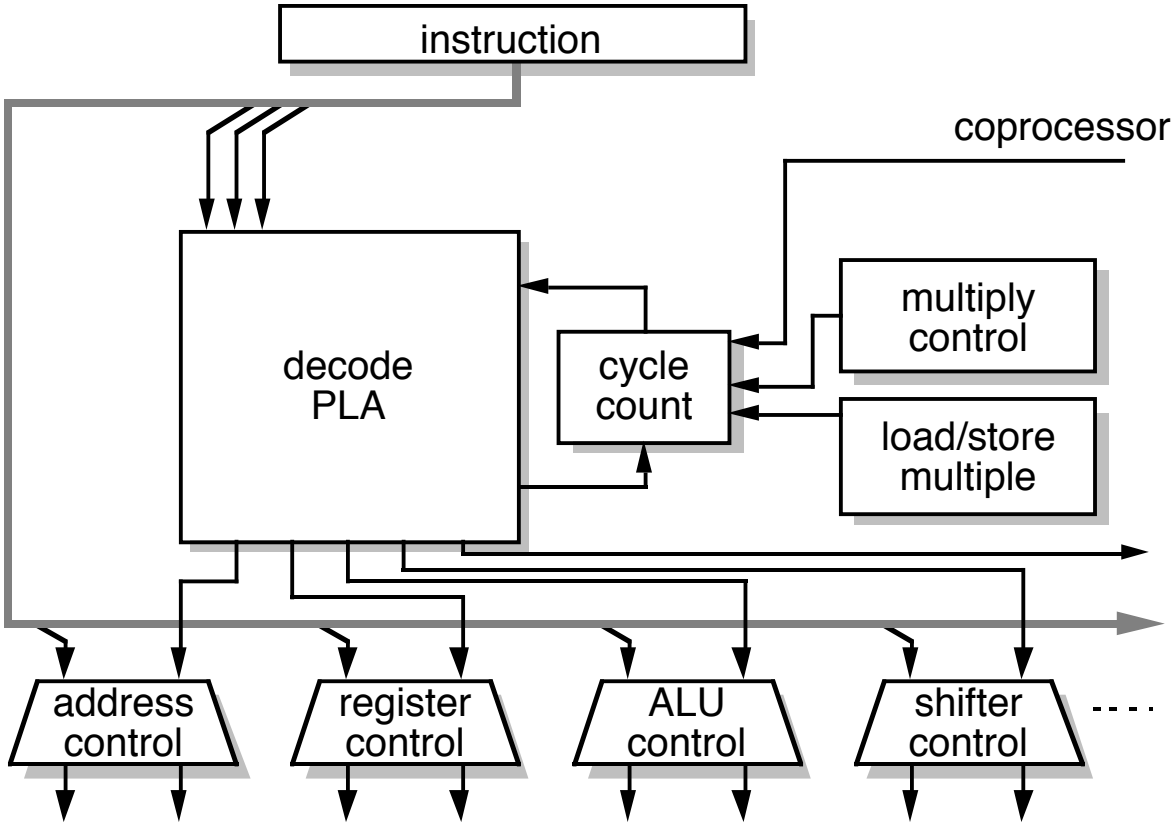
ARM control logic structure



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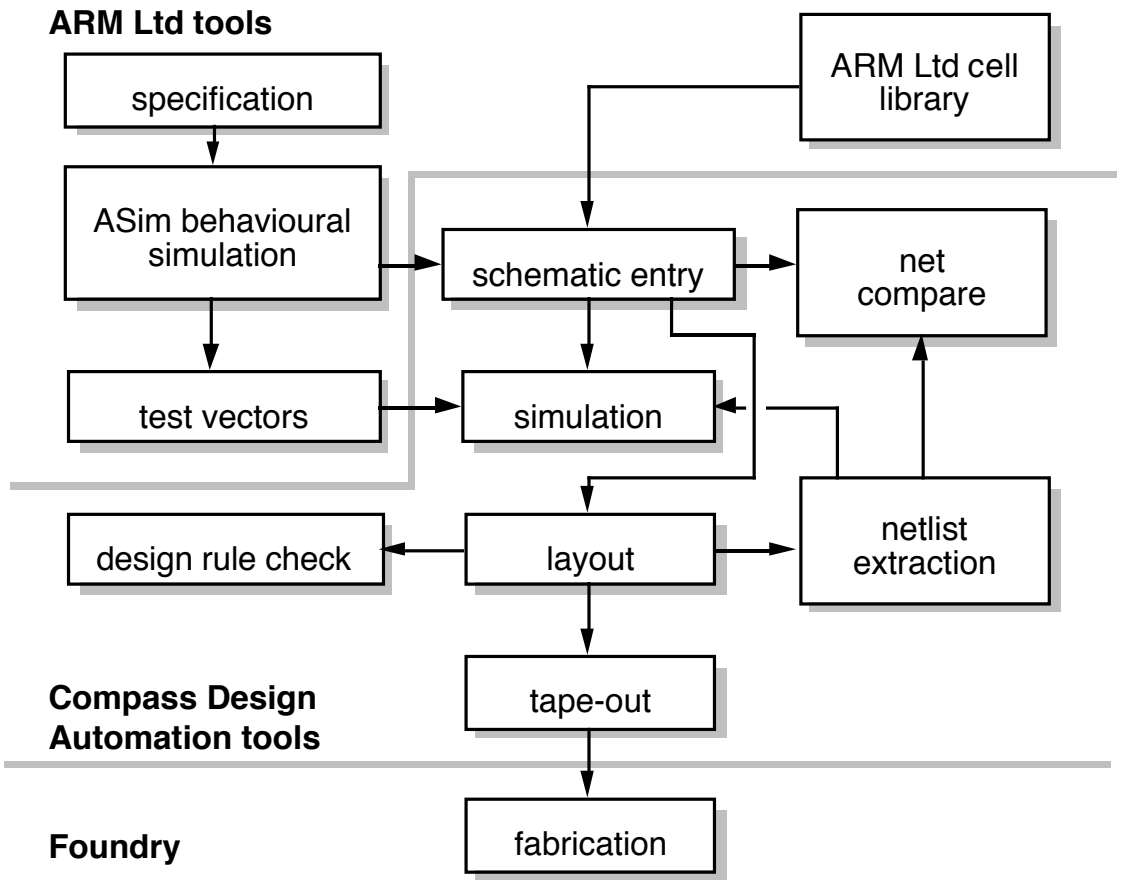
The VLSI design flow used to develop early ARM chips



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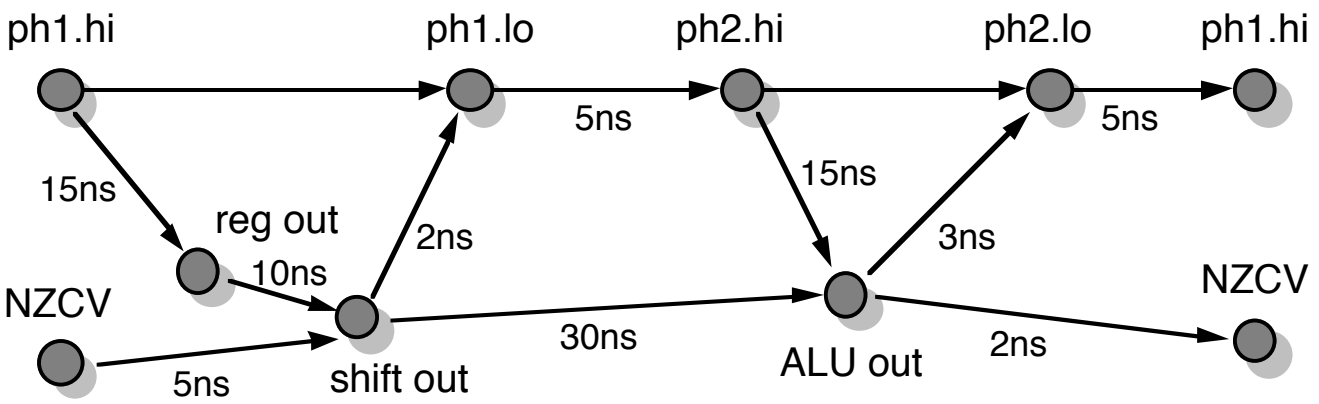
Directed graph of timing dependencies



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