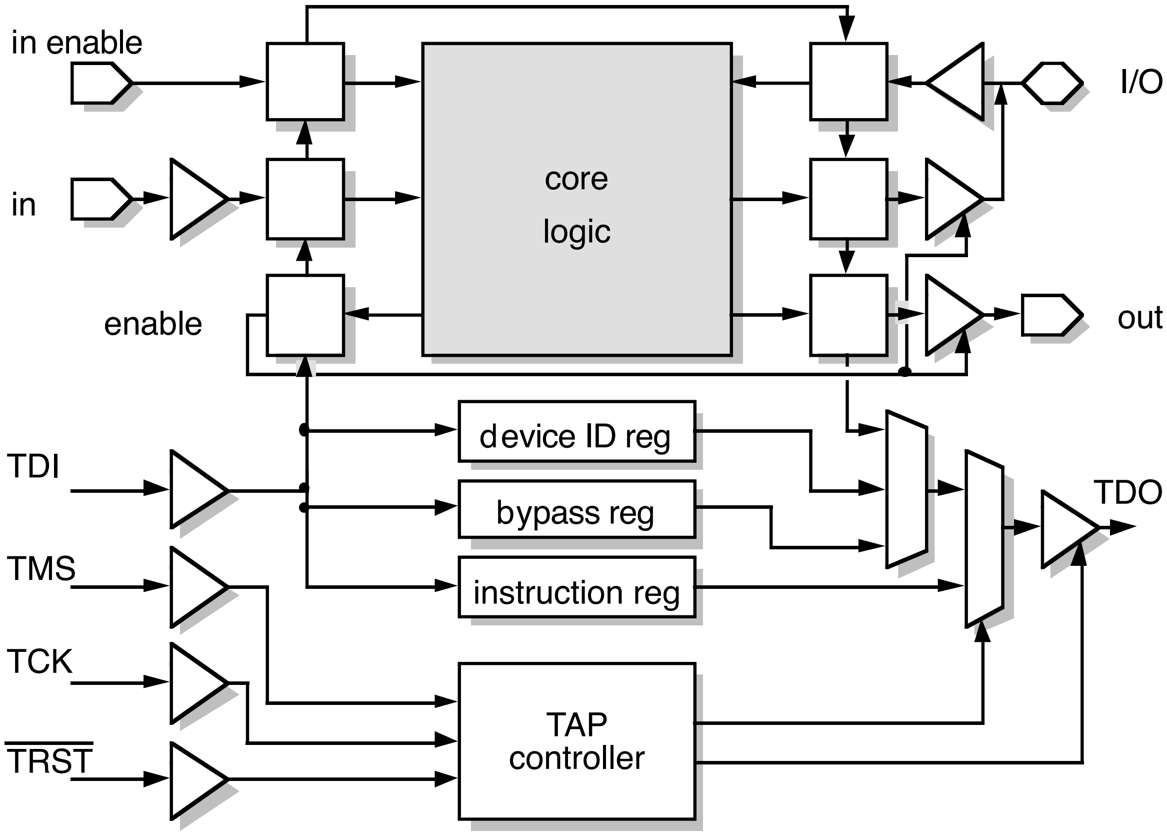
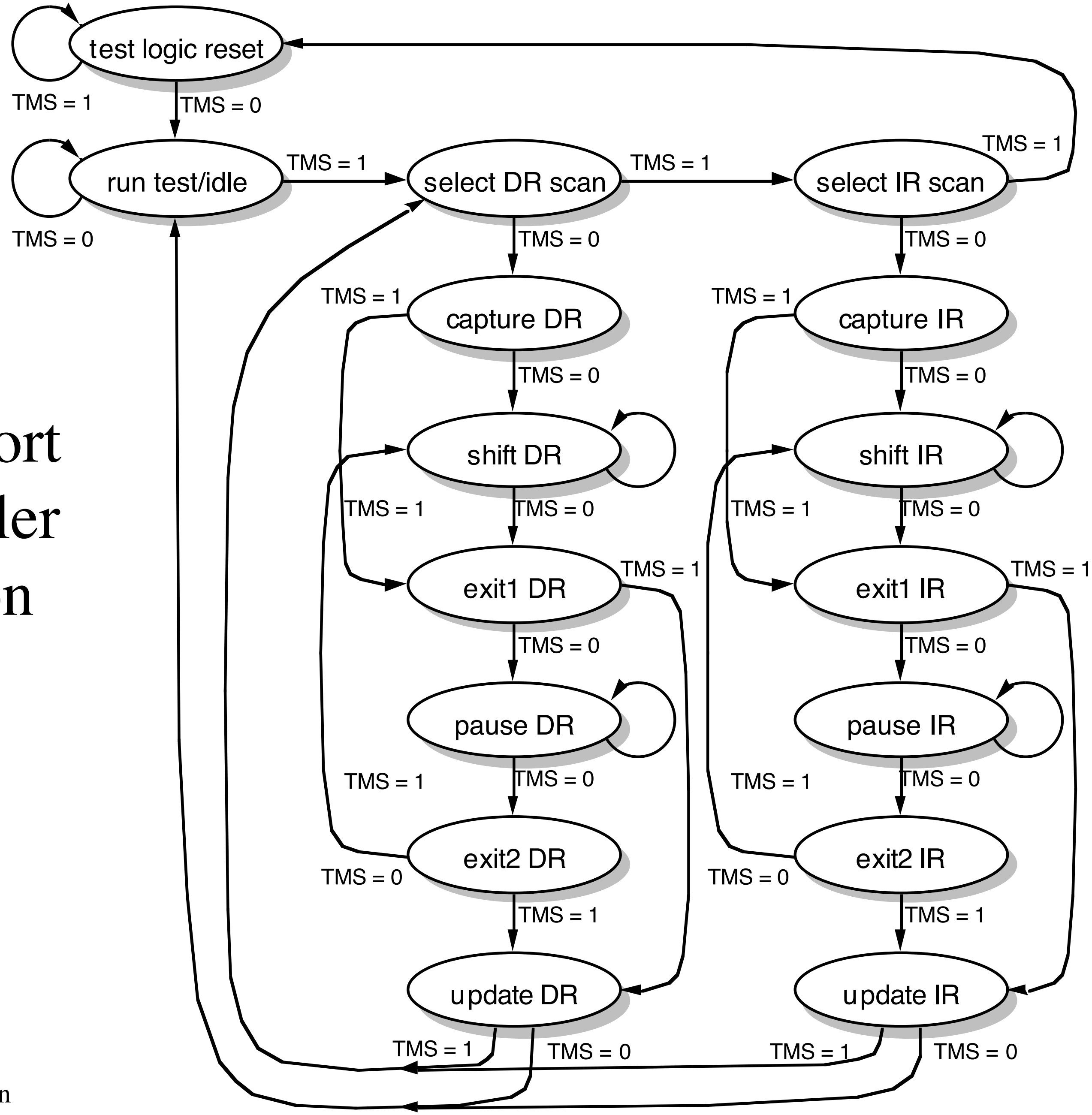
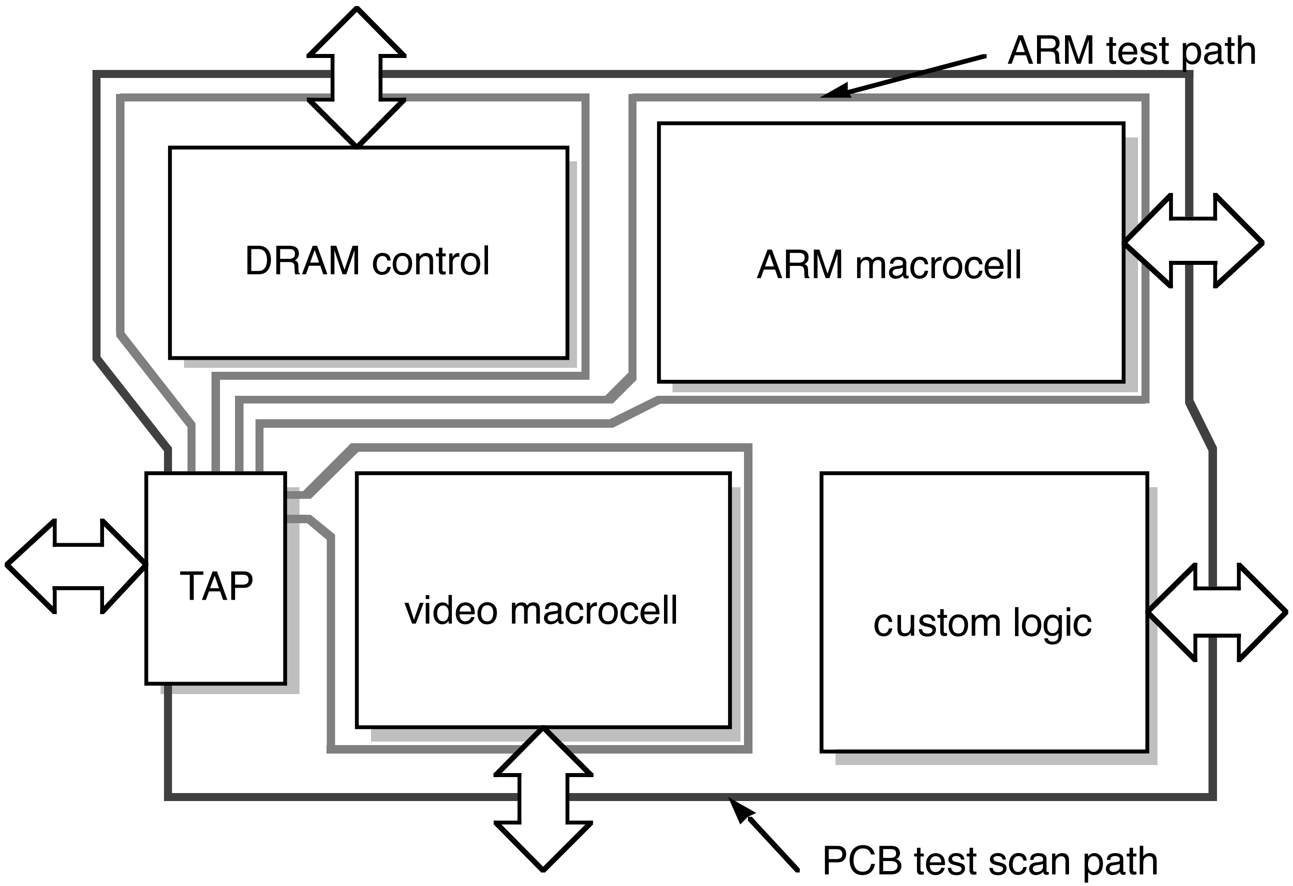
JTAG boundary scan organization



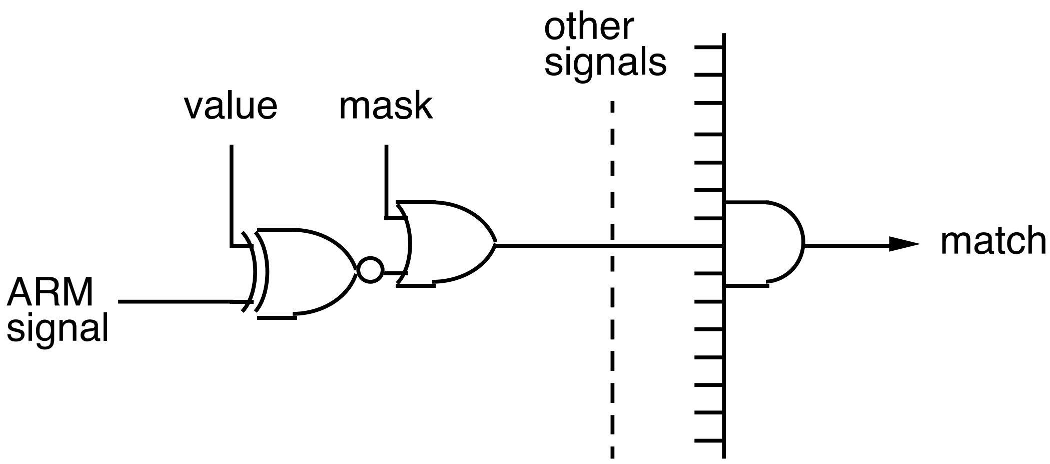
Test Access Port (TAP) controller state transition diagram



A possible JTAG extension for macrocell testing



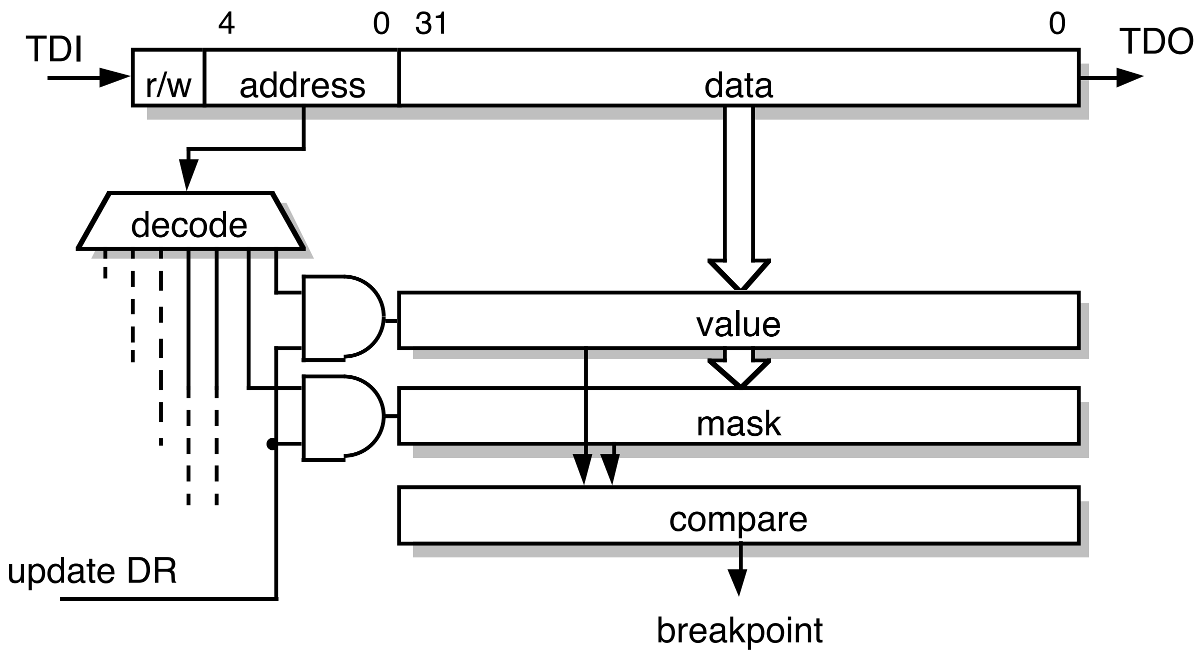
EmbeddedICE signal comparison logic



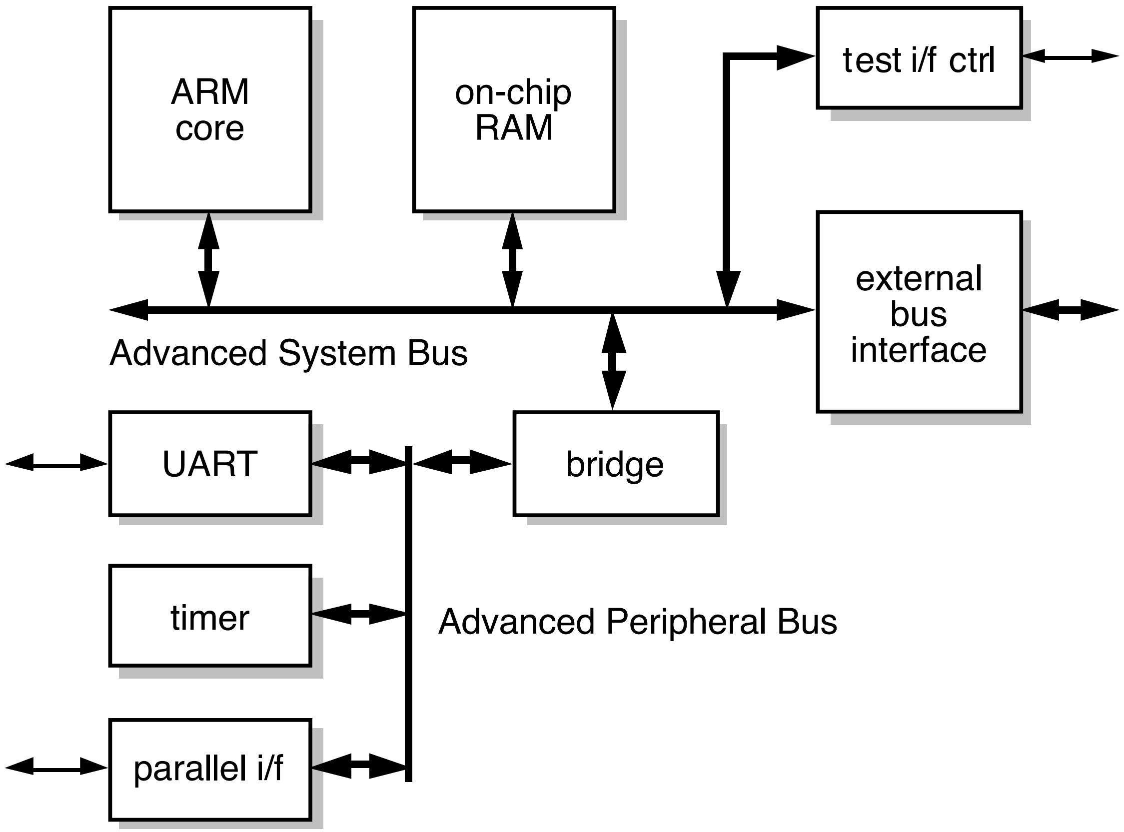
EmbeddedICE register mapping

Address	Width	Function
00000	3	Debug control
00001	5	Debug status
00100	6	Debug comms control register
00101	32	Debug comms data register
01000	32	Watchpoint 0 address value
01001	32	Watchpoint 0 address mask
01010	32	Watchpoint 0 data value
01011	32	Watchpoint 0 data mask
01100	9	Watchpoint 0 control value
01101	8	Watchpoint 0 control mask
10000	32	Watchpoint 1 address value
10001	32	Watchpoint 1 address mask
10010	32	Watchpoint 1 data value
10011	32	Watchpoint 1 data mask
10100	9	Watchpoint 1 control value
10101	8	Watchpoint 1 control mask

EmbeddedICE register read and write structure



A typical AMBA-based system



ASB bus mode state transition graph.