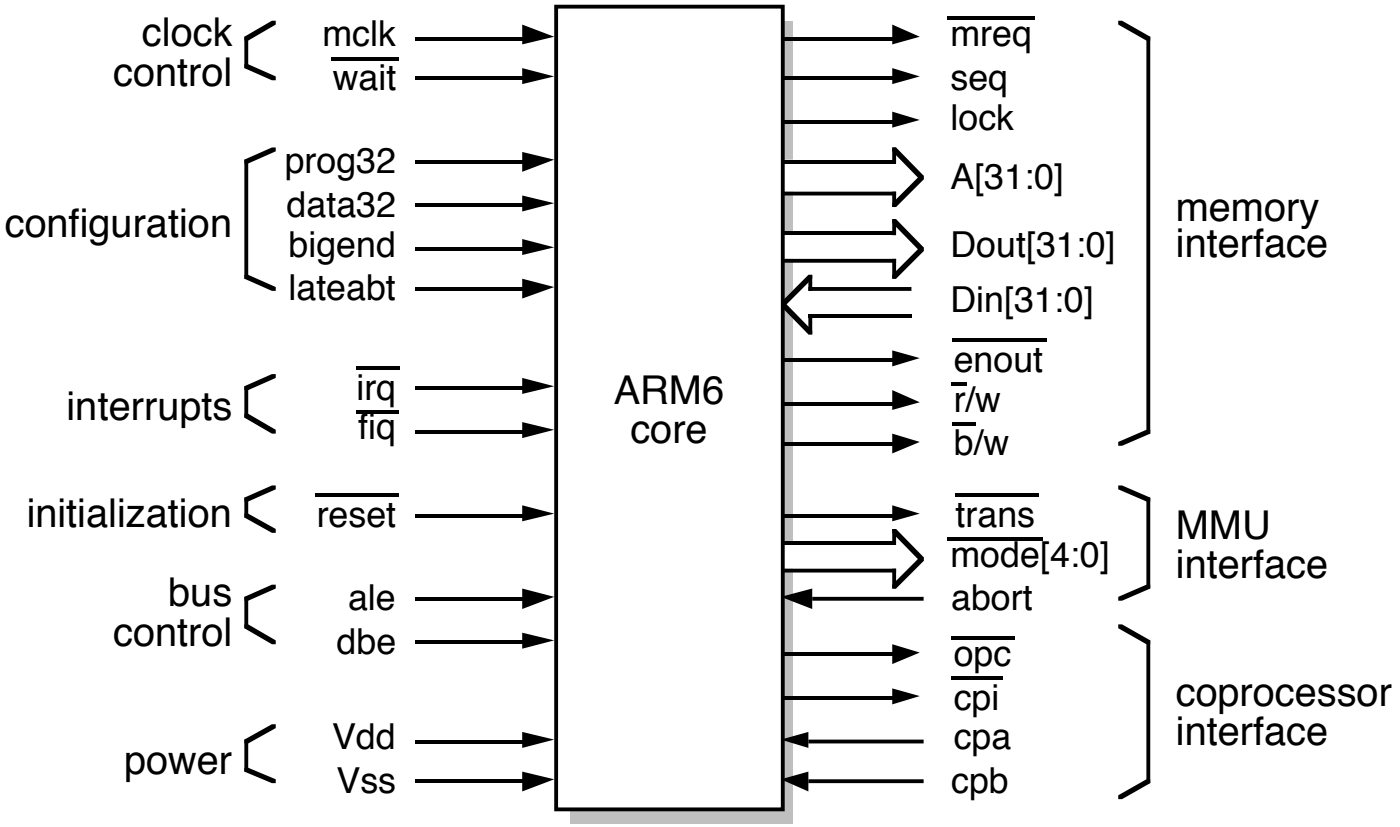
The ARM6 core interface signals



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ARM6 cycle types

mreq	seq	Cycle	Use
0	0	N	Non-sequential memory access
0	1	S	Sequential memory access
1	0	I	Internal cycle – bus and memory inactive
1	1	C	Coprocessor register transfer – memory inactive

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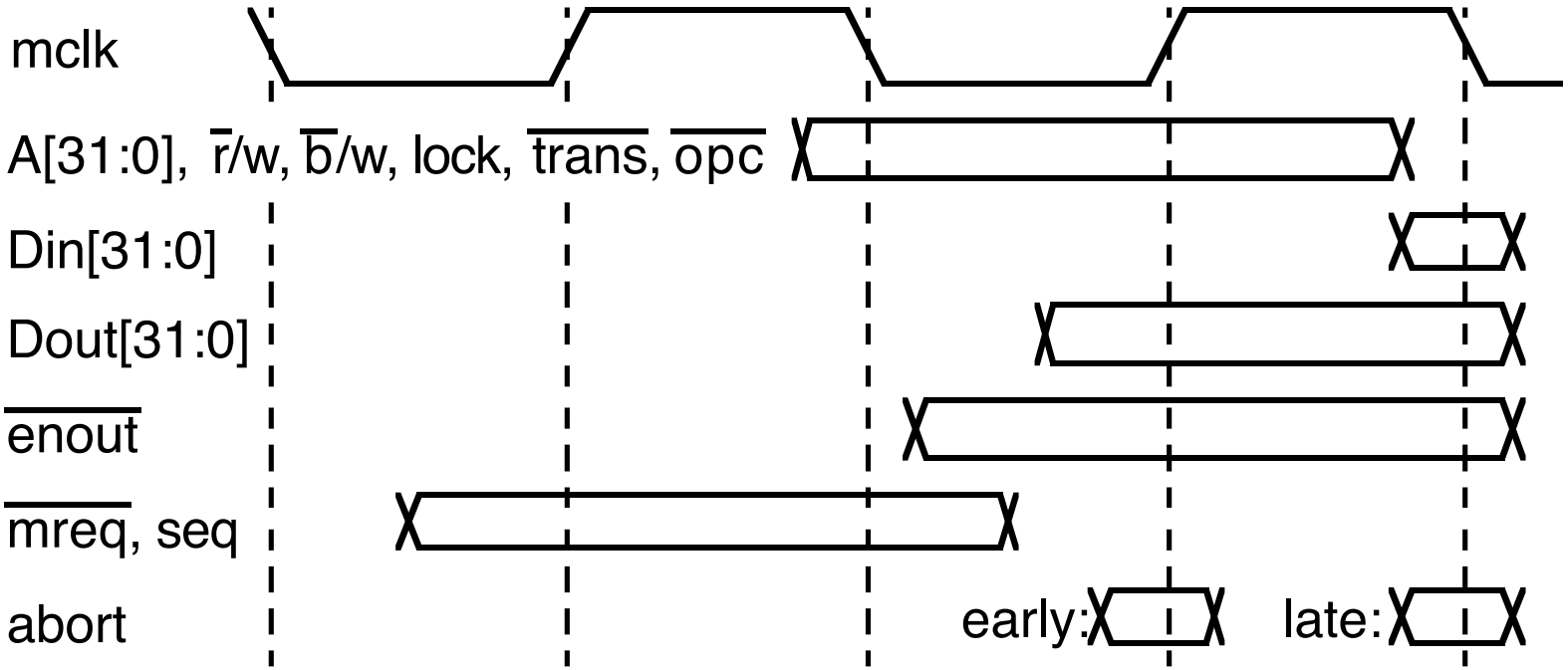
ARM6 core memory and MMU interface timing



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ARM60 characteristics

Process	0.6 μm	**Transistors**	42,748	**MIPS**	36
Metal layers	2	**Die area**	16 mm^2	**Power**	360 mW
Vdd	5 V	**Clock**	0 to 40 MHz	**MIPS/W**	100

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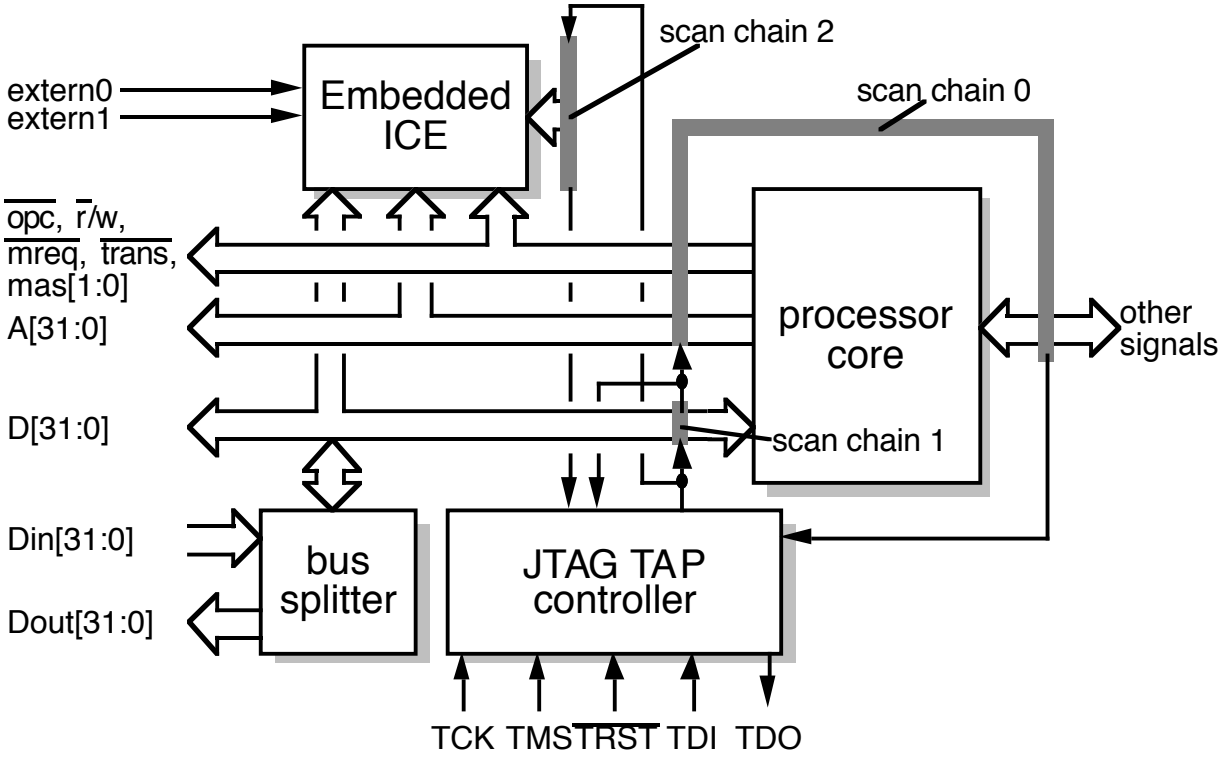
ARM7TDMI organization



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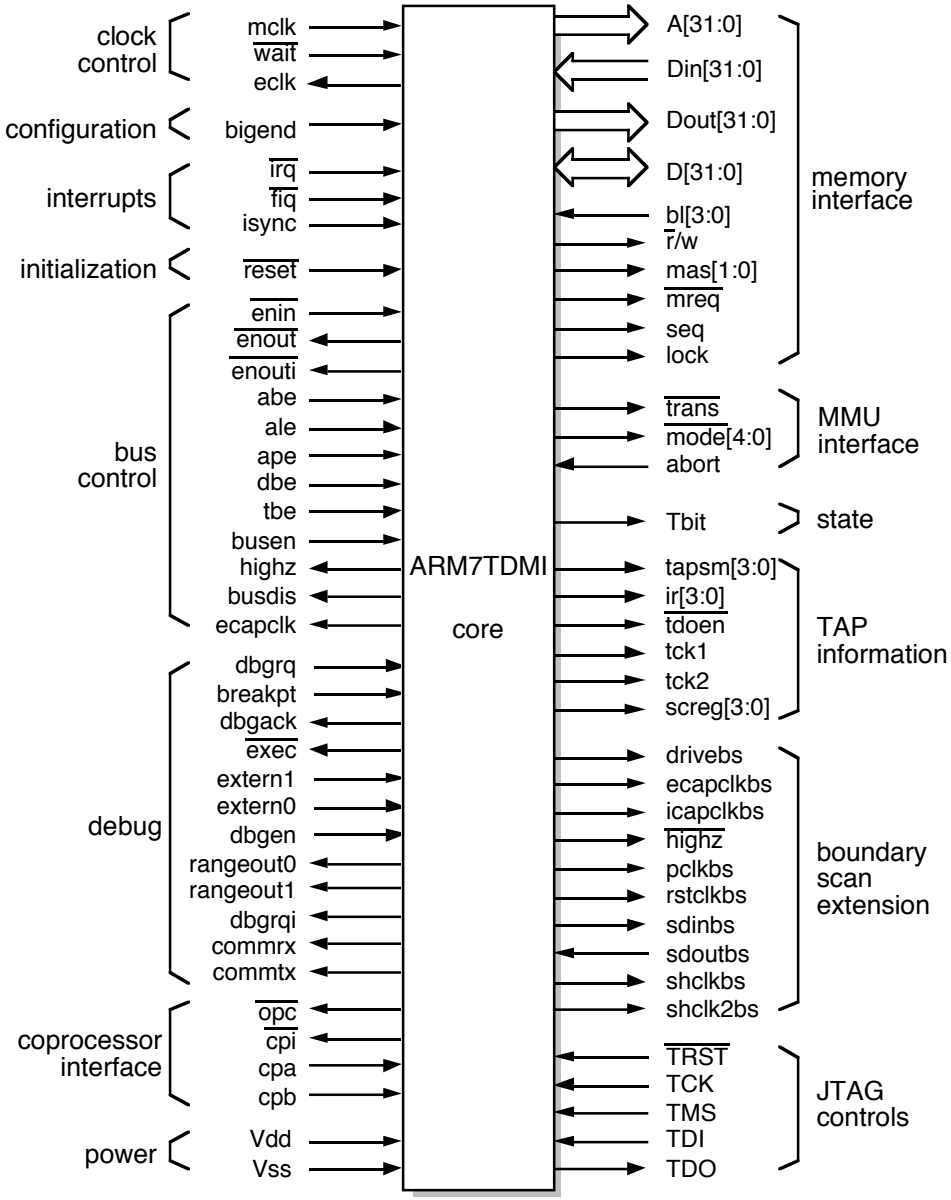
The ARM7TDMI core interface signals



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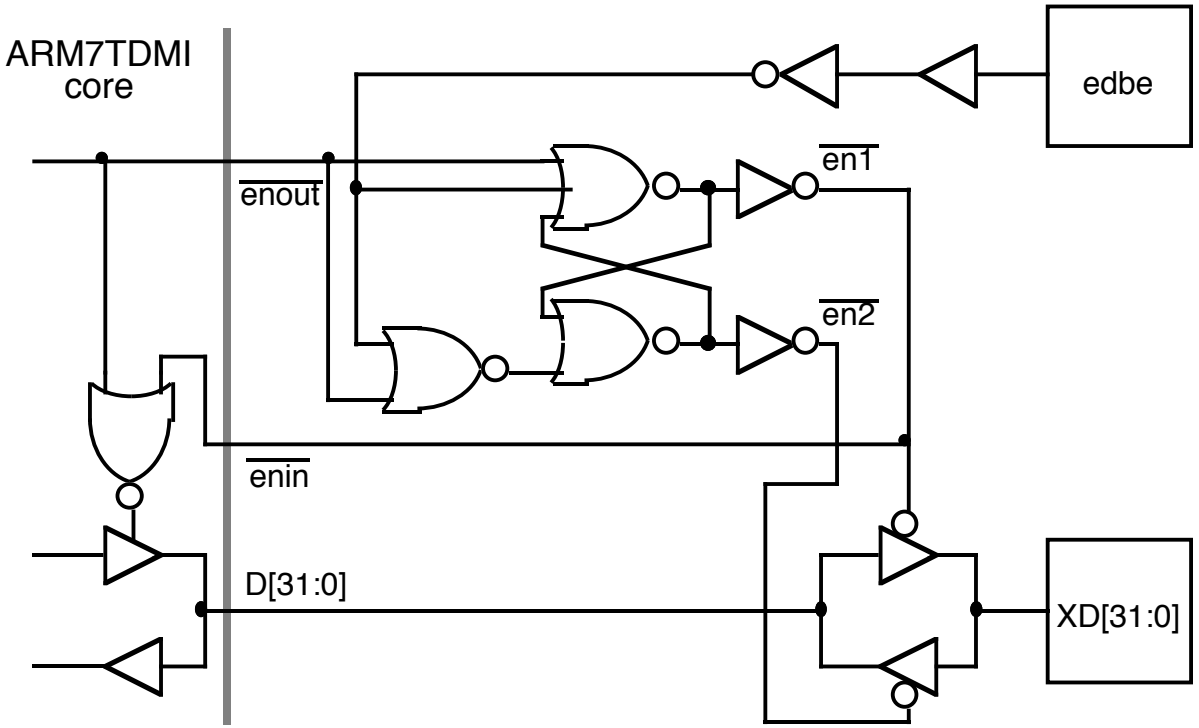
Data bus control circuit



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ARM7TDMI characteristics

Process	0.6 μm	**Transistors**	74,209	**MIPS**	36
Metal layers	3	**Core area**	5 mm^2	**Power**	80 mW
Vdd	3.3 V	**Clock**	0 to 40 MHz	**MIPS/W**	450

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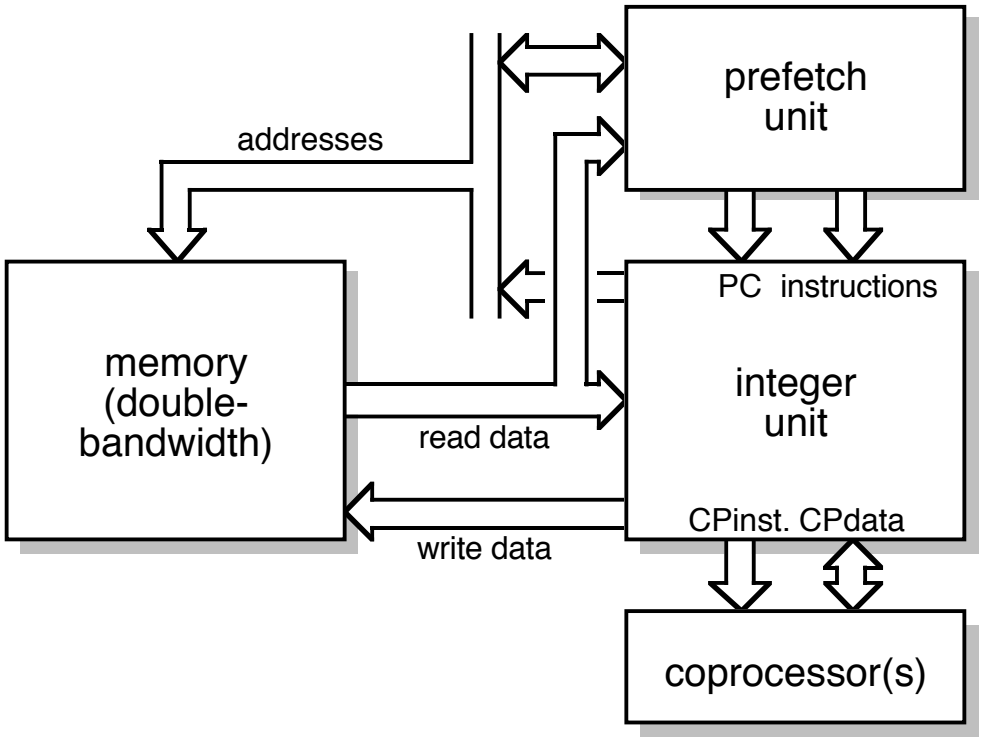
ARM8 processor core organization



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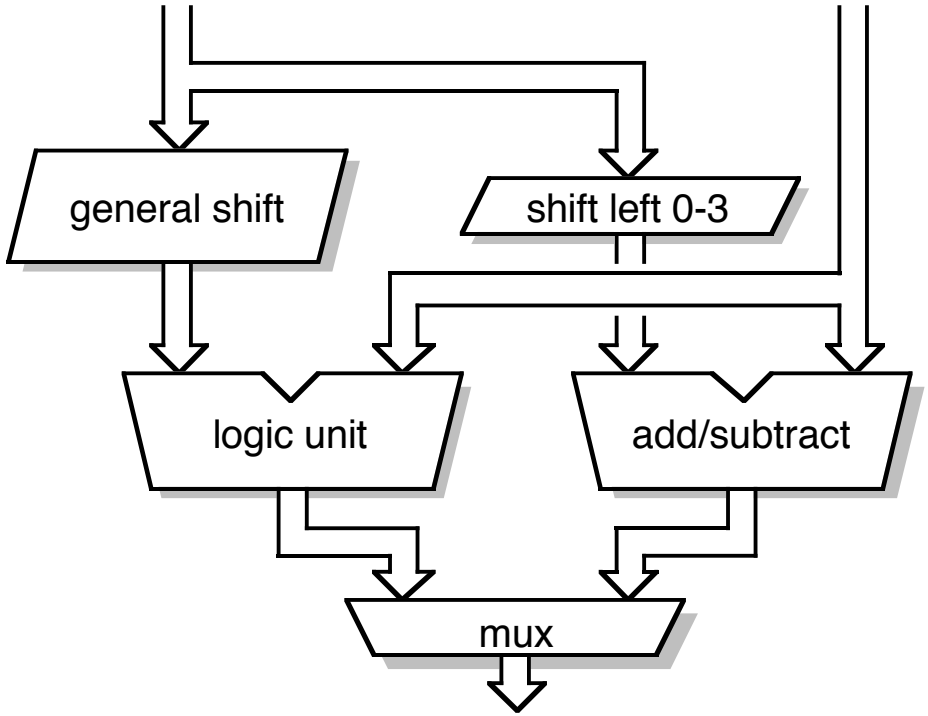
ARM8 ALU/Shifter organization



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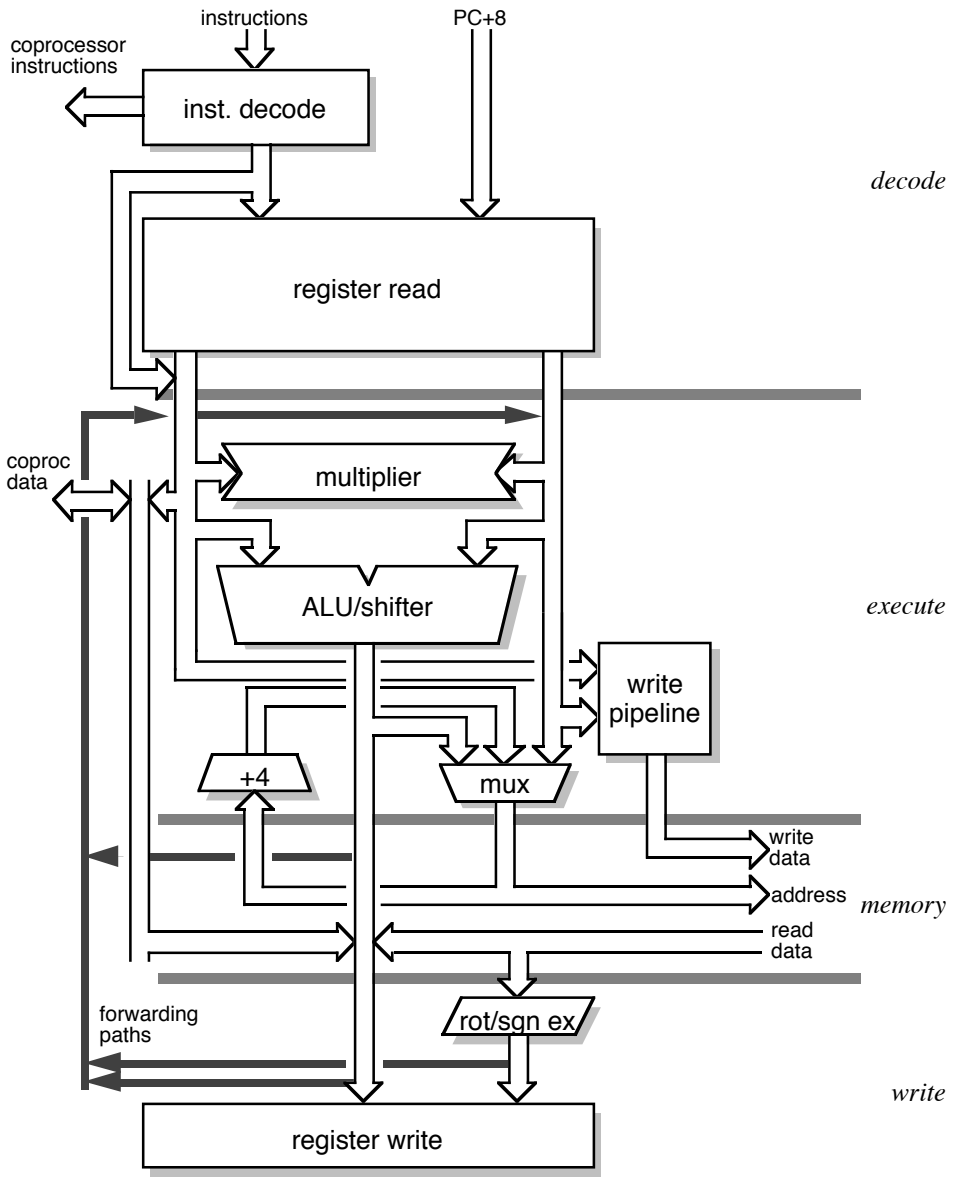
ARM8 integer unit organization



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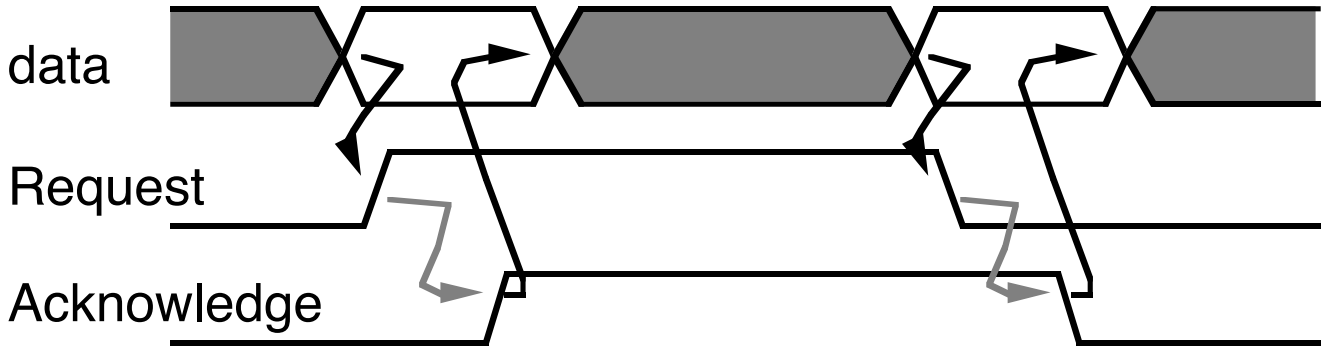
Transition-signalling communication protocol



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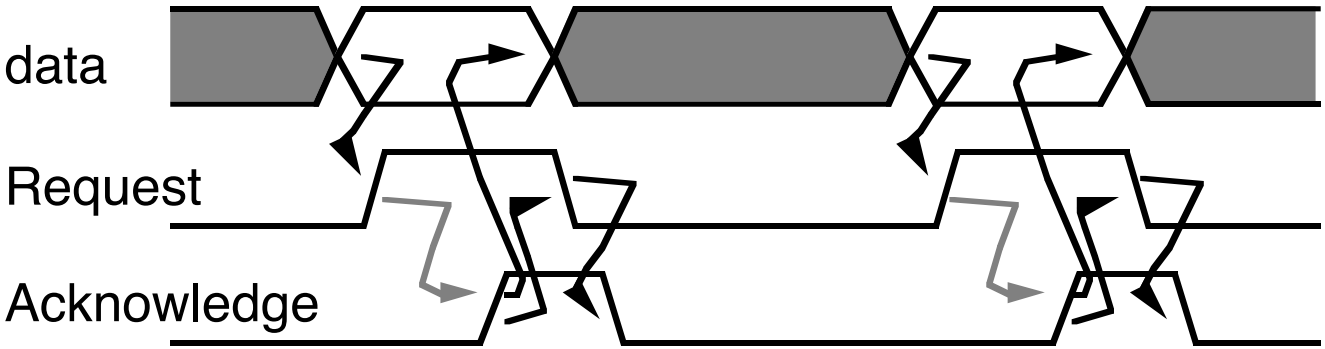
Level-signalling communication protocol



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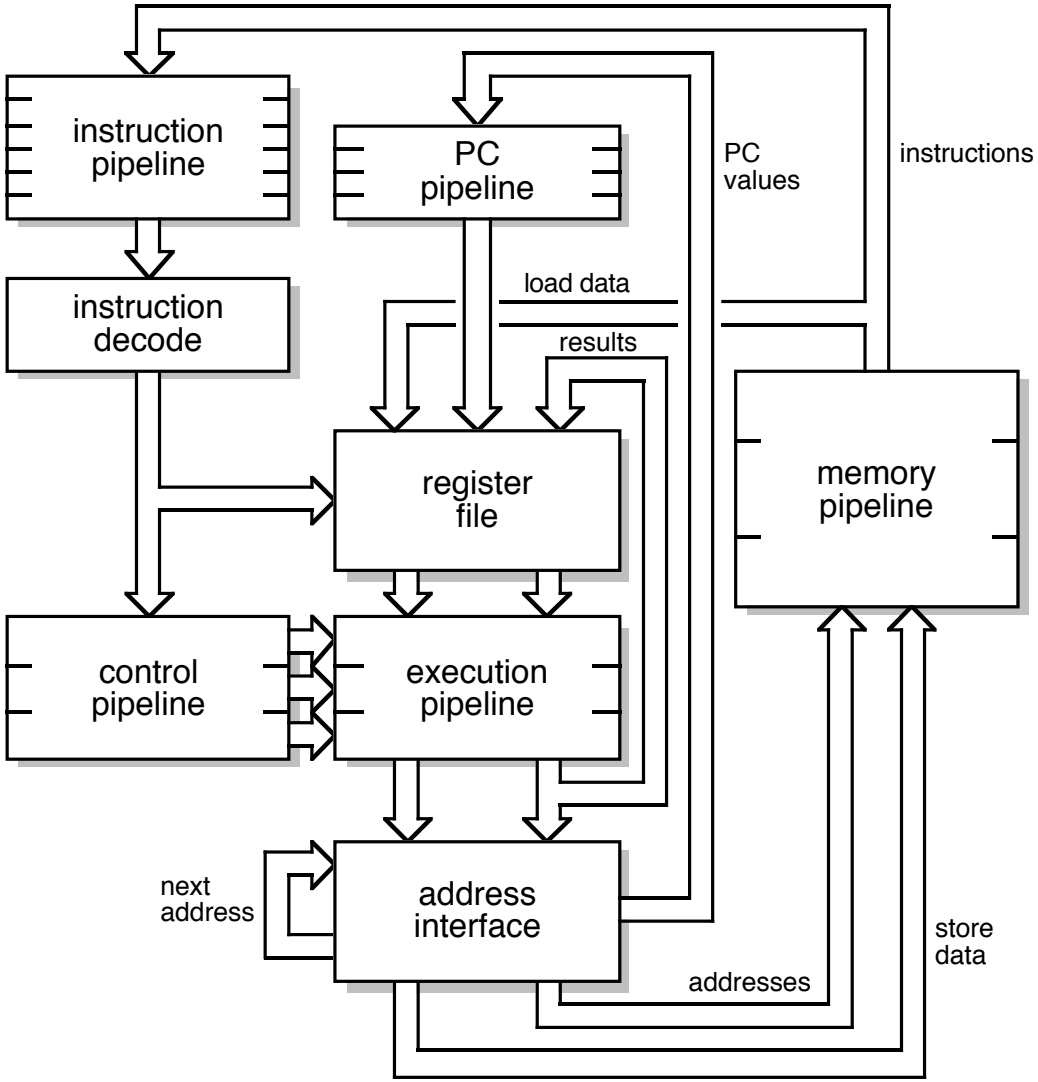
AMULET internal organization



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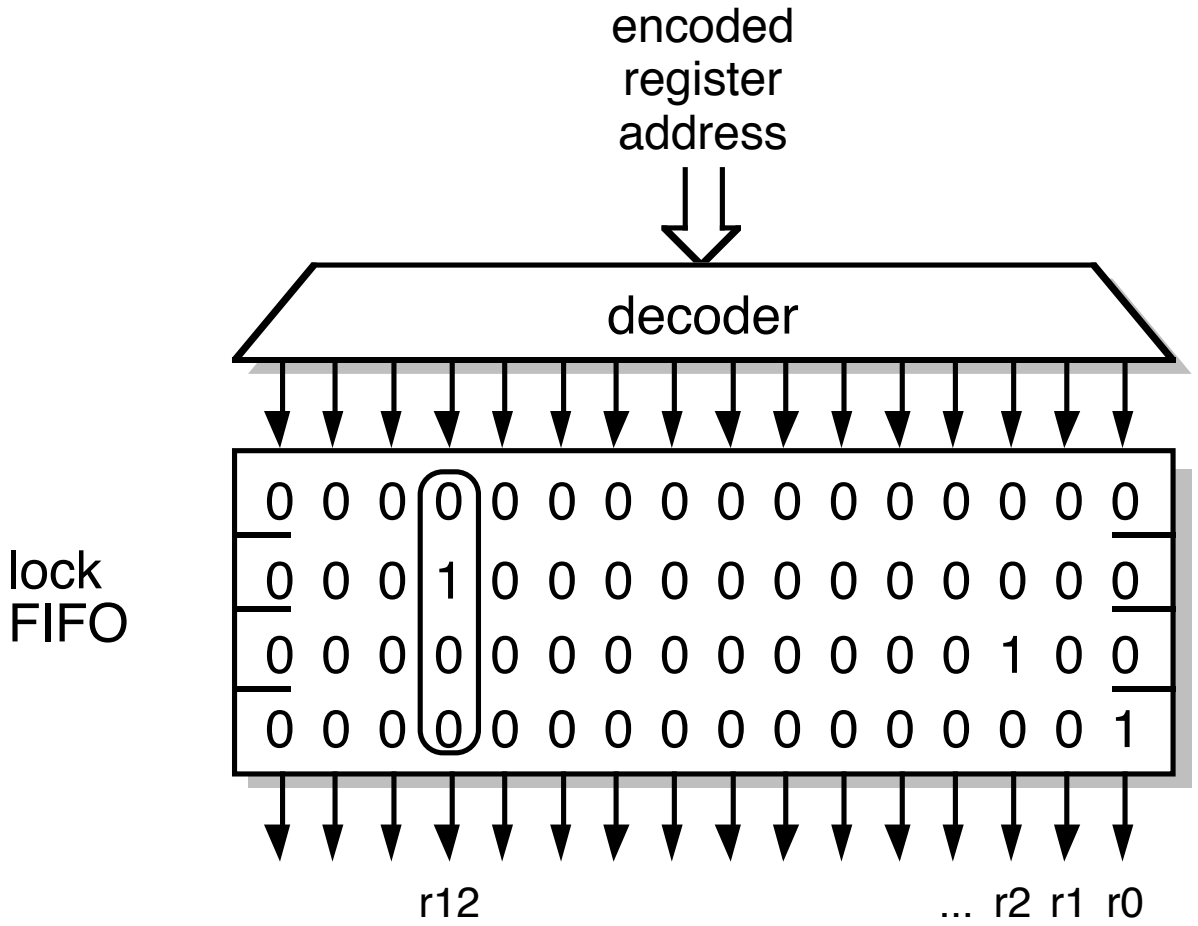
AMULET register lock FIFO organization



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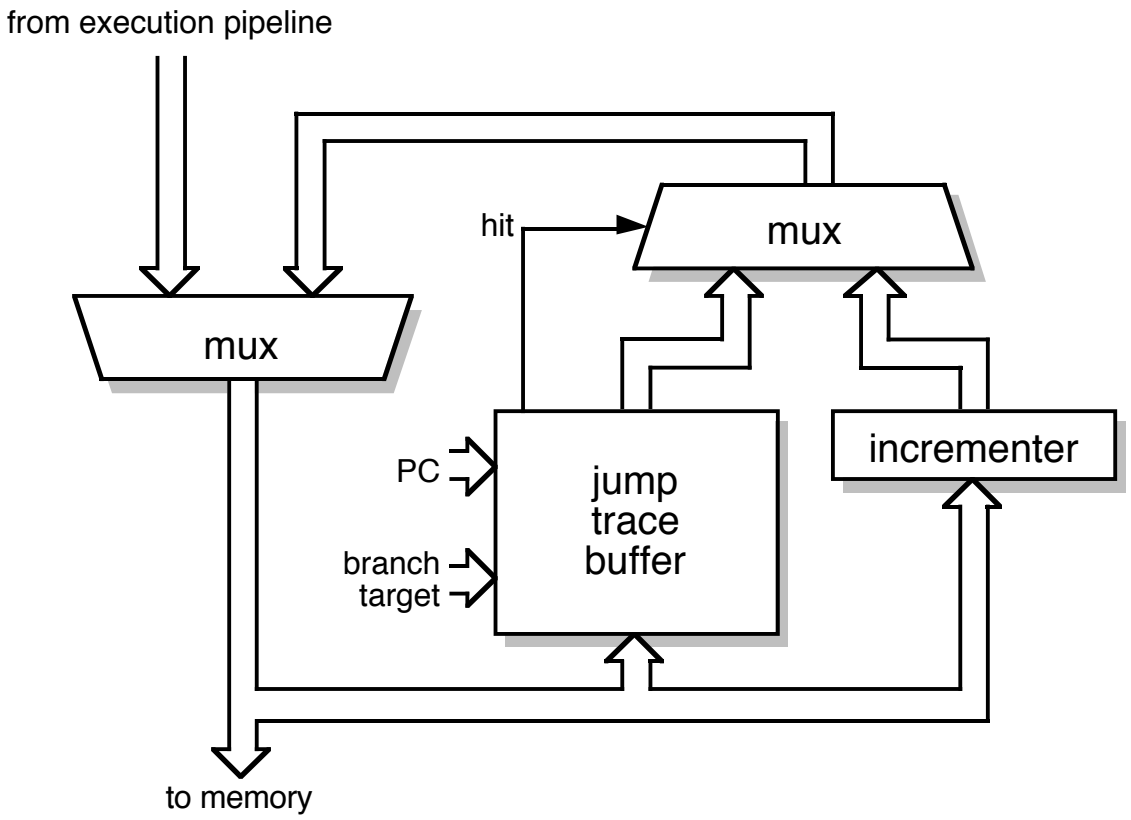
The AMULET2 jump trace buffer



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AMULET2 branch prediction statistics

Prediction algorithm	Correct	Incorrect	Redundant fetches
Sequential	33%	67%	2 per branch (ave.)
Trace buffer	67%	33%	1 per branch (ave.)

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AMULET1 characteristics

	AMULET1/ES2	AMULET1/GPS	ARM6
Process	1□um	0.7□um	1□um
Area (mm^2)	5.5 x 4.1	3.9 x 2.9	4.1 x 2.7
Transistors	58,374	58,374	33,494
Performance	20.5 kDhrystones	~40 kDhrystones	31 kDhrystones
Multiplier	5.3□ns/bit	3□ns/bit	25□ns/bit
Conditions	5□V, 20°C	5□V, 20°C	5□V, 20□MHz
Power	152□mW	N/A	148□mW
MIPS/W	77	N/A	120

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